# Start to Work with Simulators

Simulators are used in Computer Architecture quite often to be able to measure the performance of a hardware design without making a real implementation. In this homework, you are asked to make a simple measurement in gem5; a cycle-accurate simulator.

Gem5 is a full system simulator and you can simulate Alpha, ARM, SPARC, MIPS, POWER, RISC-V and x86 ISAs. For this homework, it is enough for you to simulate X86 ISA so that you can compile the application, that you want to run on the simulator, in your host computer. gem5 supports both full system (meaning all the disk access operations and the operating system) and standard edition and you can use either of it. The simulator is working on the linux/unix environment and most probably Windows is not supported in it. The home page of the simulator is <http://gem5.org>.

Definition: In this homework, you need to measure the effect of **block size** on the performance of **data cache** by simulating Matrix Multiplication application in gem5 simulator.

* You can use any implementation of matrix multiplication and take the source code from any resource as far as you reference it.
* For the input matrixes, you can generate two random matrixes with the size at least 20x20 integer in each.
* You need to put both compiled/executable file of the matrix multiplication application and input files into gem5 simulator.
* For the hardware definitions, you need to simulate **64KB L1 Instruction Cache and 64KB L1 Data cache** .
* You need to repeat the simulation for several block sizes of L1 Data cache such as; 2B, 4B, 8B, 16B, 32B and measure the hit rate for L1 Data cache.
* Finally, you need to put those hit rates in a table and draw the hit rate vs block size graph.
* For the submission, you need to submit the link of a 3-minute video that you take including following information.
  + Which files in the simulator you mainly changed?
  + What is the main code you added into the simulator (not all the lines, just your main change is enough)
  + Table showing the L1 hit rate for different block sizes for the L1 data cache.
  + Graph showing the changes in the hit rate according to the block size for L1 data cache.