Sistemas Digitais Trabalho 3

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Modelagem dos dados

Numero de peças fabricadas por dia para cada funcionário A a O

Funcionarios	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
A	10	9	11	13	14	13	15	15	12	13	15	16	17	11	10	9	7	8	13	18	12	13	15	15	13	10	9	8	7	14
B	21	22	12	12	24	21	12	16	17	18	16	19	21	20	22	21	12	12	13	15	16	16	16	12	12	21	21	21	21	21
C	13	13	21	12	11	21	21	11	11	11	13	14	19	9	9	9	8	7	11	12	13	15	18	18	18	17	18	19	11	12
D	14	14	21	12	11	21	21	11	14	14	15	16	14	13	15	16	18	17	12	18	18	12	12	15	15	16	17	18	19	20
E	15	15	12	12	17	21	21	10	11	12	11	9	9	8	7	6	6	6	5	4	6	7	8	9	11	12	11	12	7	6
F	16	16	12	10	13	12	21	10	15	16	17	17	14	15	15	16	14	13	12	14	15	15	16	16	17	14	13	13	12	11
G	11	17	13	12	16	14	19	11	18	19	19	20	5	17	21	20	20	21	22	13	18	19	19	19	21	21	21	22	22	20
H	21	12	17	15	18	16	21	11	17	18	17	18	17	18	18	18	17	18	17	18	18	17	18	18	17	19	17	18	18	
I	11	12	14	14	11	12	12	12	11	11	11	11	11	11	11	11	11	11	11	11	11	12	12	12	12	12	12	12	13	11
J	12	13	19	18	12	21	20	14	20	21	22	23	22	21	21	22	18	17	18	18	16	17	17	18	11	18	19	19	19	22
K	10	11	0	0	0	19	19	13	19	20	21	22	22	22	21	22	18	19	17	18	16	17	17	19	11	18	22	22	21	19
L	14	14	21	12	11	21	21	11	14	14	15	16	14	13	15	16	18	17	12	18	18	12	12	15	15	16	17	18	19	20
M	13	10	23	12	11	18	19	11	18	19	19	20	5	17	21	20	20	21	22	13	18	19	19	19	21	21	21	22	22	20
N	15	9	20	13	10	19	21	11	17	18	17	18	17	18	18	18	17	18	17	18	18	17	18	18	18	17	19	17	18	18
O	16	8	19	15	11	18	12	12	11	11	11	11	11	11	11	11	11	11	11	11	11	12	12	12	12	12	12	12	13	11

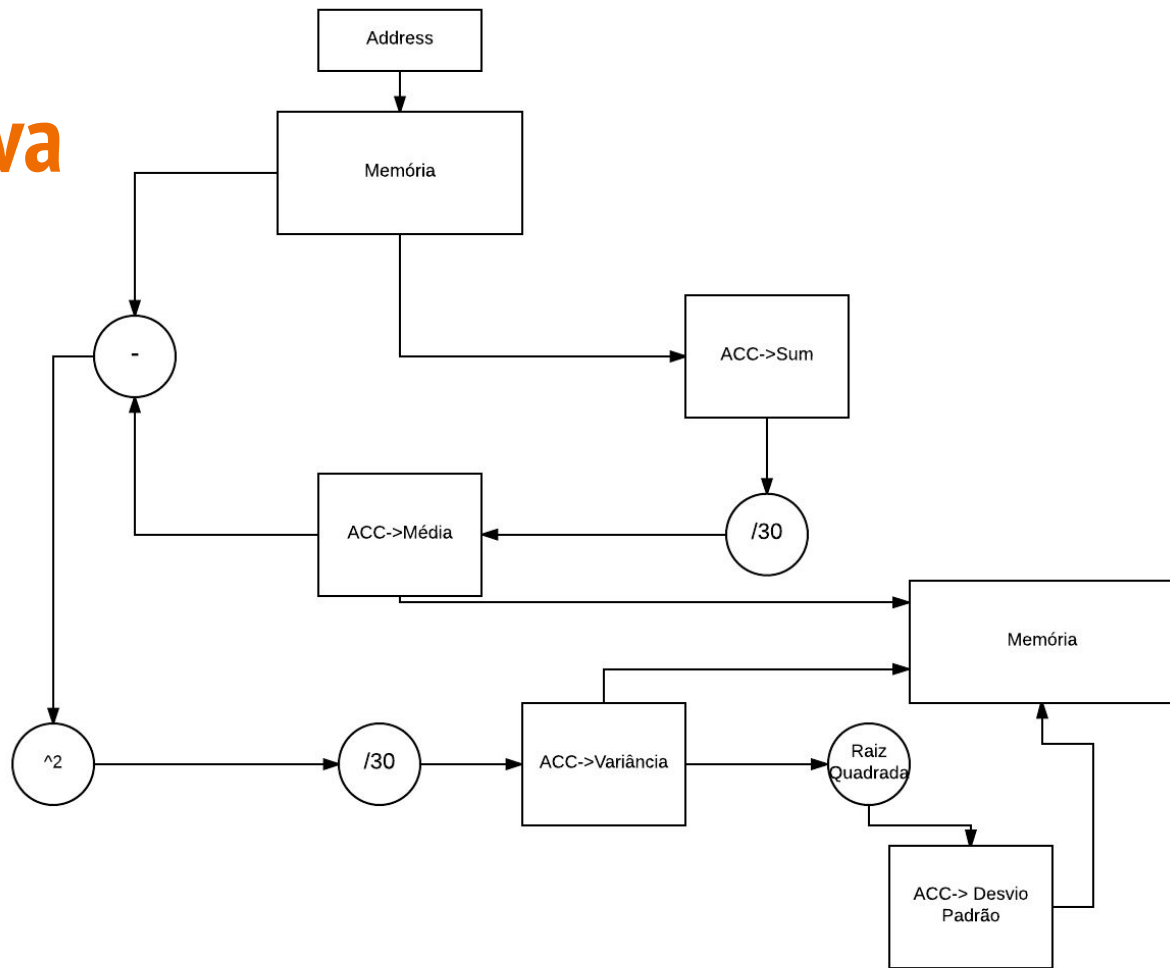Memória BRAM, tipo Single Port RAM

Largura: 5 bits (cada dia em uma posição)

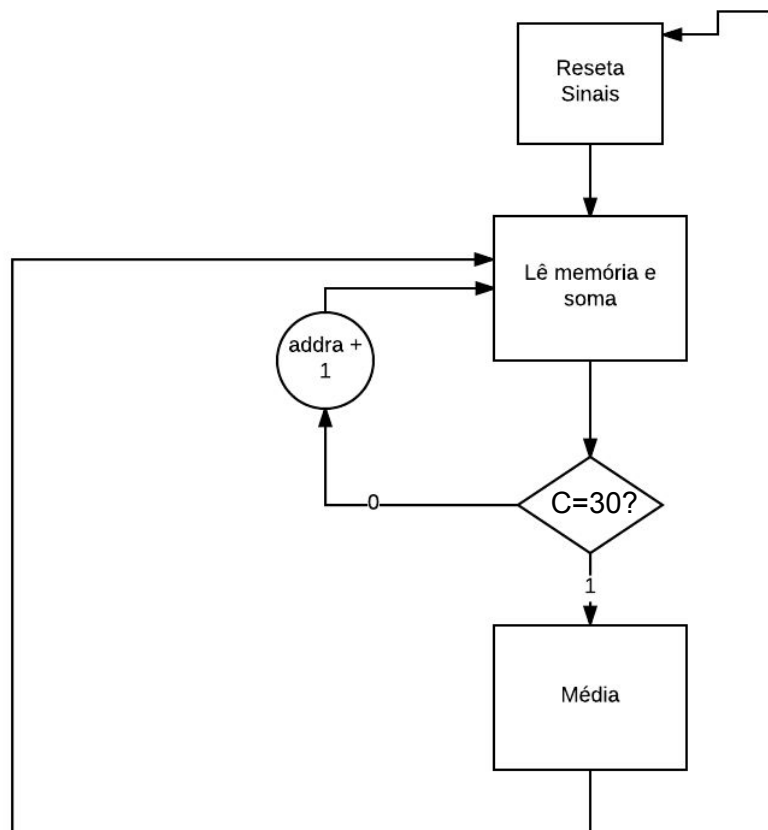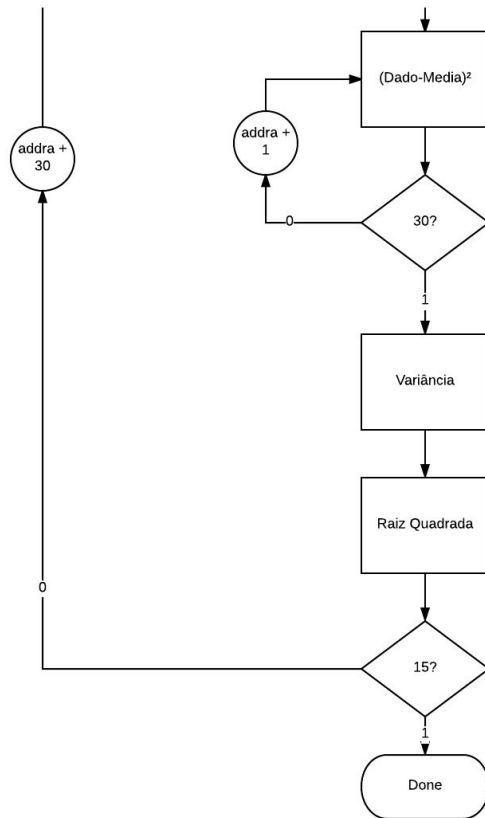Profundidade: 490 posições (450 dias + dados salvos)

Parte de Controle
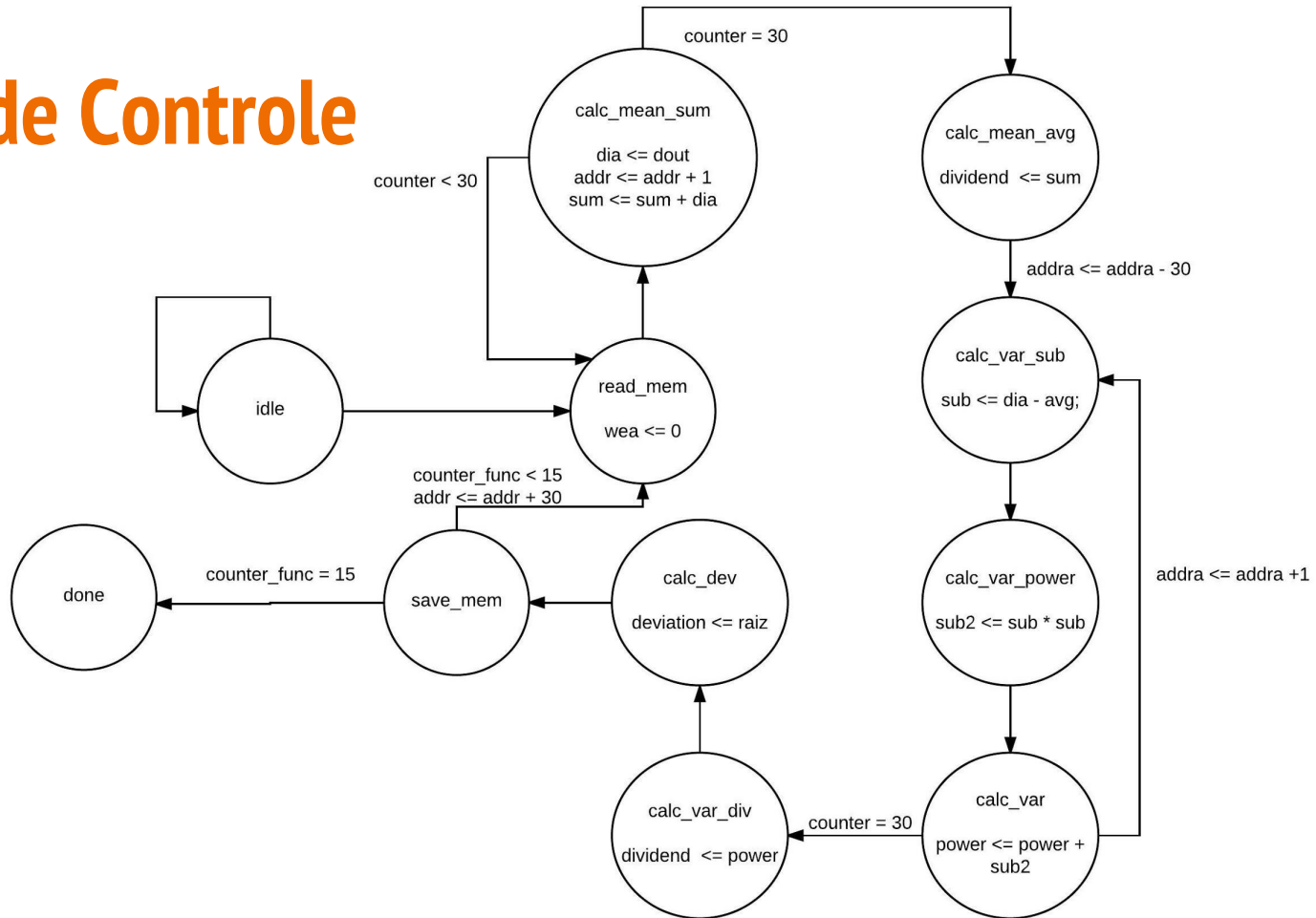
Parte Operativa

Fluxograma ASM
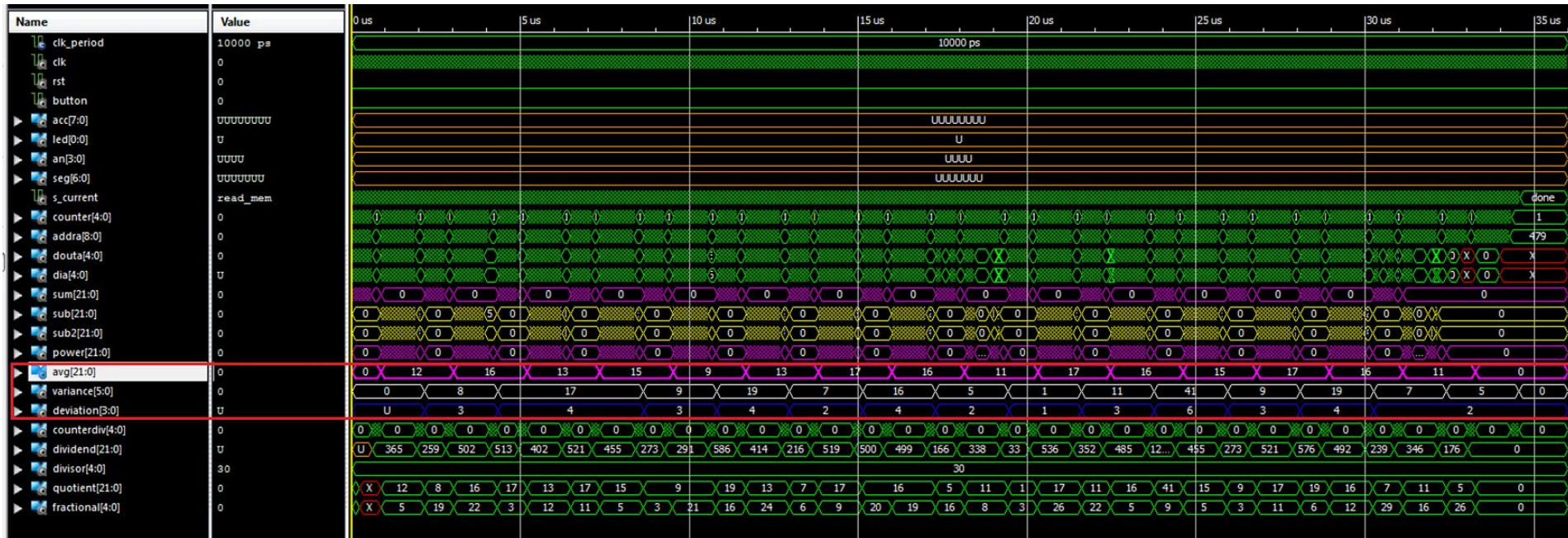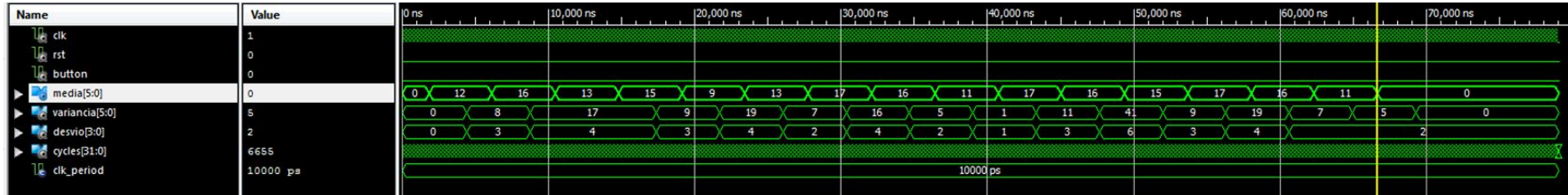
Fluxograma ASM

Simulação sem atraso

Simulação com atraso

Dados de Área

Device Utilization Summary					[-]
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**	
Number of Slice Flip Flops	1,008	1,920	52%		
Number of 4 input LUTs	434	1,920	22%		
Number of occupied Slices	708	960	73%		
Number of Slices containing only related logic	708	708	100%		
Number of Slices containing unrelated logic	0	708	0%		
Total Number of 4 input LUTs	485	1,920	25%		
Number used as logic	434				
Number used as a route-thru	51				
Number of bonded IOBs	50	83	60%		
Number of RAMB16s	1	4	25%		
Number of BUFGMUXs	1	24	4%		
Number of MULT18X18SIOs	1	4	25%		
Average Fanout of Non-Clock Nets	1.96				

Frequência Máxima

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Timing Summary:
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Speed Grade: -4

    Minimum period: 9.223ns (Maximum Frequency: 108.425MHz)
    Minimum input arrival time before clock: 5.224ns
    Maximum output required time after clock: 4.571ns
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Perguntas