GUNAVANT SETTY

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SUMMARY

Versatile and highly motivated Computer Engineering Graduate Student at NC State University studying to connect software to silicon. Looking for summer internships in Digital Design/Verification and Fabrication starting summer 2025. Ready to re-locate.

EDUCATION

North Carolina State University, Raleigh, NC **Aug 2024 - May 2026**
***Master of Science**, Computer Engineering*
Courses*: ASIC and FPGA Design with Verilog,* Architecture *of Parallel Computers, Microprocessor Architecture*

Jawaharlal Nehru Technological University Hyderabad, India **Nov 2020 – June 2024**
Bachelor of Technology, Electronics and Communication Engineering **GPA: 9.16/10**

SKILLS

Programming Languages: C, C++, Python, Verilog HDL, SystemVerilog, MATLAB
Technical Skills: IC Design Compiler and Synthesis, OOPS, Digital Electronics, Circuit Analysis and Design
Tools/Frameworks: Synopsys Design Compiler, Xilinx Vivado, Cadence Xcelium, PyCharm, EDA Playground, Questa
Certifications: SystemVerilog for Verification, Verilog HDL Fundamentals, PCAP OpenEDG Python Institute

PUBLICATIONS AND PROJECTS

VLSI Implementation of Transformer Scaled Dot-Product Attention Module for Advanced AI

- Designed a **hardware-accelerated** Scaled Dot-Product Attention module, a critical component of state-of-the-art Transformer models used in large language models and AI applications.
- Engineered complex matrix multiplication operations for matrices using SRAM-based data management, optimizing for **parallel processing** and efficient memory access.
- Developed a **synthesis-ready** SystemVerilog implementation featuring efficient control logic for DUT-testbench handshaking and pipelined SRAM operations, **utilizing scratchpad SRAM** for access to Q, K, V, and S matrices.

Floating Point Matrix Multiplication Module Design

- Designed and implemented a SystemVerilog module to perform matrix multiplication using **floating-point arithmetic**, interfacing with SRAM modules for data storage and retrieval.
- Demonstrated proficiency in SystemVerilog coding, including use of DesignWare components for efficient floating-point operations and implementation of control logic for test fixture handshaking.
- Validated design functionality via **Cadence Xcelium** simulation and synthesized the design using Synopsys Design Compiler, ensuring no major/minor synthesis errors, and optimizing for performance and area constraints.

Performance Analysis Of 64-bit Multipliers Using Area-efficient Carry-Select Adder

- Presented findings at the **3rd** International Conference on Power Electronics, Intelligent Control, and Energy Systems **(IEEE-ICPEICES-2024)** held in April 2024 at Delhi Technological University.
- Evaluated area-efficient adders, leading to the selection of an advanced carry-select adder, and implemented 64-bit Array and Vedic multipliers in Verilog HDL, achieving up to 23% performance improvement and 15% area reduction using the Virtuoso tool to optimize circuit efficiency.

Out-Of-Order Superscalar Processor Simulator

- Built an out-of-order superscalar RISC-V processor simulator using C++, enabling efficient fetching and issuing of multiple instructions per cycle to enhance parallelism and performance.
- Designed a robust Reorder Buffer (ROB) and Issue Queue, effectively mitigating RAW and WAW hazards while optimizing dynamic instruction execution.
- Conducted detailed performance analysis, fine-tuning IPC across different configurations of Issue Queue size, ROB size, and Superscalar Width to maximize processor efficiency.

Branch Predictors Simulator

- Developed a branch predictor simulator in C++ implementing bimodal, gshare, and hybrid prediction schemes, demonstrating strong computer architecture knowledge and programming skills.
- Implemented efficient data structures and algorithms to model complex branch prediction mechanisms, including 2-bit saturating counters and global history registers.
- Utilized a robust command-line argument parsing and flexible output formatting to meet rigorous project specifications, showcasing attention to detail and ability to follow precise requirements.

Python-Based Analysis of Depletion Region Slope in MOS Capacitors (*Link*)

- Engineered a Python-based MOS capacitor analysis tool, using $1/C^2$ vs. gate voltage data and interactive plotting for enhanced device behavior insights.
- Applied linear regression to analyze depletion region slopes, adjusting parameters to evaluate the impact of physical constants on MOS capacitor performance.