Spring 2015 Week 1 Module 6

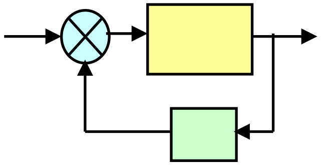
Digital Circuits and Systems

Introduction to Verilog

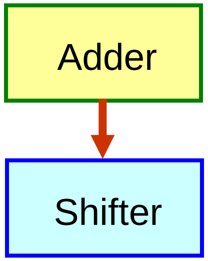
*Shankar Balachandran**
Associate Professor, CSE Department
Indian Institute of Technology Madras

*Currently a Visiting Professor at IIT Bombay

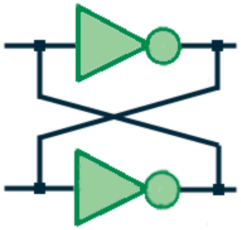
Abstraction Levels



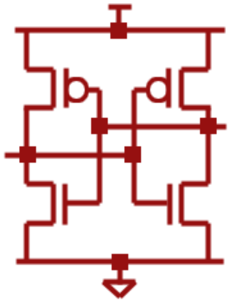
System Level



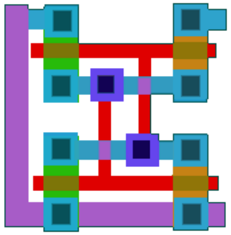
Architecture Level



Gate Level



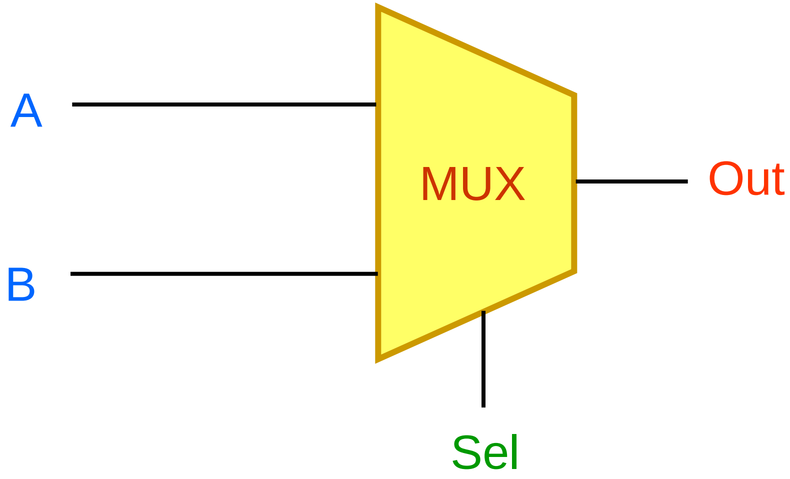
Transistor Level



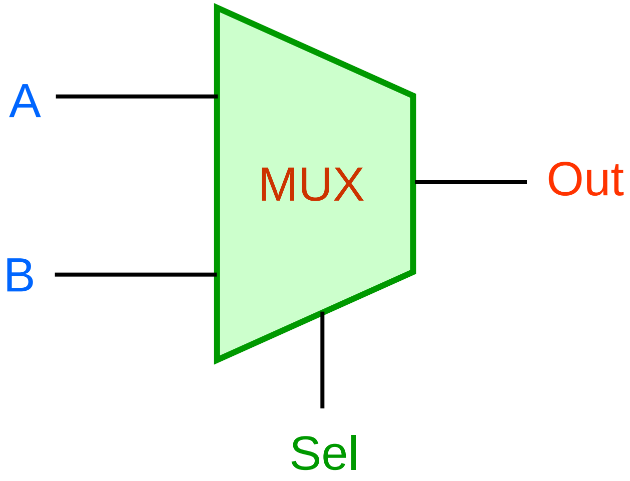
Silicon Level

Design Representation (Example 1)

- **Multiplexer**: Choose one of two inputs based on a control input
- **Sel**: Select line and is a control input
- **A,B**: Data Inputs
- **Out**: Multiplexer Output



Textual Description



- If ***Sel*** is \`0’, choose ***A*** and pass it on to ***Out***
- If ***Sel*** is \`1’, choose ***B*** and pass it on to ***Out***
- The value of ***A*** and ***B*** does not matter
  - Pass both 0’s and 1’s

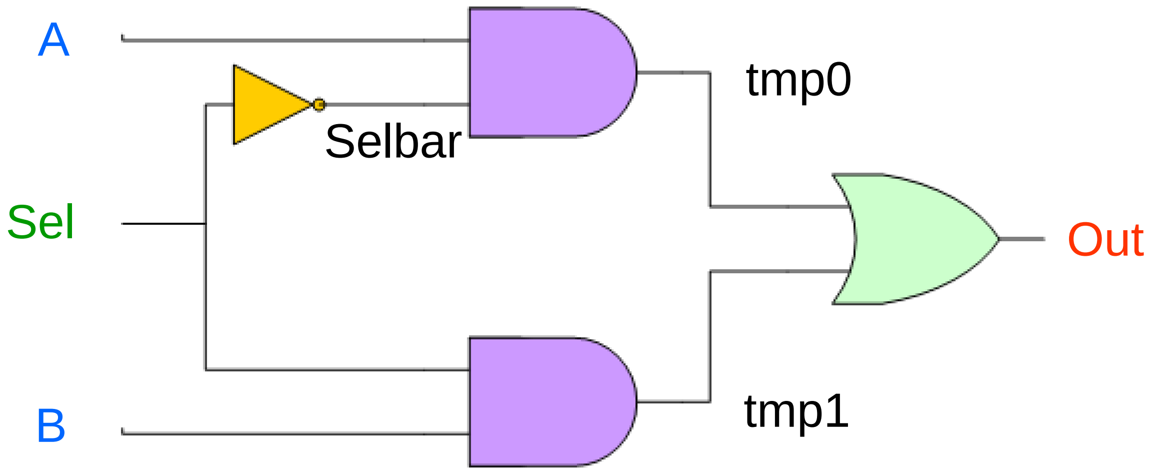
Truth Table

Sel	A	B	Out
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Boolean Equation

$$Out = \overline{Sel} \cdot A + Sel \cdot B$$

Gate Level Description

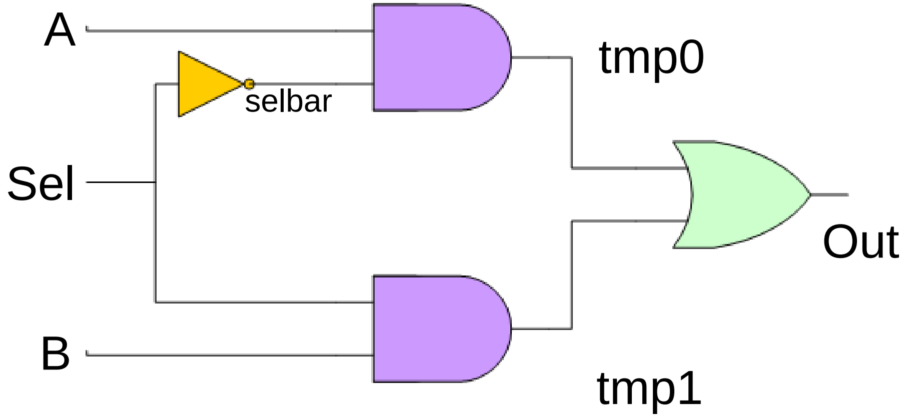


Verilog Description (Netlist)

```
module   multiplexer (A, B, Sel, Out);
    input      A, B, Sel;
    output   Out;
    wire       tmp1, tmp0;
    wire       selbar;

    and  (tmp1, B, Sel);
    not   (selbar, Sel);
    and  (tmp0, A, selbar);
    or     (out, tmp0, tmp1);

endmodule
```



What is Verilog?

- Verilog is a **Hardware Description Language (HDL)**
- **HDL:** A high level programming language used to model hardware.
- Hardware Description Languages
  - have special hardware related constructs.
  - currently model digital systems and limited analog, and in future can model complete mixed-signal systems also.
  - can be used to build models for simulation, synthesis and test.
  - have been extended to the system design level

Verilog Language

- Concurrent hardware description language
  - Naturally expresses parallelism in the hardware
- Has constructs in it for modeling delays
- Similarities in syntax to software languages

End of Week 1: Module 6

Thank You