Question 1

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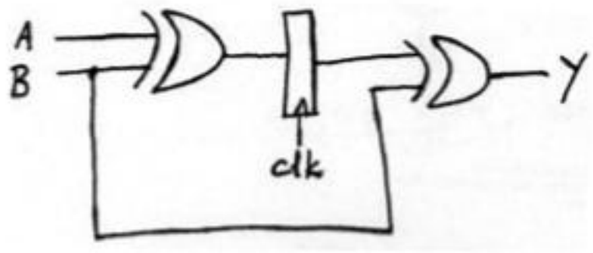
Write a Verilog module (at RTL level) that implements the below circuit.




```
module dflop(clk, d, Q);
 input clk, d;
 output reg Q;
 always @(posedge clk)
 Q<=d;
endmodule
module implementation (A, B, clk, Y);
 input  A, B, clk;
output reg Y;
wire d, Q;
XOR a1(d, A, B);
dflop d1(clk, d, Q);
XOR a2(Q, B, Y);
endmodule
```

Question 2

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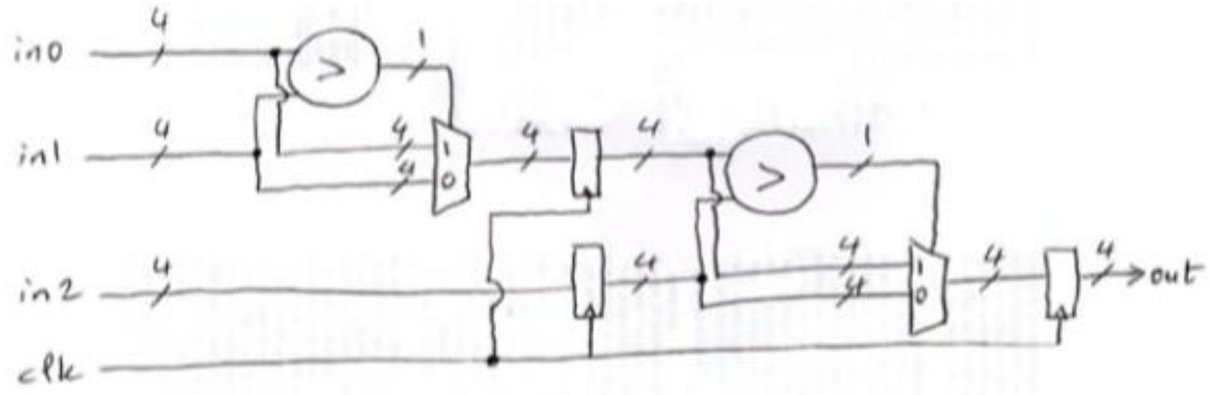
(a) Write down a synthesizable Verilog module that implements the below circuit. (b) What does this circuit do? (c) How many clock cycles does it take this circuit to its job? Can this circuit accept a new set of inputs every cycle? Why or why not?



A

```
module greater(in0, in1, in2, clk);
 input clk;
 input [3:0] in0, in1, in2;
 output reg [3:0];
 wire [3:0] p0, p1, p2, p3;

always @(posedge clk)
 begin
 p3<=(p1>p2)?p1:p2;
out<= p4;
p0<=(in0>in1)?in0;in1;
p1<=p0;
p2<=in3;
end endmodule
```

B

outputs are the greatest input

C

2 clock cycle, circuit can accept

Question 3

Not yet answered | Marked out of 20.00

Write a synthesizable Verilog code for a pipelined "product of 10 4-bit numbers". Assume that you are given multipliers and flops as many as you want. Build a binary tree of multipliers first, then pipeline it. How many multipliers do you need? How many flops do you need?

Question 4

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3 instructors are working together to grade test papers. The test contains 10 questions. Every instructor takes 2 minutes to grade each question. The instructors split the questions among them. For example, instructor 1 takes questions 1 and 2, instructor 2 takes 3, 4, 5, 6, instructor 3 takes 7, 8, 9, 10. They work with each other in a pipelined fashion.

(a) How should they split the questions among them (instead of the split given above) so that the throughput is the fastest and what is the throughput in that case in terms of test papers graded per hour?

(b) What is the latency in that case?

(c) What would be the latency and throughput if the split of questions was 1-2, 3-5, 6-10?

(d) How long would it take to grade 62 test papers?

A)

For a fast throughput they have to share amount of questions close to each other

3+3+4 or 2+4+4

4x2 min

Question 5

Not yet answered | Marked out of 14.00

Below the Verilog code for a bidirectional synchronous RAM with its controller is given. Based on this information, fill in the blanks.

```
module bidirdata_ram_sync #(          ADDR_WIDTH = 8,        DATA_WIDTH = 8) (

    input wire clk,

    input wire we,

    input wire [ADDR_WIDTH-1:0] addr,

                                [DATA_WIDTH-1:0] bi_data
    );

    reg [ADDR_WIDTH-1:0] addr_reg;

                [DATA_WIDTH-1:0] ram [2**           -1:0];

    assign              = (we) ? 8'hZZ: ram[addr_reg];

    always @(posedge clk) begin

        addr_reg <= addr;

        if (we)  // write operation

            ram[addr] <=          ;

        end

endmodule
```