Gunjan Bhargava

Seattle, WA **| Phone:** (+1) 425-894-0008**|**
Email: gunjanb2006@gmail.com | **GitHub:** https://github.com/gunjanb **|**
LinkedIn: https://www.linkedin.com/in/gunjan-bhargava/

Summary

Electronics and Telecommunication Engineer, worked as a Verification Engineer in VLSI Domain for 3 years. I took few years off to raise my child and now I am eager to return to work. Expanding my knowledge by attending the Full Stack Web Development program at University of Washington Seattle with the latest technologies for full stack web developers. Excellent ability to learn new technologies and work in collaborative environments.

Education and Certificates

- University of Washington Professional Certificate in Full Stack Web Development (Expected September 2021)
- Certificate in HTML5, CSS3 and Responsive Design for Web Development, *Web Forms, JavaScript, and Responsive Design*! (2016) from UW Professional and Continuing education. (2016)
- Certificate in C# Programming from UW Professional and Continuing education (2016)
- Masters in Opto-Electronics and Optical Communication from IIT – Delhi (9.25/10) (2009-2011)
- Bachelor of Engineering in Electronics and Telecommunication from RGPV India. (2002-2006) (University Merit Holder)

Technical Skills

- HTML5
- CSS3
- JavaScript
- jQuery
- React
- Bootstrap
- MySQL
- MySQL Workbench
- Robo 3T
- Node.js
- ES6
- Express
- Web APIS
- Third Party APIs
- JSON
- OOP
- Rest APIs
- Handlebars
- ORM Sequelize
- ORM Mongoose
- PayPal
- Bcrypt
- MVC
- Cloudinary
- Multer
- Responsive design
- UIkit
- Git, GitHub
- Heroku
- Insomnia
- JEST
- Inquirer
- Nodemon
- Express Session
- Dotenv
- ESLint
- Prettier
- Moment.js
- ModelSim
- ncSIMVISION
- Verilog,
- E-Specman
- Specman
- MongoDB

Work Experience

Full Stack Web Development (March 2021 -September 2021)

- Completed two Team projects, one focused on frontend development and third-party API calls (https://gunjanb.github.io/Kids-Corner-Learning-Tool/) other is focused on MVC approach and CRUD operations.(https://happylittleartgallery072021.herokuapp.com/) Git version control is used for integration.
- Front-End Design and Development for various assignments and group projects. Utilized UIkit and Bootstrap as CSS framework. Standardized layout with templates, specifically using Handlebars.
- Back-End Design and development for various assignments and group projects. Developed application through Node.js and NPM packages. Implemented web server using express. Used MongoDB and MySQL as Database.
- Used Jest for testing.

Engineer at eInfochips LTD (2011-2013)

1. **Team Lead - Verification of DC (Display Controller) IP -June 2012 to Jan 2013**
   - IP regression client's setup for different IPs.
   - Adding test case for new features.
   - Running the regressions for different IP versions.
   - Prepared presentations for different components in DC.
2. **Team Member - Verification of DC (Display Controller) as part of SOC - Nov 2011 to May 2012**
   - Involved in verification of DCIO, SANITY and MC STRESS categories which are part of DC SOC.
   - DCIO contains the controls for display related GPIO pads. In this category, mainly worked on hpd, dp aux, i2c, ddcvga and ddc interfaces.
   - MC (memory controller) STRESS category objective is to verify Display Controller and MC interfaces in close to real-life worst-case scenario in terms of MC bandwidth and data return latency for Display controller. Also made a test plan for this category

Project Engineer at Wipro Technologies (Sep 2006 to Feb 2008)

1. **Module Lead -Verification of CoreSPI and H2F Interrupt Controller- August 2007 to Feb 2008**
   - As part of this implementation project, I was responsible for complete integrated Test Management which consists of Development / execution / tracking of test cases.
2. **Team Member - Title: I2C Master Slave controller verification -April 2007 to June 2007**
   - I was responsible for Development and execution of test scenario / test cases for I2C Master Slave controller verification.
3. **I2C eVC & SPI eVC development -Nov 2006 to March 2007**
   - Developed the Data units, sequences, and driver of the I2C eVC. Various types of sequences have been made using the macro such as read, write etc. Developed the scoreboard module for the I2C eVC using the ram (sparse memory) model
   - Developed the arbitration logic to check whether DUT has lost the arbitration or not. Different scenarios are coded to check this feature.
   - Developed Master\Slave Agents, Scoreboard. Defined and developed testcases to check SPI