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ECE 6443 VLSI

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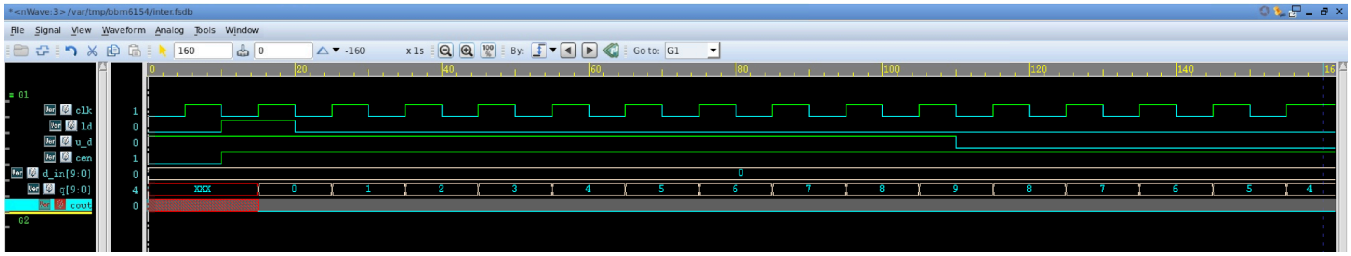
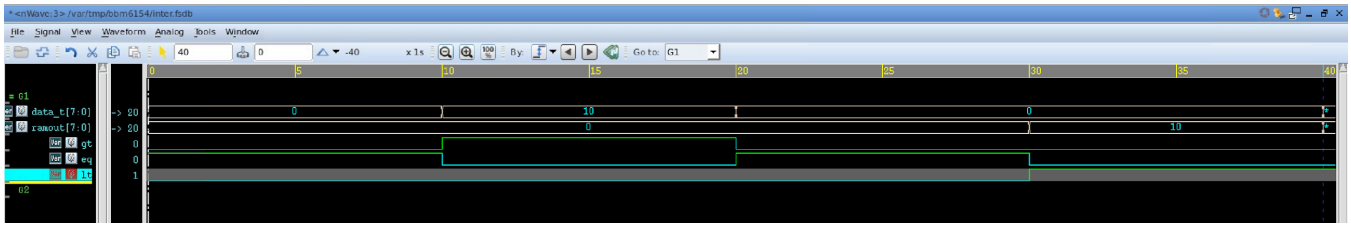
Edmund’s Submission

Simulations:

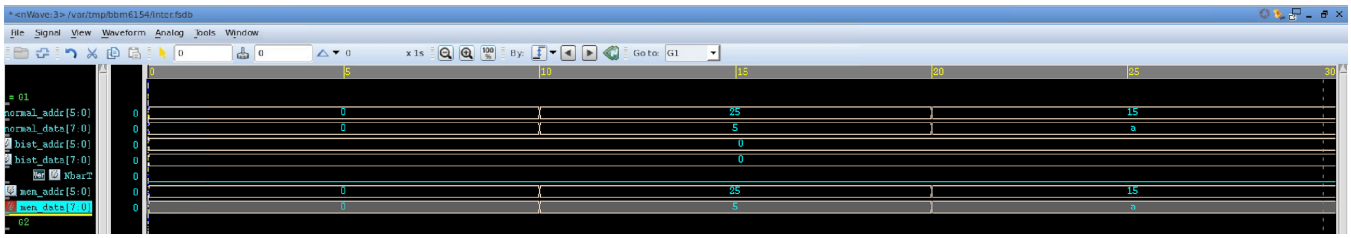
1. Counter: The waveform shows the counter incrementing on each clock cycle, with the count output increasing from 0 to 15 (4 bits). The counter resets to 0 when it reaches its maximum value.



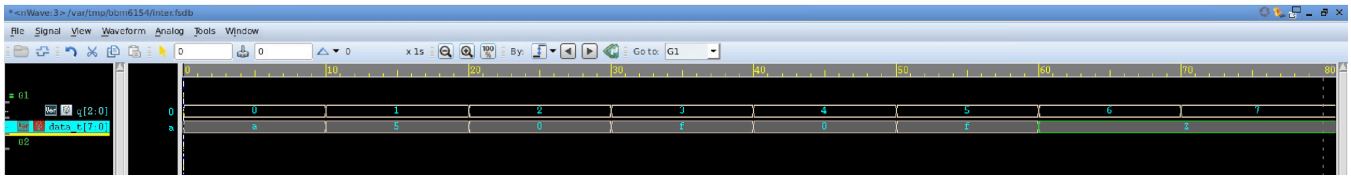

2. Comparator: The simulation verifies the comparator's functionality by showing the comp output going high when data_in matches data_out, indicating a match between the input and stored data.



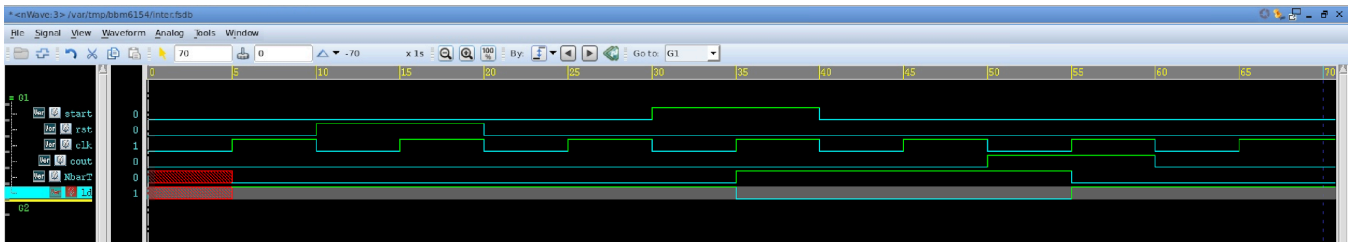
3. Multiplexer: The waveform demonstrates the multiplexer selecting between data inputs based on the sel signal. When sel is low, data0 is passed to dout, and when sel is high, data1 is passed to dout.



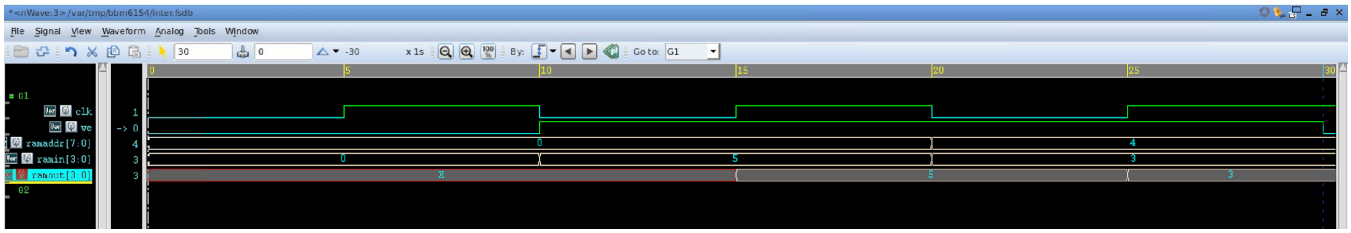
4. Decoder: The simulation shows the decoder converting a 2-bit binary input (addr) into a 4-bit one-hot output (word_line). Each address input corresponds to a unique word line being asserted high.



5. Controller: The waveform illustrates the controller's state transitions based on the current state and input signals. It generates appropriate control signals for BIST operations like write, read, and compare.



6. SRAM: The simulation verifies the SRAM's read and write operations. Data is written to the memory when write_en is high and read from the memory when read_en is high, with the data appearing on the dout port.



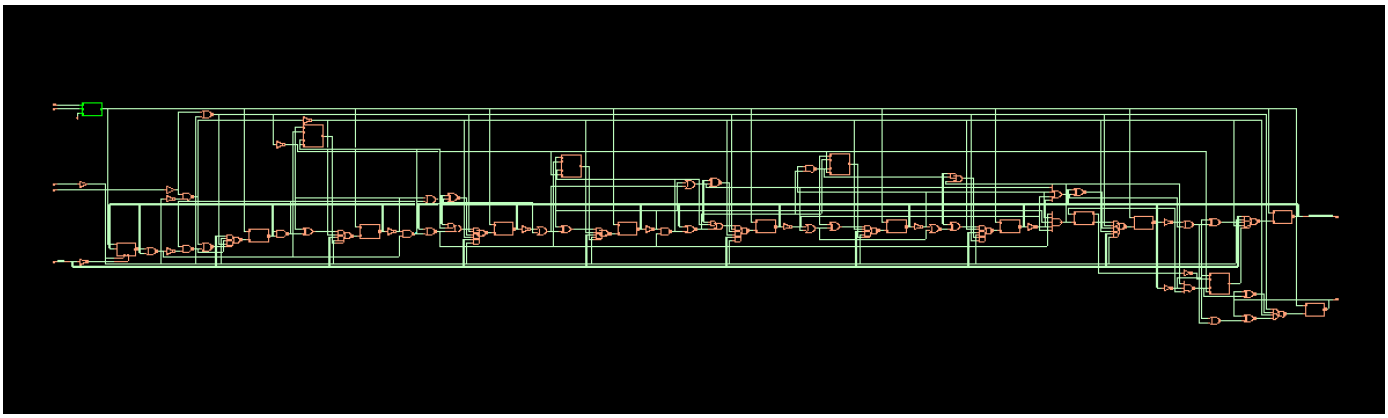
## Synthesis

1. **Counter: The synthesized counter schematic shows a 4-bit synchronous up-counter with a reset. The critical path is highlighted, indicating the longest delay path that limits the maximum operating frequency.**

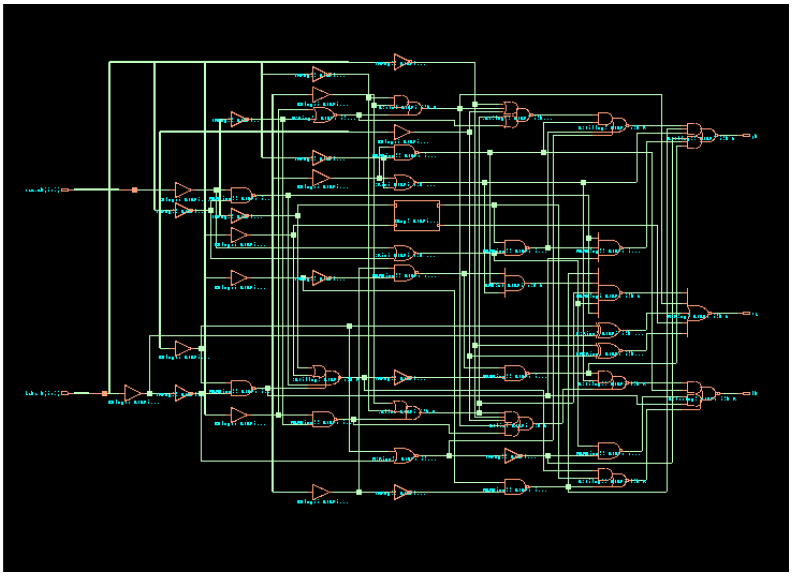
```
Path 1: VIOLATED (-129 ps) Setup Check with Pin cnt_reg_reg[10]/clk->d
         Group: clk
    Startpoint: (R) cnt_reg_reg[0]/clk
         Clock: (R) clk
      Endpoint: (R) cnt_reg_reg[10]/d
         Clock: (R) clk

                   Capture       Launch
       Clock Edge:+      50            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=      50            0

            Setup:-      17
    Required Time:=      33
     Launch Clock:-       0
        Data Path:-     162
            Slack:=    -129
```

```
File  Edit  View  Search  Terminal  Help
create_clock -period 1800.0 -name clk [get_ports clk]
set_input_delay 0.1 -clock clk [all_inputs]
set_output_delay 0.15 -clock clk [all_outputs]
set_load 0.1 [all_outputs]
set_max_fanout 1 [all_inputs]
set_fanout_load 8 [all_outputs]
set_clock_uncertainty .01 [all_clocks ]
set_clock_latency 0.01 -source [get_ports clk]
```

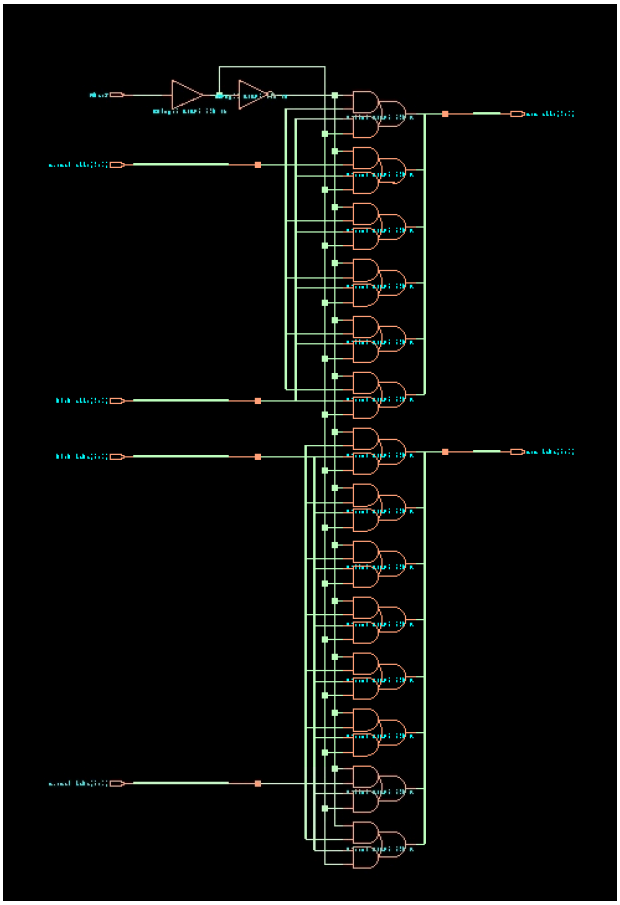
```
Path 1: MET (1 ps) Setup Check with Pin cnt_reg_reg[10]/clk->d
          Group: clk
     Startpoint: (R) cnt_reg_reg[0]/clk
          Clock: (R) clk
       Endpoint: (R) cnt_reg_reg[10]/d
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+     180            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=    180            0

             Setup:-     17
     Required Time:=    163
      Launch Clock:-      0
         Data Path:-    162
             Slack:=      1
```



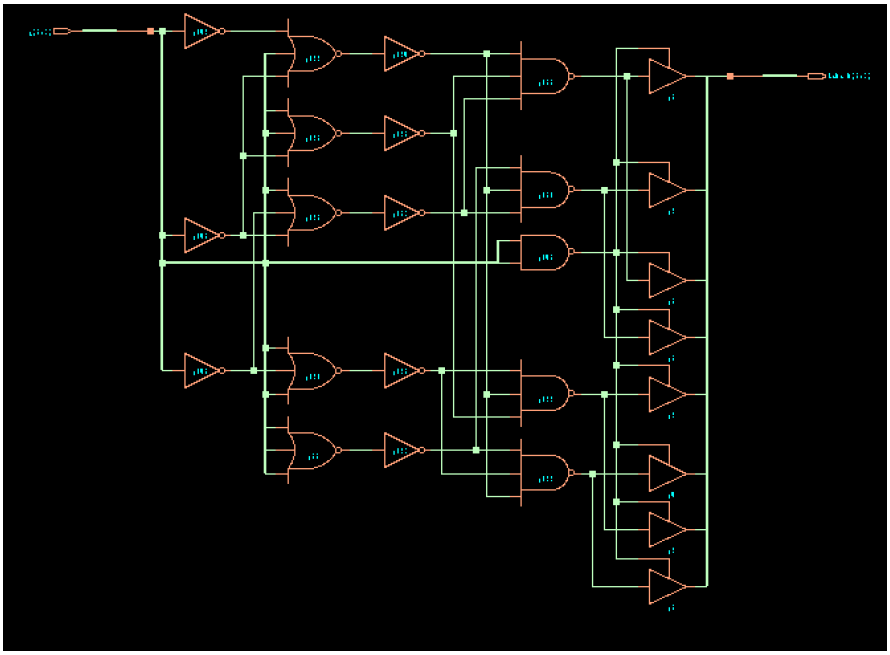
2. Comparator: The synthesized comparator circuit compares two 4-bit inputs (data_in and data_out) and generates a 1-bit output (comp) indicating whether the inputs match.



3. Multiplexer: The synthesized multiplexer schematic shows a 2-to-1 multiplexer that selects between two 4-bit data inputs (data0 and data1) based on a select signal (sel), producing a 4-bit output (dout).



4. Decoder: The synthesized decoder circuit converts a 2-bit address input (addr) into a 4-bit one-hot output (word_line), enabling the selection of a specific word line in the SRAM.

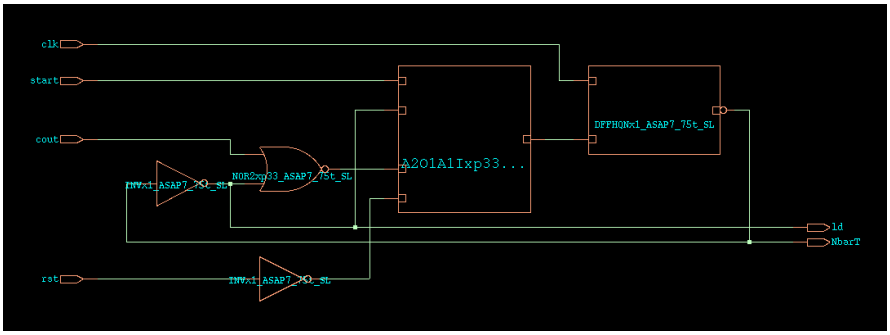


5. Controller: The synthesized controller schematic shows a finite state machine that generates control signals for BIST operations based on the current state and input signals. The critical path is highlighted.

```
Path 1: VIOLATED (-48 ps) Setup Check with Pin current_reg[0]/clk->d
          Group: clk
     Startpoint: (R) current_reg[1]/clk
          Clock: (R) clk
       Endpoint: (R) current_reg[0]/d
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+      50            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=      50            0

             Setup:-      17
     Required Time:=      33
      Launch Clock:-       0
         Data Path:-      81
             Slack:=     -48
```

```
File  Edit  View  Search  Terminal  Help
create_clock -period 100.0 -name clk [get_ports clk]
set_input_delay 0.1 -clock clk [all_inputs]
set_output_delay 0.15 -clock clk [all_outputs]
set_load 0.1 [all_outputs]
set_max_fanout 1 [all_inputs]
set_fanout_load 8 [all_outputs]
set_clock_uncertainty .01 [all_clocks ]
set_clock_latency 0.01 -source [get_ports clk]
```

```
Path 1: MET (2 ps) Setup Check with Pin current_reg[0]/clk->d
          Group: clk
     Startpoint: (R) current_reg[1]/clk
          Clock: (R) clk
       Endpoint: (R) current_reg[0]/d
          Clock: (R) clk

                    Capture       Launch
       Clock Edge:+     100            0
       Src Latency:+      0            0
       Net Latency:+      0 (I)        0 (I)
           Arrival:=    100            0

             Setup:-     17
     Required Time:=     83
      Launch Clock:-      0
         Data Path:-     81
             Slack:=      2
```




6. SRAM: The synthesized SRAM schematic shows the memory array, address decoder, and read/write circuitry. The critical path is highlighted, indicating the longest delay path that determines the maximum operating frequency. Timing constraints are met after resolving setup and hold violations.

```
Path 1: VIOLATED (-66 ps) Late External Delay Assertion at pin ramout[0]
          Group: clk
     Startpoint: (R) addr_reg_reg[0]/clk
          Clock: (R) clk
       Endpoint: (R) ramout[0]
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+      50            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=      50            0

      Output Delay:-       0
     Required Time:=      50
      Launch Clock:-       0
         Data Path:-     115
             Slack:=     -66
```

```
File  Edit  View  Search  Terminal  Help
create_clock -period 120.0 -name clk [get_ports clk]
set_input_delay 0.1 -clock clk [all_inputs]
set_output_delay 0.15 -clock clk [all_outputs]
set_load 0.1 [all_outputs]
set_max_fanout 1 [all_inputs]
set_fanout_load 8 [all_outputs]
set_clock_uncertainty .01 [all_clocks ]
set_clock_latency 0.01 -source [get_ports clk]
```

```
Path 1: MET (4 ps) Late External Delay Assertion at pin ramout[0]
          Group: clk
     Startpoint: (R) addr_reg_reg[0]/clk
          Clock: (R) clk
       Endpoint: (R) ramout[0]
          Clock: (R) clk

                     Capture       Launch
        Clock Edge:+     120            0
       Src Latency:+       0            0
       Net Latency:+       0 (I)        0 (I)
           Arrival:=     120            0

      Output Delay:-       0
     Required Time:=     120
      Launch Clock:-       0
         Data Path:-     115
             Slack:=       4
```