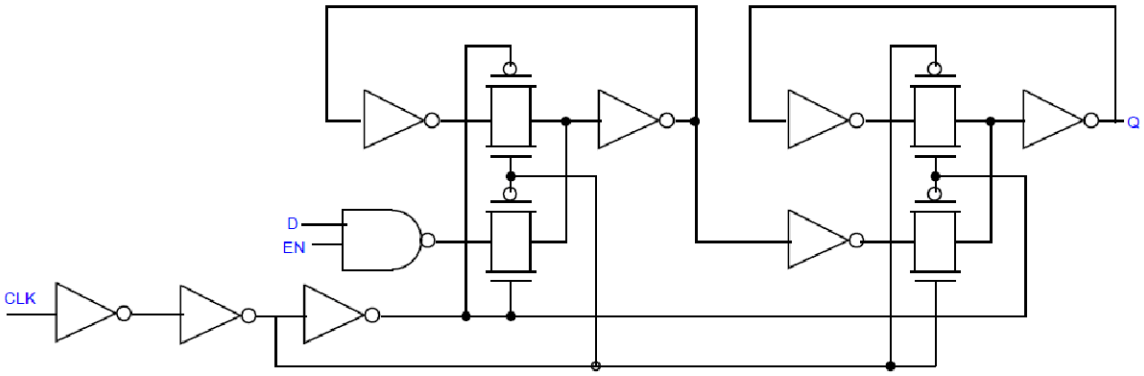
1. The components of the flip-flop below have the following rise/fall delays (in picoseconds).

Nand gate: 75/125
Transmission gate: 75/75
Inverter: 50/50

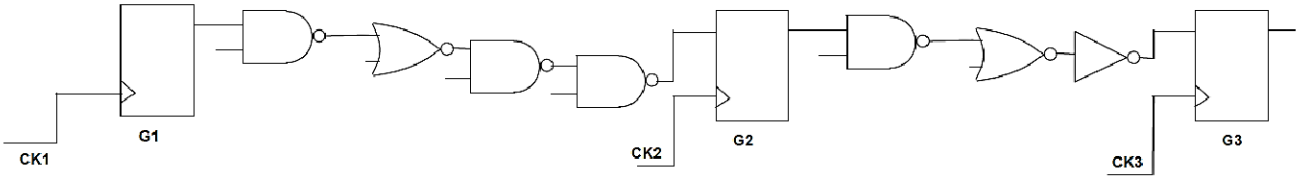
What are the values of the following flip-flop parameters:

(i) Setup time (ii) Hold time (iii) CLK-Q Delay

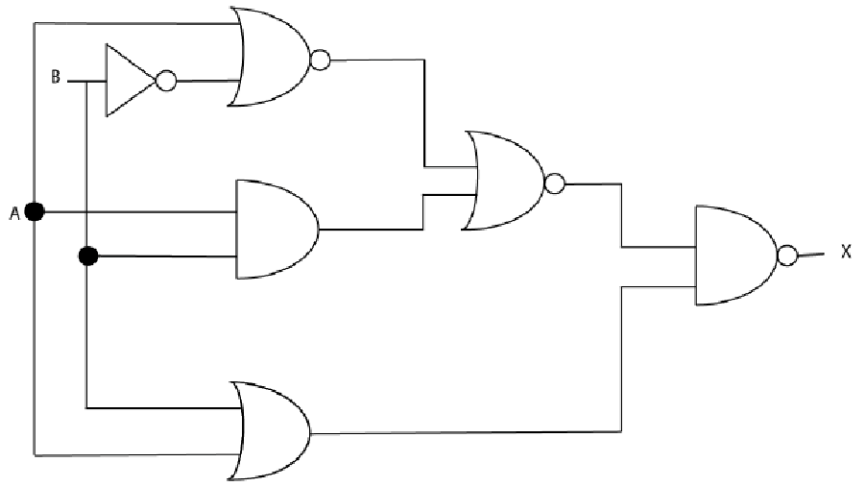


2. A part of a pipelined circuit is shown below. The CLK input to the 3 Flip-Flops are CK1, CK2 and CK3. (i) What is the maximum CLK frequency of this circuit if CK1, CK2 and CK3 are all connected to CLK? (ii) Is this result different if the skew b/w CK1 and CK2 = ±20ps and the skew b/w CK2 and CK3 is ±60ps ?

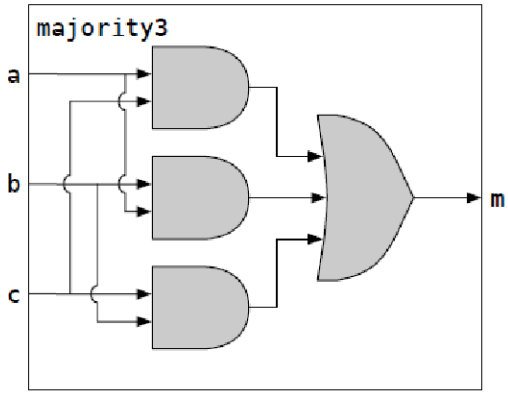
Setup time	50 ps
Hold time	45 ps
Clock-to-q delay	40 ps (min), 60 ps (max)
Propagation delay per gate	80 ps (min), 100 ps (max)

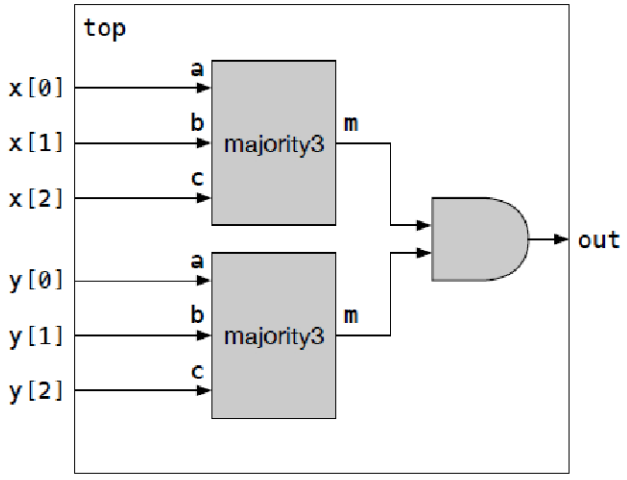


3. For the logic circuit shown below, write the equivalent behavioral Verilog module which takes A and B as inputs, and gives X as output.



4. write the Verilog module which implement the circuit drawn below.





5. In the N-tree dynamic gate shown below, assume B=1 and A=0 during precharge (node x gets charged to VDD and during the evaluate phase of the clock, B→0 followed by A→ 1. What voltages do nodes x, y and z settle to during the evaluate phase given the node capacitances for x, y and z?