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ECE 6913 CSA
HW 7
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NYU Tandon School of Engineering

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(Extra Credit) Homework Assignment 7

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Course Assistant Office Hour Schedule

(On Zoom) Monday, Tuesday & Thursday 9:30 - 10:30 AM,

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Homework Assignment 7 [released Thursday May 2nd 2024] [due Tuesday May 7th by 11:59PM]

You *are allowed* to discuss HW assignments with anyone. You are *not allowed* to share your solutions with other colleagues in the class. Please feel free to reach out to the Course Assistants or the Instructor during office hours or by appointment if you need any help with the HW. Please enter your responses in this Word document after you download it from NYU Classes. *Please use the Brightspace portal to upload your completed HW.*

- Please use the online 32-bit RISC V simulator:

https://www.kvakil.me/venus/
or
https://www.cs.cornell.edu/courses/cs3410/2019sp/riscv/interpreter/

- Please write the RISC V code, run it online to test/debug, demonstrate it works, include your code in the PDF you upload – as text not as an image

- Your code is graded for (1) validity (it works) (2) size (fewer lines, higher grades) (3) discussion explaining choices you made and why

• You cannot use/copy parts of or all of anyone else's code

1. Write a RISC V program using instructions in the RISC V ISA to calculate the sum of the squares of all odd numbers between 0 and +N where N is an integer < 100

SEE 1.asm

2. Write a RISC V program using instructions in the RISC V ISA to calculate the factorial of any positive integer N < 10

SEE 2.asm

3. Write a RISC V program using instructions in the RISC V ISA to calculate the sum of all prime numbers less than a given integer N where N < 100

SEE 3.asm

4. Write a RISC V program that calculates the sum of N terms in a geometric series where a = 1 and r = -3

SEE 4.asm

5. Write a RISC V program that calculates the sum of N terms in a arithmetic series where a0 = 1 and d = 3

SEE 5.asm

Part II

1. Please read the ISSCC 2014 Keynote Publication by Professor Mark Horowitz *"Computing's Energy Problem (and what we can do about it)"* [1]

1.1 How does Technology Scaling decrease the cost of Computing? How do reductions in the cost of manufacturing a transistor enable widespread use of computing devices?

Answer:

Technology scaling, particularly guided by Moore's Law, has historically enabled the reduction of the cost of computing primarily through the miniaturization of transistor size. This miniaturization means more transistors can be placed on a chip of the same size, effectively decreasing the cost per transistor and thus the cost of computing power. The decrease in cost makes computing devices more affordable and thus more accessible, leading to their widespread use. This economic accessibility has been instrumental in the proliferation of computing devices across various sectors of society, enhancing productivity and connectivity.

1.2 Why did scaling processor clock frequency become more difficult in the last 15 years? How did Power dissipation become the primary constraint on server CPU performance?

Answer:

Scaling processor clock frequency became more difficult due to physical limitations, such as heat dissipation and energy inefficiency. As frequencies increase, power consumption, which rises with the square of the voltage, also increases, leading to more heat generation. This issue of power dissipation, particularly in dense server environments, became a primary constraint because managing the thermal output of processors limits the feasible clock speeds and the number of cores that can be effectively utilized without causing overheating or requiring excessive cooling solutions.

1.3 Why is Moore's Law slowing down? Why did Dennard Scaling end?

Answer:

Moore's Law is slowing down due to physical and economic limits in further miniaturizing transistors on a chip. The sizes have reached near-atomic levels, where quantum effects and other physical phenomena make further size reductions impractical, unsafe, or too costly. Dennard Scaling, which posited that as transistors get smaller their power density stays constant, ended because voltage scaling could not keep pace with size reduction without causing increases in leakage currents and power density, making chips unmanageably hot and unreliable at smaller sizes.

1.4 Why is the energy consumption by Memory substantial ?

Answer:

Energy consumption by memory is substantial because modern computing tasks often involve significant data access and manipulation, which requires frequent read/write operations to memory. Memory operations consume power not just in the data access itself but also in the maintenance of the memory state and data integrity over time. As computing devices handle larger data sets and strive for faster access times, the power required to operate memory efficiently becomes a larger fraction of the total system power.

1.5 What solutions to Computing's Energy Problem does Professor Mark Horowitz's envision?

Answer:

Professor Mark Horowitz suggests several solutions to computing's energy problem, focusing on improving energy efficiency through architectural innovations rather than relying solely on advances in semiconductor technology. These include the development of specialized hardware (like ASICs) for specific tasks, which can offer better performance for less power compared to general-purpose processors. He also highlights the importance of optimizing software and hardware together to maximize energy efficiency, suggesting that future advances will likely come from smarter system-level designs that better integrate components and software.

2. This assignment requires you to review several references on RISCV beginning with a summary transcript [2] of the Debate on Proprietary Vs Open Source Instruction Sets at the 4th Workshop on Computer Architecture Research Directions, June 2015 sponsored by the ACM.

This Debate between Professor David Patterson (author of the textbook you are using) and Dave Christie of AMD highlights all of the key technical and business arguments for and against an Open-Source ISA such as RISC V as of 2015 (the same year the RISC V Foundation was established). A Technical Report from EECS UC Berkeley highlights the technical reasons for Open ISAs [3] providing a more detailed discussion on the advantages offered by open source ISAs

(1) Articulate *your* views on the topics debated in [2]. Justify your views.

Essentially the debate focuses on whether the openness that benefited software can also accelerate hardware innovation. Dave Christie of AMD argues for proprietary ISAs citing the success of commercial ISAs due to their ecosystems and the economic and technical support they provide. David Patterson advocates for open-source ISAs, arguing that they foster greater innovation, lower costs, and democratize access to technology development.

As someone who is trying to make 6G hardware i am a firm believer that open source hardware is the way to go. I'll be covering the following areas to back my beliefs. Innovation and Accessibility,

1. Innovation and Accessibility:
    a. Open-source ISAs can significantly lower the barrier to entry for new companies and academic institutions, fostering a more diverse ecosystem of hardware innovation. This openness can lead to faster innovation cycles, similar to how open-source software has accelerated software development.
2. Economic Impact:
    a. By reducing the licensing costs and eliminating the proprietary control of ISAs, smaller players can compete more effectively, potentially driving down costs and increasing the variety of specialized hardware solutions.
3. Longevity and Security:
    a. Open-source ISAs can provide longevity to hardware platforms that proprietary companies might no longer support. They also allow for greater scrutiny, potentially increasing security through community engagement in identifying and fixing vulnerabilities.

I can understand the argument for keeping hardware proprietary because if you made something it's yours, sure I get that. But why not share that gift with everyone especially when it can snowball into global change for the better. And in my honest opinion if you can come up wth of that caliber once who's to say you can't come up with more.

(2) Review and summarize technical reasons for Open-Source ISAs in [3].

Based on the technical support we will be covering the following subjects before we go on to the summary. Cost and Flexibility, Innovation through Accessibility, Avoiding Monopoly Constraints, Standardization Across Devices, Community Verification and Security.

1. Cost and Flexibility:
    a. Open-source ISAs reduce the cost of designing processors and allow for greater flexibility in customization. This is particularly beneficial for academia and small companies that cannot afford pricey ISA licenses.
2. Innovation through Accessibility:
    a. By making the ISA open, a broader community of developers can contribute to its development, speeding up innovation and adaptation in various computing sectors.
3. Avoiding Monopoly Constraints:
    a. Open-source ISAs prevent any single company from monopolizing the ISA, which can stifle innovation and lead to higher costs.
4. Standardization Across Devices:
    a. An open ISA like RISC-V can be used across multiple platforms, from embedded devices to servers, simplifying development and supporting a unified approach to computing across different hardware.
5. Community Verification and Security:
    a. The community can continuously verify and enhance the security features of the ISA, unlike proprietary ISAs where security verification is limited to the ISA owner.

To summarize, the shift towards open-source ISAs like RISC-V could significantly impact the semiconductor industry by democratizing access to chip design, much as open-source software has done for software development. The change might lead to more innovative and customized computing solutions, especially as demands for computing continue to diversify.

References

[1] M Horowitz, *"Computing's Energy Problem (and what we can do about it)"* Plenary Session 1.1, 2014 ISSCC Digest of Tech. papers, Feb 2014 [*PDF attached*]

[2] M Hill et al, "Proprietary Versus Open Instruction Sets" 4th Workshop on Computer Architecture Research Directions, June 2015, ACM [*PDF attached*]

[3] K Asanovic et al, "Instruction Sets Should Be Free: The Case For RISC-V", EECS, University of

California Berkeley, Technical Report No. UCB/EECS-2014-146, Aug 6 2014 [*PDF attached*]