ASSIGNMENT - 4

DIGITAL SYSTEMS ES204

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ARRAY MULTIPLIER

PART - 1

8-bit **Array Multiplier**

VERILOG CODE

```
module Arrmul(A, B, P);

parameter N = 4;
input [N - 1 : 0] A, B;
output reg [2 * N - 1 : 0] P;
integer i, j;
    always @* begin
        P = 0;
        for (i = 0; i < N; i = i + 1) begin : outer_loop
            for (j = 0; j < N; j = j + 1) begin : inner_loop
                P = P + ((A[i] & B[j]) << (i + j));
            end
        end
    end
```

```
endmodule
```

TESTBENCH

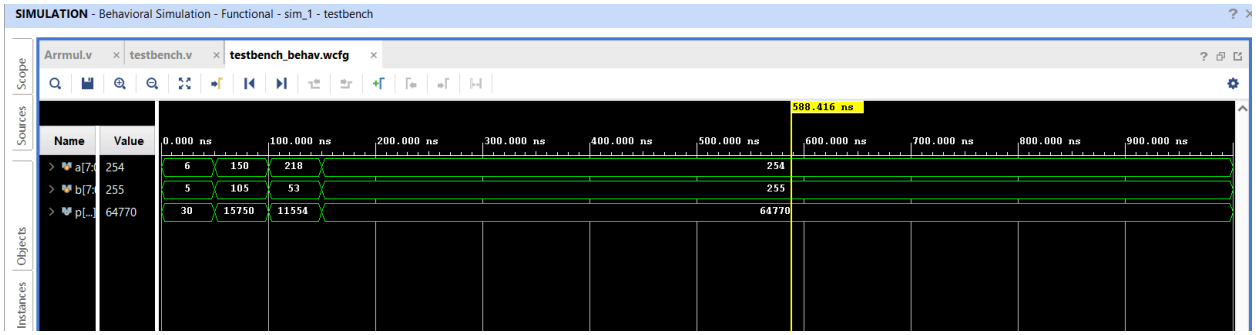
```
module testbench;

reg [7 : 0] a, b;
wire [15 : 0] p;

Arrmul obj(.A(a), .B(b), .P(p));

initial begin
//    $monitor($time, " A = %d (%b), B = %d (%b), P = %d (%b)",
a, a, b, b, p, p);
    a = 8'b00000110; b = 8'b00000101;
     #50 a = 8'b10010110; b = 8'b01101001;
     #50 a = 8'b11011010; b = 8'b00110101;
    #50 a = 8'b11111110; b = 8'b11111111;
//    #5 $finish;
end

endmodule
```

CONSTRAINT FILE

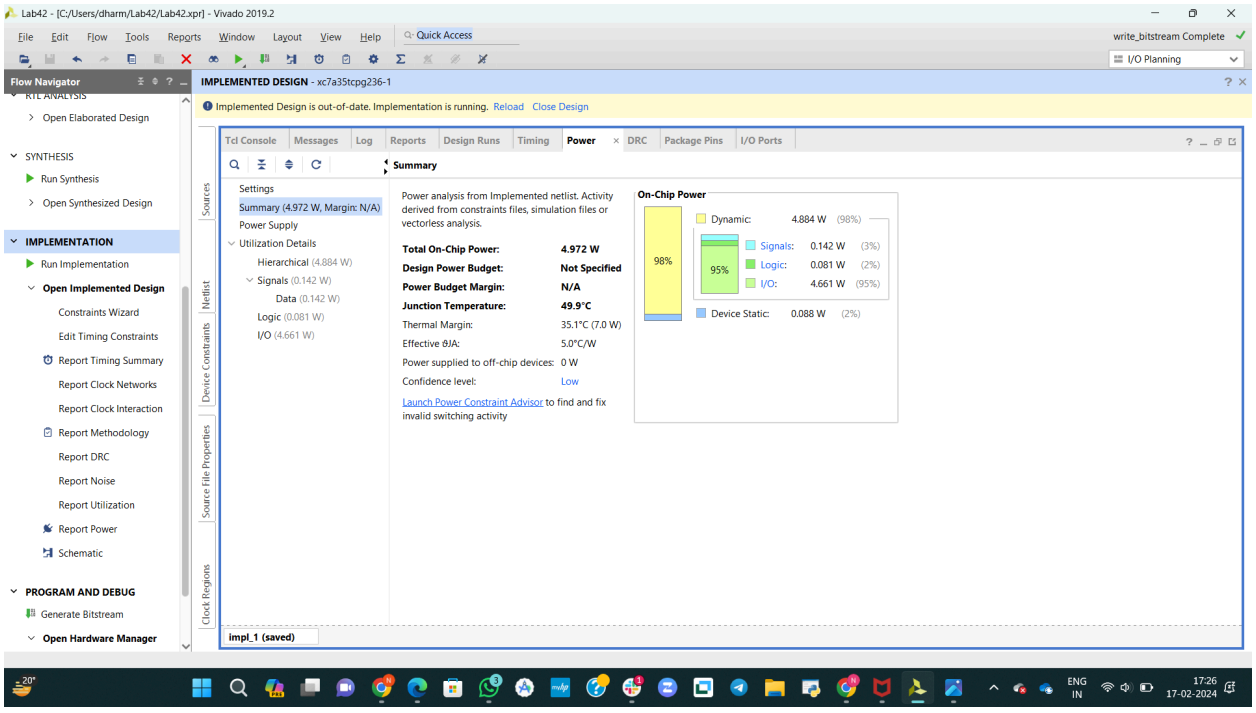
```
set_property IOSTANDARD LVCMOS33 [get_ports {A[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {A[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {B[0]}]
```

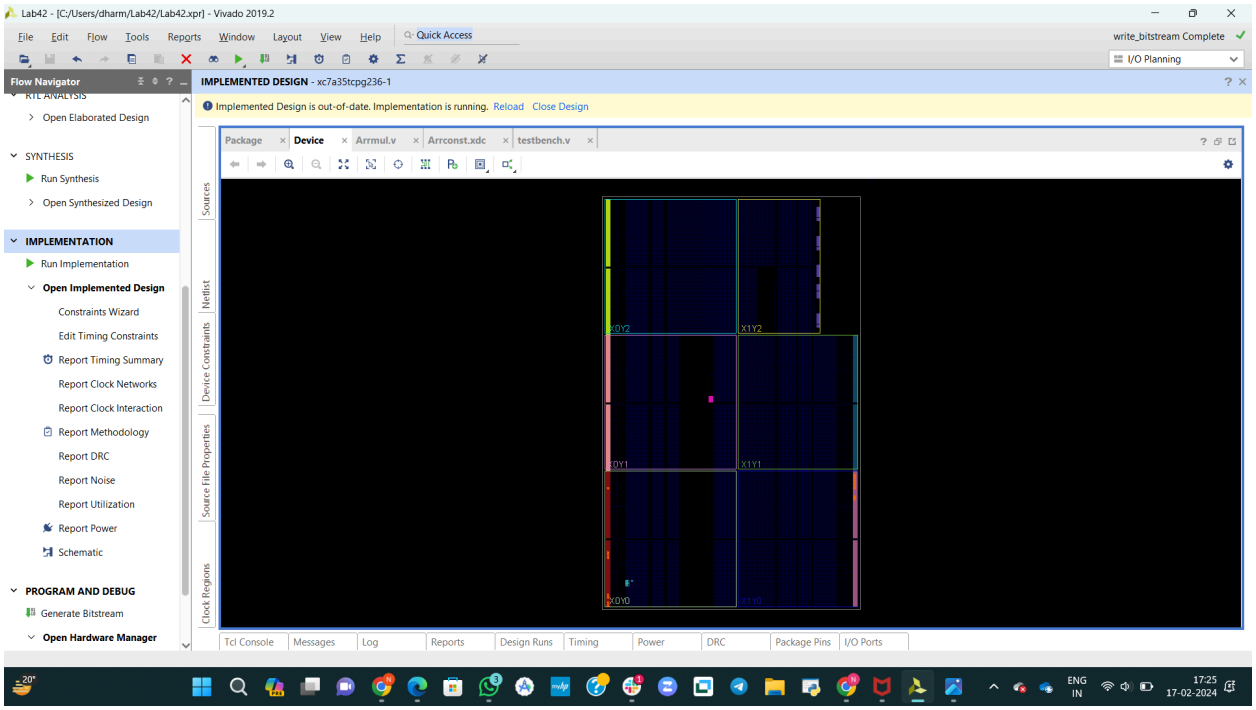
```
set_property IOSTANDARD LVCMOS33 [get_ports {P[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[0]}]
set_property PACKAGE_PIN R2 [get_ports {A[3]}]
set_property PACKAGE_PIN T1 [get_ports {A[2]}]
set_property PACKAGE_PIN U1 [get_ports {A[1]}]
set_property PACKAGE_PIN W2 [get_ports {A[0]}]
set_property PACKAGE_PIN R3 [get_ports {B[3]}]
set_property PACKAGE_PIN T2 [get_ports {B[2]}]
set_property PACKAGE_PIN T3 [get_ports {B[1]}]
set_property PACKAGE_PIN V2 [get_ports {B[0]}]
set_property PACKAGE_PIN V14 [get_ports {P[7]}]
set_property PACKAGE_PIN U14 [get_ports {P[6]}]
set_property PACKAGE_PIN U15 [get_ports {P[5]}]
set_property PACKAGE_PIN W18 [get_ports {P[4]}]
set_property PACKAGE_PIN V19 [get_ports {P[3]}]
set_property PACKAGE_PIN U19 [get_ports {P[2]}]
set_property PACKAGE_PIN E19 [get_ports {P[1]}]
set_property PACKAGE_PIN U16 [get_ports {P[0]}]
```

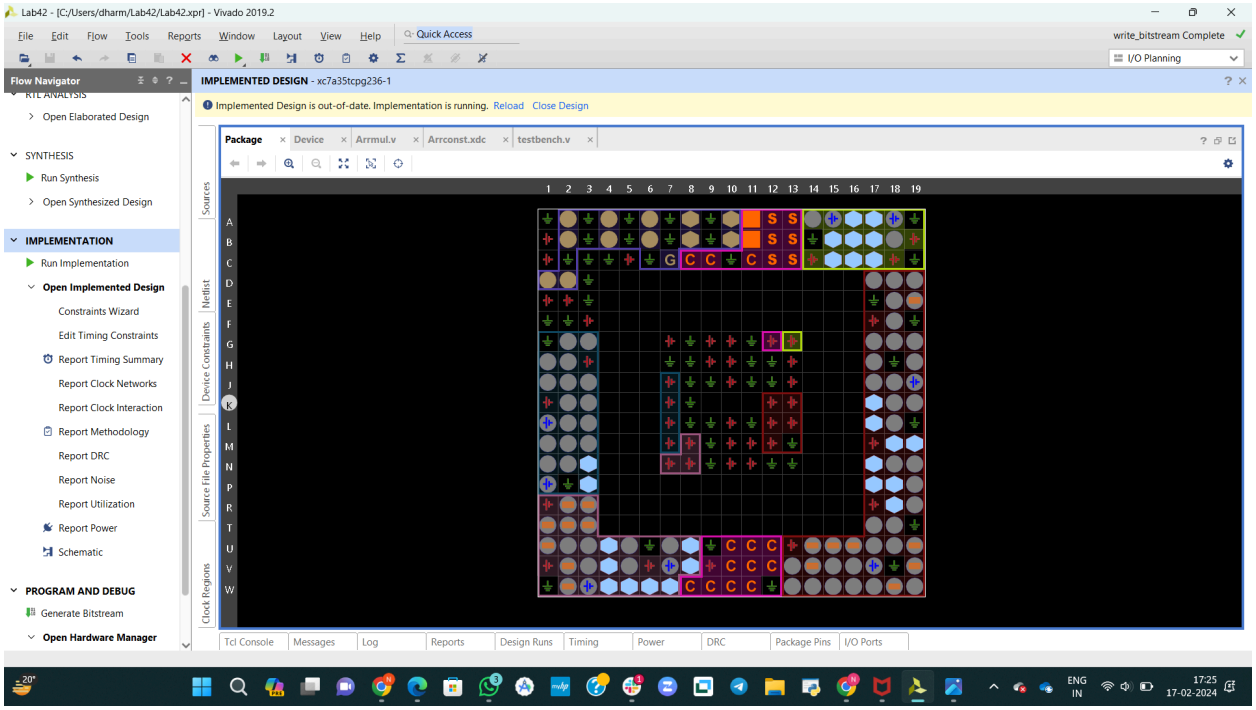
RESULTS OF SIMULATION OF 8-Bit ARRAY MULTIPLIER



POWER UTILIZATION REPORTS




Lab42 - [C:/Users/dharm/Lab42/Lab42.xpr] - Vivado 2019.2
File Edit Flow Tools Reports Window Layout View Help
Quick Access
write_bitstream Complete
I/O Planning
Flow Navigator
Open Elaborated Design
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
Constraints Wizard
Edit Timing Constraints
Report Timing Summary
Report Clock Networks
Report Clock Interaction
Report Methodology
Report DRC
Report Noise
Report Utilization
Report Power
Schematic
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Implemented Design is out-of-date. Implementation is running. Reload Close Design
Package Device Arrmul.v Arrconst.xdc testbench.v
X0Y2
X1Y2
X0Y1
X1Y1
X0Y0
X1Y0
Sources
Netlist
Device Constraints
Source File Properties
Clock Regions
Tcl Console Messages Log Reports Design Runs Timing Power DRC Package Pins I/O Ports
ENG IN
17:25
17-02-2024


Lab42 - [C:/Users/dharm/Lab42/Lab42.xpr] - Vivado 2019.2
File Edit Flow Tools Reports Window Layout View Help
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PROGRAM AND DEBUG
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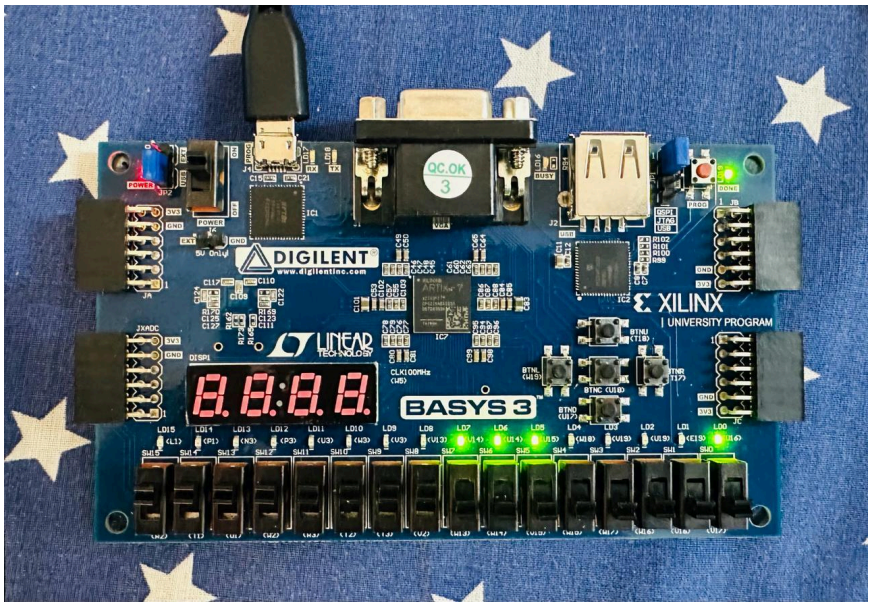
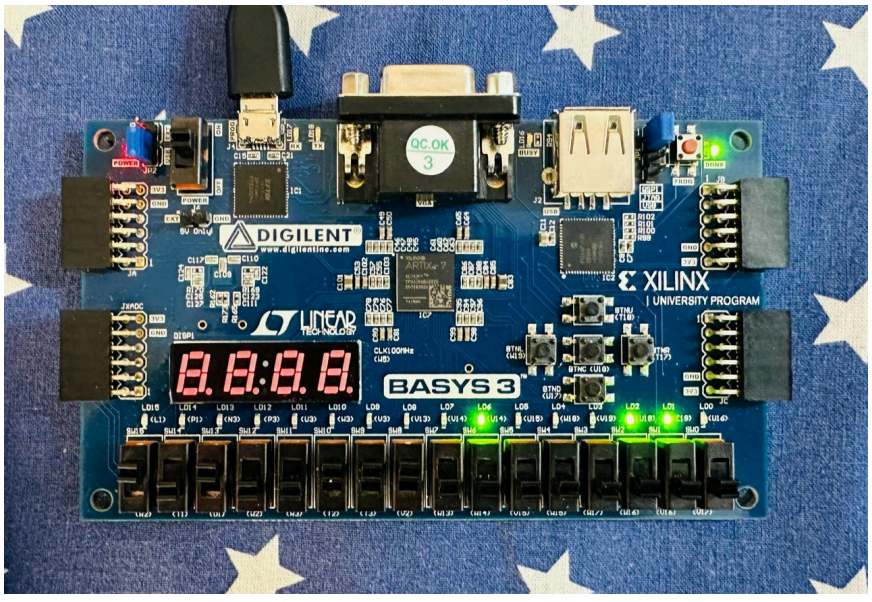
IMPLEMENTED DESIGN - xc7a35tcpg236-1
Implemented Design is out-of-date. Implementation is running. Reload Close Design
Package Device Arrmul.v Arrconst.xdc testbench.v
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
A B C D E F G H J K L M N P R T U V W
Sources
Netlist
Device Constraints
Source File Properties
Clock Regions
Tcl Console Messages Log Reports Design Runs Timing Power DRC Package Pins I/O Ports
ENG IN
17:25
17-02-2024

FPGA IMPLEMENTATION

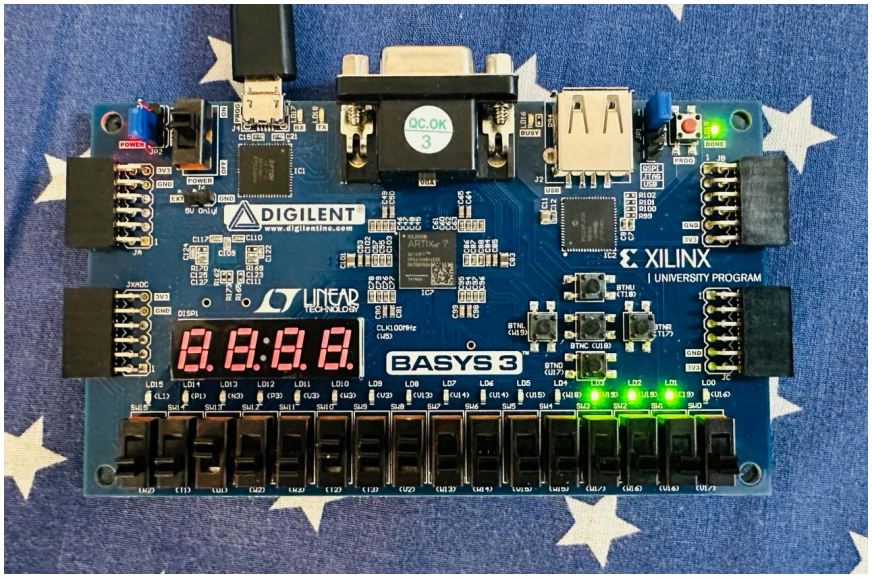
A = 4’b1111 (15), B = 4’b1111 (15), P = 8’b11100001 (225)



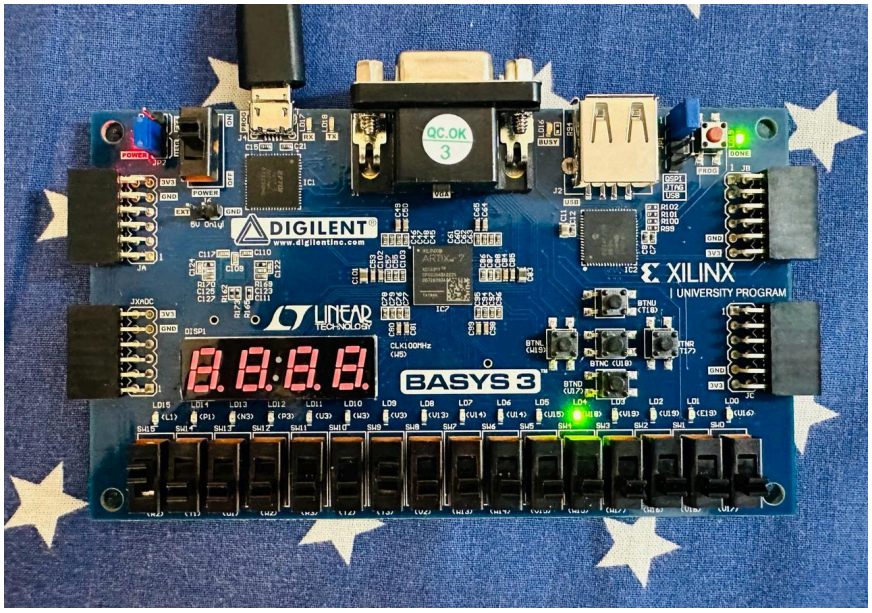
A = 4’b1010 (10), B = 4’b0111 (7), P = 8’b01000110 (70)



A = 4’b0010 (2), B = 4’b0111 (7), P = 8’b00001110 (14)



A = 4’b1000 (8), B = 4’b0010 (2), P = 8’b00010000 (16)



BINARY MULTIPLIER

PART – 2

8-bit **Binary (Shift - Add) Multiplier**.

VERILOG CODE

```
`timescale 1ns / 1ps
module bin_mul(Multiplicand, Multiplier, P);

parameter N = 4;
input [N - 1 : 0] Multiplicand, Multiplier;
output reg [2 * N - 1 : 0] P;

reg [2 * N - 1 : 0] MultiplicandC;
reg [2 * N - 1 : 0] MultiplierC;
integer i;

always @(*) begin
    P = 0;
    MultiplicandC = Multiplicand;
    MultiplierC = Multiplier;
    for (i = 0; i < N; i = i + 1) begin
        if (MultiplierC[0] == 1) begin
            P = P + MultiplicandC;
        end
        MultiplicandC = MultiplicandC << 1;
        MultiplierC = MultiplierC >> 1;
    end
end

endmodule
```

TESTBENCH

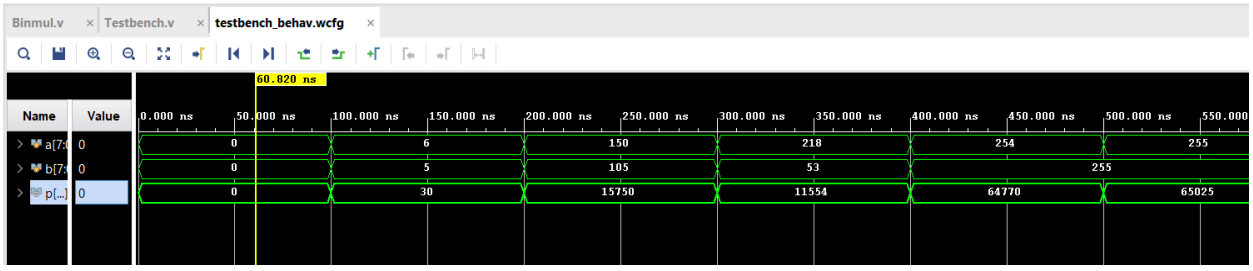
```
module testbench;

reg [7 : 0] a, b;
wire [15 : 0] p;

bin_mul obj(.Multiplicand(a), .Multiplier(b), .P(p));

initial begin
    $monitor($time, " A = %d (%b), B = %d (%b), P = %d (%b)", a,
a, b, b, p, p);
    a = 8'b00000000; b = 8'b00000000;
    #100 a = 8'b00000110; b = 8'b00000101;
    #100 a = 8'b10010110; b = 8'b01101001;
    #100 a = 8'b11011010; b = 8'b00110101;
    #100 a = 8'b11111110; b = 8'b11111111;
    #100 a = 8'b11111111; b = 8'b11111111;
    #100 $finish;
end

endmodule
```

CONSTRAINT FILE

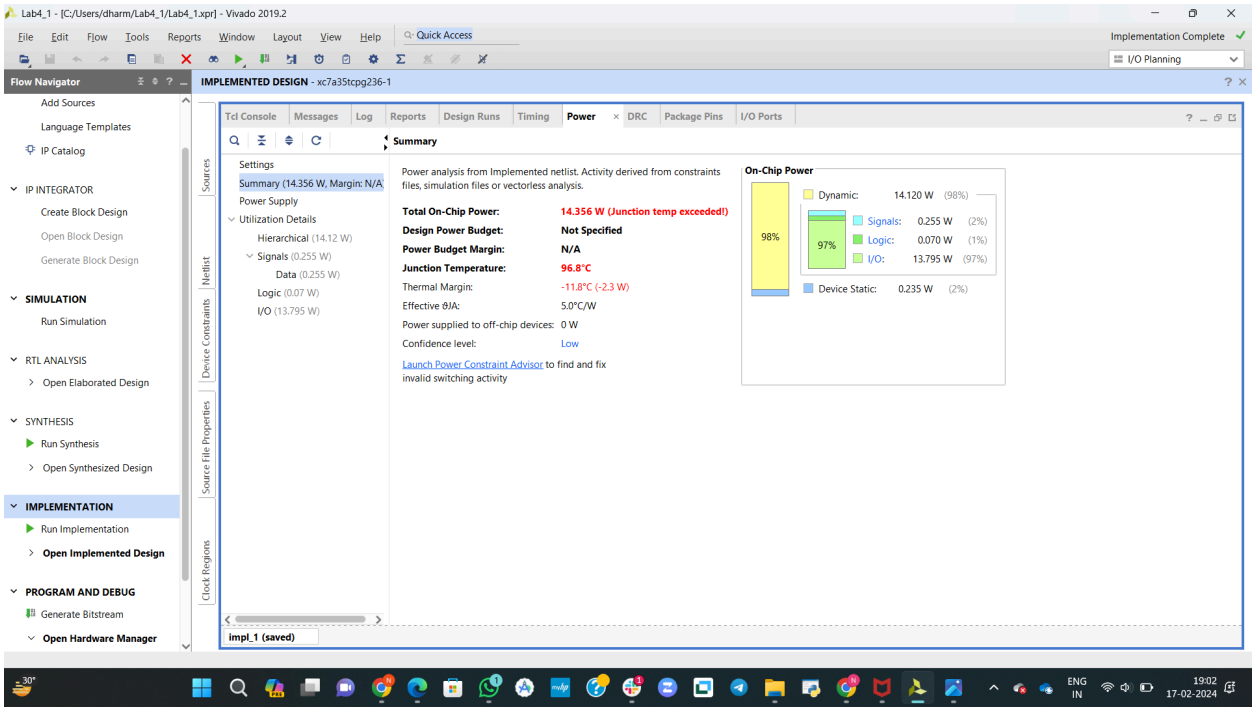
```
set_property IOSTANDARD LVCMOS33 [get_ports {Multiplicand[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Multiplicand[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Multiplicand[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Multiplicand[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Multiplier[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Multiplier[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {Multiplier[1]}]
```

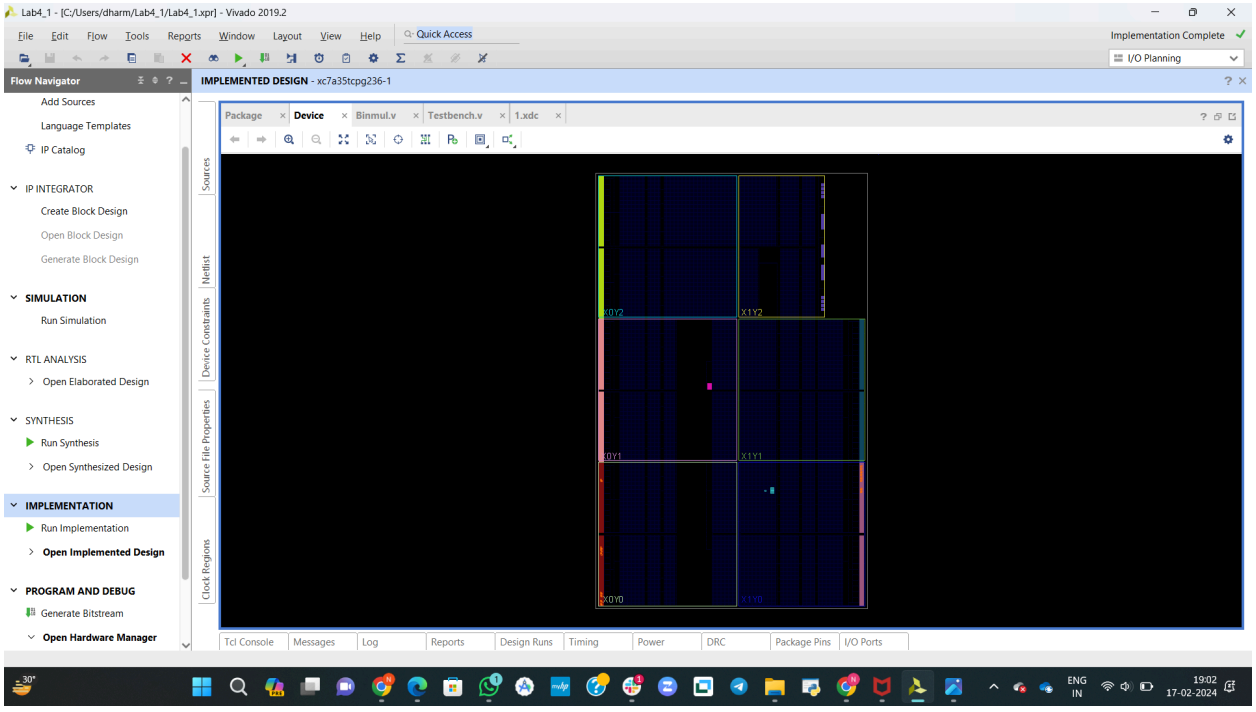
```
set_property IOSTANDARD LVCMOS33 [get_ports {Multiplier[0]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[7]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[6]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[5]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[4]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[3]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[2]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[1]}]
set_property IOSTANDARD LVCMOS33 [get_ports {P[0]}]

set_property PACKAGE_PIN R2 [get_ports {Multiplicand[3]}]
set_property PACKAGE_PIN T1 [get_ports {Multiplicand[2]}]
set_property PACKAGE_PIN U1 [get_ports {Multiplicand[1]}]
set_property PACKAGE_PIN W2 [get_ports {Multiplicand[0]}]
set_property PACKAGE_PIN R3 [get_ports {Multiplier[3]}]
set_property PACKAGE_PIN T2 [get_ports {Multiplier[2]}]
set_property PACKAGE_PIN T3 [get_ports {Multiplier[1]}]
set_property PACKAGE_PIN V2 [get_ports {Multiplier[0]}]
set_property PACKAGE_PIN V14 [get_ports {P[7]}]
set_property PACKAGE_PIN U14 [get_ports {P[6]}]
set_property PACKAGE_PIN U15 [get_ports {P[5]}]
set_property PACKAGE_PIN W18 [get_ports {P[4]}]
set_property PACKAGE_PIN V19 [get_ports {P[3]}]
set_property PACKAGE_PIN U19 [get_ports {P[2]}]
set_property PACKAGE_PIN E19 [get_ports {P[1]}]
set_property PACKAGE_PIN U16 [get_ports {P[0]}]
```

RESULTS OF SIMULATION OF 8-Bit BINARY MULTIPLIER



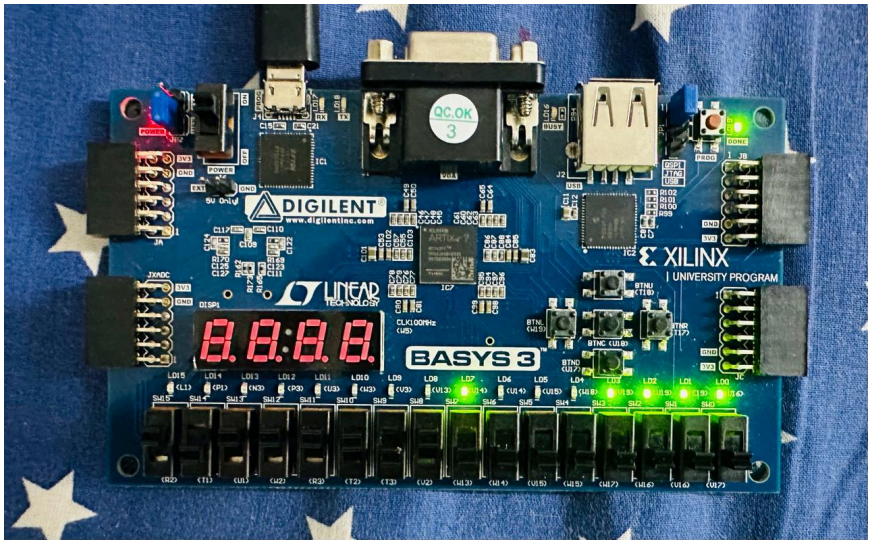
POWER UTILIZATION REPORTS



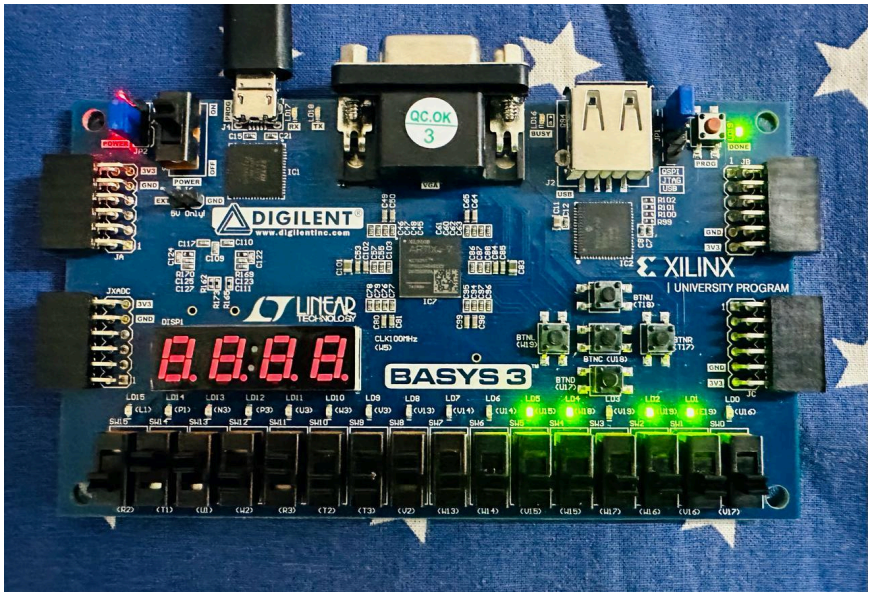


FPGA IMPLEMENTATION

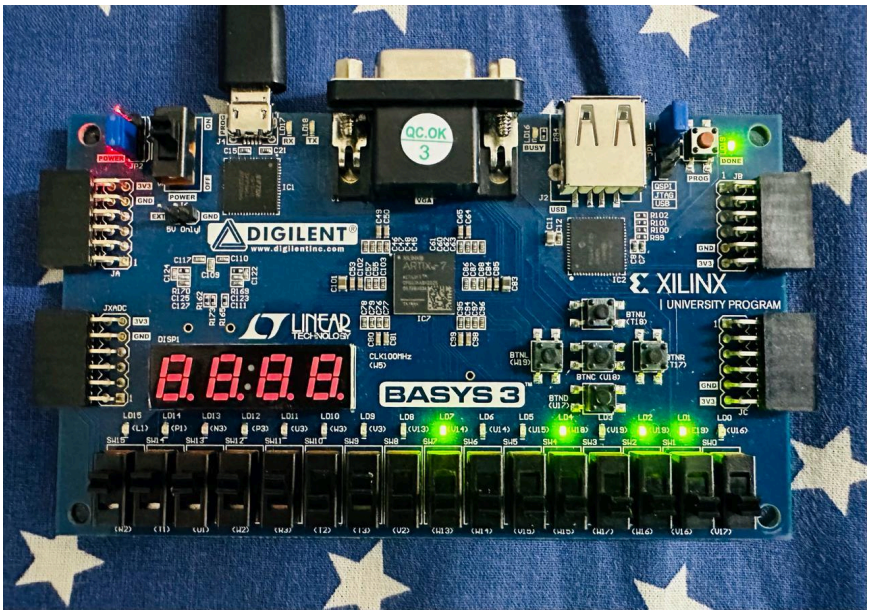
A = 4’b1011 (11), B = 4’b1101 (13), P = 8’b10001111 (143)



A = 4’b0110 (6), B = 4’b1001 (9), P = 8’b00110110 (54)



A = 4’b1111 (15), B = 4’b1010 (10), P = 8’b10010110 (150)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