

Energy- and Cost-Efficiency Analysis of ARM-Based Clusters

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Abstract—General-purpose computing domain has experienced strategy transfer from scale-up to scale-out in the past decade. In this paper, we take a step further to analyze ARM-processor based cluster against Intel X86 workstation, from both energy-efficiency and cost-efficiency perspectives. Three applications are selected and evaluated to represent diversified applications, including Web server throughput, in-memory database, and video transcoding. Through detailed measurements, we make the observations that the energy-efficiency ratio of the ARM cluster against the Intel workstation varies from 2.6-9.5 in in-memory database, to approximately 1.3 in Web server application, and 1.21 in video transcoding. We also find out that for the Intel processor that adopts dynamic voltage and frequency scaling (DVFS) techniques, the power consumption is not linear with the CPU utilization level. The maximum energy saving achievable from DVFS is 20%. Finally, by utilizing a monthly cost model of data centers, we conclude that ARM cluster based data centers are feasible, and are advantageous in computationally lightweight applications, e.g. in-memory database and network-bounded Web applications. The cost advantage of ARM cluster diminishes progressively for computation-intensive applications, i.e. dynamic Web server application and video transcoding, because the number of ARM processors needed to provide comparable performance increases.

Keywords—energy-efficiency; cost-efficiency; scale-out; ARM cluster;

I. INTRODUCTION

With the increasing use of Internet services and cloud computing, energy efficiency of data centers is a major concern for industry and a focus of an array of research activities. In the past, data centers relied on purpose-built servers with highly powerful processors, whilst today the dominant approach is to build datacenters from commodity hardware components [1]. The same processors used in general purpose computing, e.g. workstations, are now used in servers. Following the Moore's law, the performance of these general-purpose processors has greatly improved. Although their energy-efficiency has also improved, low energy consumption has, until recently, been a secondary objective. Most desktops and workstations were wire-powered, environmental concerns were weak, and the share of electricity cost in the overall operational expense was small.

At the same time, another line of processors were developed to meet the needs of the rapidly growing sector

of handheld devices. For these battery-operated devices the energy-efficiency has been the key design goal since the beginning. The performance of these embedded processors is naturally lagging the performance of general-purpose processors. However, it is interesting to ask if a large number of these low-power, low-performance processors could be used to build a data center with similar processing power but smaller energy consumption. The general-purpose processors already overtook the powerful purpose-built processors in data centers [1]. Could the wimpy mobile processors, in turn, overtake the general-purpose processors in future data centers?

To answer this question, Hamilton [2] built a low-power, low-cost server prototype utilizing relatively low power AMD Athlon processors. However, in this research we want to investigate even weaker processors utilized in cellular phones and other embedded systems. In particular we study the widely used ARM processors. In the field of high performance computing, embedded processors have been investigated to build supercomputers [3] [4]. However, to the best of our knowledge, building server clusters with such embedded processors for general purpose computing has not been investigated systematically before. Our aim is to compare the use of embedded processors with the use of general-purpose processors and to understand the performance, energy consumption, and cost tradeoffs.

For concrete experimentation, we use ARM-based Cortex A9 MPCore processor as a representative of embedded processors and Intel Core2-Q9400 as a representative of general-purpose processors. We build a cluster consisting of four PandaBoard development boards with dual-core Cortex A9 MPCore processors and compare it against an Intel workstation with quad-core Core2-Q9400 processor.

Our contributions are as follows:

(1) A set of detailed measurements, with benchmarks on Web server throughput, in-memory database access, and video transcoding, showing that ARM-based clusters are more energy-efficient than Intel X86 processors. For the same task an ARM cluster is 1.2 to 9.5 times more energy-efficient than an Intel workstation.

(2) We find out that linear model does not fit for processors that adopt advanced power management techniques,

specifically dynamic voltage and frequency scaling, whilst a linear model fits well with the ARM cluster and the Intel processor when the SpeedStep is disabled. SpeedStep can achieve at maximum 20% energy saving when the processor is under relatively lightweight load, e.g. less than 40% CPU utilization level. It contributes minor energy saving when the CPU is heavily loaded.

(3) From the cost perspective, ARM cluster based data centers are most economical when applications have small computational needs. The cost advantage in comparison to Intel processors diminishes for computation-intensive applications because the number of ARM processors required for comparable performance increases.

The rest of the paper is structured as follows. In Section II, we present background and related literature of energy-efficient server design. Section III details the experimental setup and Section IV describes the measurement results. Section V analyzes the feasibility of building data centers from ARM clusters from cost and energy perspectives. In Section VI we conclude the paper and present ideas for future work.

II. BACKGROUND AND MOTIVATION

Thanks to Moore's law, the number of transistors that can be integrated economically in a single integrated circuit has been doubled approximately every two years for more than four decades. Going step by step with the progressively increasing number of transistors in a single integrated circuit is the advancement of the processor capability. That is referred to as *scale-up* strategy. On the other hand, the Internet sector, wherein the applications are naturally distributed, has been the fastest growing server market in recent years and starts to dominate the low-end server market revenue growth [5]. Utilizing large volume of commodity servers to replace a small number of high-end servers starts to dominate the data center design for Internet sector, which is referred to as *scale-out* strategy. However, the *scale-out* strategy is still based on high-quality, purpose-built design. Hamilton [2] made one step further from that direction by building up a low cost, low power prototype server based on non-server-class components, i.e. AMD Athlon processors. The results from [2] showed that the non-server components design could achieve 3.7 times improvement from cost perspective, and 3.9 times improvements from energy perspective.

One straightforward step from the work of Hamilton [2] is to utilize embedded components directly to build up a data center. There are a few activities in this direction. EuroCloud [6] has been focused on building ARM Cortex processors with 3D memory technology to support hundreds of cores in a single server. Mont-Blanc [3] and Green Flash project [4] are targeting at building supercomputers from ARM processors for high performance computing rather than for general purpose computing, whilst the latter is the focus of this paper. Lim et al. [5] provided a compact comparison

of various processor types, ranging from mid-range server systems to low-end embedded systems. However, their work solely compared the various systems from a single processor perspective, without considering the scenario wherein multiple lower-performance processors organize into a cluster to compete against a more powerful processor. Furthermore, they did not look into the relationship between performance and CPU utilization level. Andersen et al. [7] presented a log-structured key-value storage system, i.e. FAWN (Fast Array of Wimpy Nodes), by coupling low-power embedded CPUs with local flash disks. Specifically, commodity PEngine Alix 3c2 devices with single-core 500 MHz AMD Geode LX processors are utilized to set up the system. The primary difference with the work in this paper is that FAWN [7] targeted at designing a specialized system for key-value based storage system, whilst the work presented in this paper provides generic comparison between ARM processors and Intel processors. ZT Systems [8] announced a more loosely coupled solution to integrate eight discrete servers, which are based on dual-core ARM Cortex A9 processor, into one 1U enclosure. Like all proprietary products, no statistics about the performance or energy-consumption are released. This motivates our work to analyze the performance, energy-efficiency, and cost-efficiency of data centers built from ARM clusters against from Intel workstations.

III. EXPERIMENTAL CONFIGURATIONS

A. Experimental Configurations

We use four PandaBoards connected locally through an Ethernet switch to build up the ARM-based cluster. We purposely choose an Intel workstation, which is currently used in our office environment, rather than an Intel server because client-components have tentatively been used to provide lower cost and lower power, as shown in [2]. It is noteworthy that the processor of the workstation, i.e. Intel Core 2 Q9400, was launched in 2008, whilst ARM Cortex-A9 MPCore was launched in 2009, and newer Intel processors might provide better performance with similar thermal design power. However, the performance of ARM processors are increasing at the same time. Thus, this potential bias from slightly outdated hardware configuration does not impact the conclusions we made in this paper to a large extent. The detailed configurations are illustrated in Table I.

PandaBoard does not have a hard disk drive (HDD) or solid-state drive (SSD) storage disk, but rather a SD card. Thus, we try to avoid experiments that involve disk operations. Furthermore, the workstation and the PandaBoard have different memory capacity, 8GB vs. 1 GB. Since they use the same generation of memory technology, i.e. DDR2, the capacity difference should not bias the results significantly. Be noted that the PandaBoard has a 100 Mbps Ethernet Network Interface Card (NIC), whilst the Intel workstation has a 1000 Mbps Ethernet NIC. This affects the maximum

Table I
EXPERIMENTAL CONFIGURATIONS

	PandaBoard	Intel Workstation
Processor	OMAP4430 (ARM Cortex-A9 MPCore)	Intel Core2 Q9400
Lithography	45 nm	45 nm
# cores	2	4
Clock frequency	1 GHz	2.66 GHz
Memory	1 GB DDR2	8 GB DDR2
Storage	16 GB SD card	248 GB hard disk
Network	100 Mbps Ethernet	1000 Mbps Ethernet
Operating System	Ubuntu 10.10 with Linux kernel 2.6.35	Ubuntu 10.10 with Linux kernel 2.6.35
Thermal design power	1.9 watts	95 watts

Web throughput achievable for the ARM cluster in network-bounded operations, as shown in Section IV.

B. Test Methodology

For metering the ARM platform, we use a Monsoon power monitor to measure the power consumption of a Pandaboard. For Intel workstation power measurement, we use a Mastech MS2102 AC/DC clamp meter with a maximum of 200A current and an accuracy of $\pm 2.5\%$. The sampling frequency of the clamp meter is 2 times/sec. We attach the clamp meter to 5V and 12V lines from the power supply to acquire the line current. By multiplying the measured current with the line voltage, we can derive the power consumption. To increase the accuracy of the measurements, power supply lines are wrapped around the clamp meter as many times as possible, and the final record is the total value divided by the number of loops, the same method as in [9].

Our aim is to provide an apple-to-apple comparison. Given the fact that it is difficult to isolate the power consumption of the ARM processor from the other peripheral components (e.g. SD card) in PandaBoard, we have to use the overall power consumption of the whole PandaBoard to compare with power consumption of the Intel workstation. To better understand the relationship between processor utilization level and the associated power consumption, Dstat¹, a Linux system monitoring software, is used to record the CPU utilization level.

Furthermore, to factor out casual errors and environmental interferences, every test case in Section IV is running over 60 seconds after its value is stable. There is a reboot between two exhausting tests (tests during which the CPU utilization level is close to 100%) to cool down and reset the system. Each trial is repeated multiple times in indoor office environment to exclude casual errors.

C. Evaluation Metrics

To get a straightforward view of the varying trend of energy-efficiency (EE) corresponding to performance, we

use the same EE index as in [9], which is defined as the ratio of the useful work (e.g. computation, communication) conducted to the energy consumed:

$$EE = \frac{Work}{Energy} = \frac{Work}{Power * Time} = \frac{Performance}{Power} \quad (1)$$

A 95% confidence interval is used where appropriate.

IV. ENERGY-EFFICIENCY ANALYSIS

We describe in detail three sets of experiments as aforementioned in this section. Power consumption and performance are the primary metrics used to compare the ARM-based cluster and the Intel workstation.

To set a baseline for the comparison between the ARM cluster and Intel workstation, we first use a micro-benchmark tool, LMBench², to measure the completion time of basic UInt64 operations, including Bit, Add, Multiply, Divide, and Mod, for a PandaBoard and the Intel workstation. Not surprisingly, the Intel workstation outperforms PandaBoard from every basic operation. For simple operations, e.g. Add and Bit, the difference is roughly 4-5 times; for more complex operations, e.g. Divide, the Intel workstation outstrips PandaBoard by 14 times.

A. Web Server Throughput

Both static and dynamic Web server throughput measurements are conducted. To test Web server throughput, we install Httpperf³ benchmark tool on a powerful workstation as the client, to avoid possible bottlenecks from the client side. At the server side, Linux Virtual Server (LVS)⁴ is used as a front-end load balancer for the ARM cluster, and Nginx⁵ works as the static resource web server, whilst httpd⁶ is adopted for dynamic Web pages testing.

For static Web measurements, six different file sizes have been measured, including 1 KB, 4 KB, 10 KB, 30 KB, 50 KB and 100 KB. For dynamic Web measurements, PHP5 and httpd are installed on the system under test. PHP scripts are used to generate the responding HTML file dynamically. Three different workload levels are designed (low, medium, and high) to perform mathematical summation (from 1 to 100, from 1 to 1000, and from 1 to 10000, respectively). It is worth noting that to better measure the Web server's capability, the responses are non-cached at the server side.

For the Httpperf parameters, the configurations are based on practical usage experience from [10]. We have tested 1, 10, 20, and 30 requests per connection, and the difference amongst them is not substantial. Thus, we use 10 requests per connection throughout the Web server measurements. These parameters might affect the absolute value of each

²LMBench: <http://www.bitmover.com/lmbench/>

³Httpperf: <http://www.hpl.hp.com/research/linux/httpperf/>

⁴Linux Virtual Server (LVS): <http://www.linuxvirtualserver.org/>

⁵Nginx: <http://wiki.nginx.org/Main>

⁶httpd: <https://httpd.apache.org/docs/2.0/programs/httpd.html>

¹Dstat: <http://dag.wieers.com/home-made/dstat/>

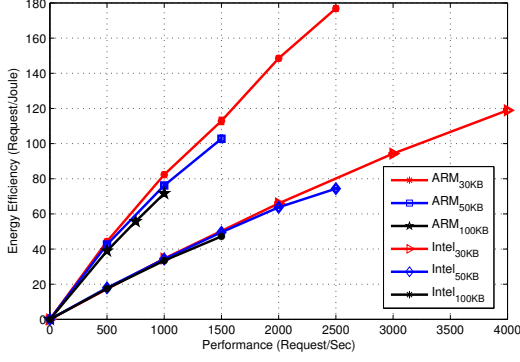


Figure 1. Static Web throughput measurements

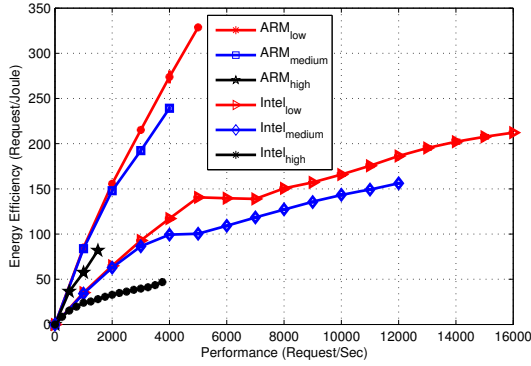


Figure 2. Dynamic Web throughput measurements

measurement, but do not have any influence on the comparison because they are the same for both the ARM cluster and Intel workstation.

Figure 1 depicts the results of static Web throughput measurements of ARM cluster vs. Intel workstation for file sizes 30 KB, 50 KB, and 100 KB. Fig. 2 demonstrates the results of dynamic Web throughput measurements with the aforementioned low, medium, and high workloads. The results of static Web throughput measurements for file sizes 1 KB, 4 KB, and 10 KB show similar trend as the dynamic Web throughput measurement, because they both are CPU-bounded. We do not show the figure in this paper because of space limitation. It should be noted that the experiments shown in Fig. 1 are network-bounded. The CPU utilization level is less than 60% for the ARM cluster, whilst less than 17% for the Intel workstation.

From Fig. 1 and Fig. 2, we can see that the trends for the ARM cluster are the same, i.e. the EE index grows linearly as the performance increases. The acceleration (the slope of the curves) stays approximately the same within each experiment. For different experiment, slightly different acceleration occurs (cf. ARM_{low} and ARM_{medium} in Fig.

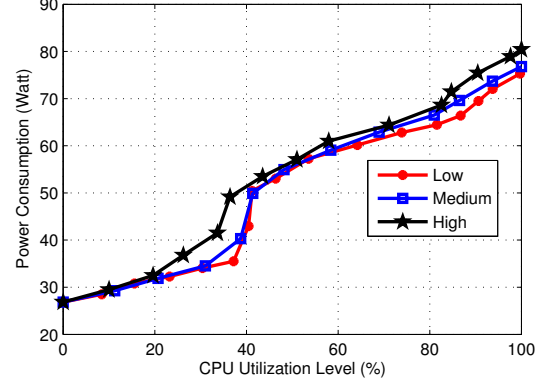


Figure 3. Power consumption vs. CPU utilization level of Intel workstation (SpeedStep enabled)

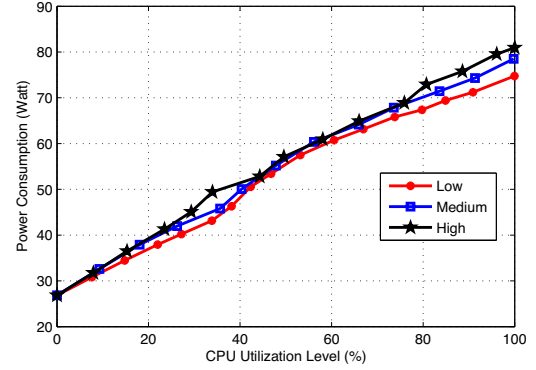


Figure 4. Power consumption vs. CPU utilization level of Intel workstation (SpeedStep disabled)

2). For the Intel workstation, the trends are more complex. It is shown that in Fig. 2, the EE index of the Intel workstation increases in tandem with performance at the beginning (cf. $Intel_{low}$ from 0 to 5000 requests/sec). Then the EE index stays the same for certain performance levels (cf. the $Intel_{low}$ from 5000 to 7000 requests/sec). Afterwards, the EE index continues growing but with lower acceleration until the processor reaches its full processing capability (cf. $Intel_{low}$ from 7000 through 16000 requests/sec).

We conjecture the irregular behaviour of the Intel workstation is caused by the Enhanced Intel SpeedStep technology⁷ that the Intel Core2-Q9400 processor adopts. Thus, we further look into the relationship between CPU utilization level and power consumption for dynamic Web throughput measurements. The results are depicted in Fig. 3.

Figure 3 shows that a step occurs during 30%-40% CPU utilization level, whilst another step occurs at around 80% CPU utilization level. When we conducted the experiments,

⁷<http://www.intel.com/support/processors/sb/CS-028855.htm>

we noticed that when the CPU utilization level of the Intel workstation reached around 30%, one core started to scale from 2.00 GHz to 2.33 GHz. When the CPU utilization level reached around 35%, the core further scaled from 2.33 GHz to 2.66 GHz. When close to 40%, two cores scaled to 2.66 GHz. Then for relatively broad range of CPU utilization levels, from 40% to 80%, two cores stayed steadily at 2.66 GHz, whilst the other two cores remained at 2.00 GHz. When the CPU utilization level continued to increase to exceed 80%, all the four cores were scaled to 2.66 GHz. The abrupt scaling of frequency occurring at 30%-40% and 80% of CPU utilization levels makes the performance gains hard to justify the increased power consumption. Thus, the EE of $Intel_{low}$ in Fig. 2 stays at the same value when the performance ranges from 5000 to 7000 requests/sec, wherein the processor utilization level is exactly during 30% and 40%. The curves of $Intel_{medium}$ and the $Intel_{high}$ in Fig. 2 show similar trend as $Intel_{low}$. The scaling of frequency also explains the behavior of the Intel workstation shown in Fig. 1, because the CPU utilization level of the Intel workstation is less than 17%.

To further investigate the impact of SpeedStep technology on the energy consumption of the Intel workstation, we disable the SpeedStep function of the workstation and rerun the experiments in Fig. 3. The results are depicted in Fig. 4. Unsurprisingly, the energy consumption of the Intel workstation grows linearly with the CPU utilization level. The initial energy consumption of the Intel workstation at idle state is the same for the SpeedStep enabled and disabled cases. Compare Fig. 3 with Fig. 4, we can see that the primary difference of the two cases, i.e. SpeedStep enabled vs. SpeedStep disabled, occurs when the CPU utilization level is lower than 40%, wherein the SpeedStep enabled case is 1.1-1.2 times energy efficient than the SpeedStep disabled case. Namely, the SpeedStep can achieve up to 20% energy saving. The energy consumption of the two cases stays approximately the same when their respective CPU utilization level is higher than 40%. A generic trend is that when the same number of requests is served, the CPU utilization level of SpeedStep enabled case is slightly higher than that of SpeedStep disabled. This is understandable because the SpeedStep technology utilizes lower CPU frequency to achieve better energy efficiency, thus higher CPU utilization level is required.

We also check the relationship between the CPU utilization level and power consumption for PandaBoard, the result is illustrated in Fig. 5. We can see that the power consumption increases linearly with the CPU utilization level, and the high workload consumes slightly more power than the medium and low workload.

In Fig. 1 and Fig. 2, we compare the EE indices of the ARM cluster and the Intel workstation at different performance level. It is also interesting to compare their EE indices at the same CPU utilization levels. The result

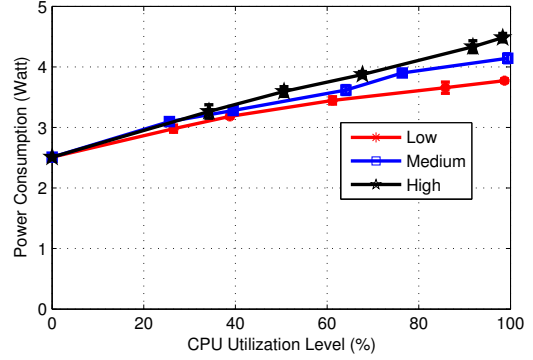


Figure 5. Power consumption vs. CPU utilization level of PandaBoard

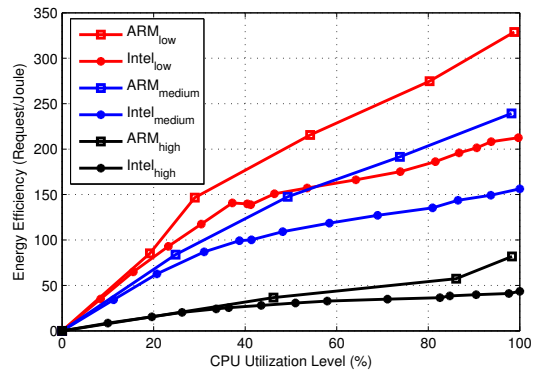


Figure 6. Energy-efficiency vs. CPU utilization level

is depicted in Fig. 6. It is shown that the ARM cluster does not have substantial advantage against the Intel workstation when the CPU utilization level is less than 20%. This is because the PandaBoard has a relatively large fraction of upfront power consumption when the processor is idle. The idle power of PandaBoard is 2.59 Watts, whilst the peak power is 4.45 Watts for high workload in dynamic Web server measurements (2.59/4.45=58.2% idle/peak). The Intel workstation has 26.85 Watts, and 80.45 Watts for its idle power and peak power, respectively (26.85/80.45=33.37% idle/peak). When the CPU utilization level is larger than 20%, ARM cluster shows its advantage in energy-efficiency. The EE ratio of the ARM cluster against the Intel workstation is 1.2-1.4 for CPU utilization level from 20% to 100%.

B. In-Memory Database

This experiment is targeting at database's energy efficiency. Because the PandaBoard does not have a hard disk, this experiment only measures in-memory database to exclude the performance difference between hard disk and SD card. We choose SQLite 3.07⁸ as the benchmark. Also

⁸SQLite: <http://www.sqlite.org/>

Table II
IN-MEMORY DATABASE COMPARISON

Operation	Power (Watts)		Time (s)		EE ratio
	ARM	Intel	ARM	Intel	
Full table scan	3.56	45.93	119.3	88.27	9.5
Update	3.50	44.25	60.24	14.42	3.0
Insert	3.47	44.13	51.39	12.26	3.0
Delete	3.48	43.98	43.23	8.73	2.6

be noted that as the database cannot be distributed across different PandaBoards, we use one single PandaBoard to compare against the Intel workstation.

SQLite includes common operations, but does not measure multi-user performance or optimization of complex queries involving multiple joins and subqueries. The experiment includes six test cases: (1) 10000 entries insert; (2) 5000 times full table scan with string comparison; (3) set up an index on the table; (4) 2000 times update with full table string comparison; (5) 5000 times insert from a result of full table scan; (6) 10000 records delete with full table string comparison.

It should be noted that all SQL queries in one test case are included in one SQL transaction to optimize the execution time. The in-memory database experiment contains 6 query tests, but only four tests last more than 1 second, the other two queries' power consumption is negligible. The CPU utilization level is approximately 60% for PandaBoard and 40% for the Intel workstation.

As shown in Table II, the EE ratio of PandaBoard vs. Intel workstation for write operation (update and insert) is around 3.0 and read operation (scan) is 9.5. For a large fraction of real world cases, the in-memory database is used for reading data rather than writing and updating. Generally speaking, ARM processors have an advantage in the in-memory database operations. For further optimizing the execution speed, ARM processors could adopt partition technology, in which each ARM processor only processes one physical sub-table from a big logic table, and the total access speed can be further enhanced.

C. Video Transcoding

Video transcoding is a processing-hungry task, in which ARM processors do not naturally perform well. We run a set of measurements to compare the execution speeds between a single PandaBoard and the Intel workstation. We test four video files from HD-VideoBench [11] (Blue_sky, Pedestrian, Riverbed, and Rush_hour) with three resolutions (1088p, 576p, and 720p). The completion time ratio of ARM/Intel is ranging from 7 to 14 times. The irregularity that occurs at the Riverbed test case is because some part of the encoding algorithm is sequential and exhibits limited data and instruction level parallelism [11]. Normally the Intel workstation is 12-14 times as fast as the PandaBoard.

Pereira et al. [12] demonstrated that by splitting the

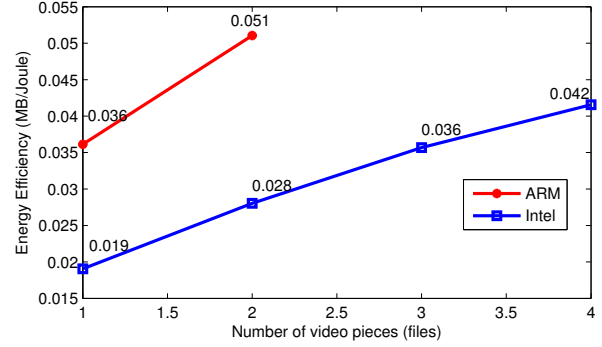


Figure 7. Energy efficiency of video transcoding

overall video into multiple pieces, and then processing the pieces in parallel, the completion time could be significantly shortened. We use the same split and merge mechanism in our experiments. HD-VideoBench with H.264 codec is used as the transcoding benchmarking tool. The original test video is an 86 MB AVI file encoded by H.264 standard in 24 frame/sec, with the resolution of 1920*1080. MEncoder⁹ is used to split a video file into multiple pieces, whilst FFmpeg from HD-VideoBench is used to transcode the video from AVI format into FLV format, and also compress its resolution from 1920*1080 to 640*480, then MEncoder is used to merge the separate FLV files into a complete file.

It is worth noting that multiple FFmpeg processes are used to fully utilize the processing capability of the processors. Furthermore, the power consumption and time spent on merging and splitting video are omitted, because they are too small to be measured.

We use four PandaBoards to form the ARM cluster, the same as in the Web server measurements. We test transcoding one and two video pieces (each of size 86/8=10.75 MB) on a single PandaBoard. To reach comparable execution time, we then test from one through four copies of the complete 86MB video file on the Intel workstation. Two video pieces for a PandaBoard and four 86MB video files for the Intel workstation, respectively, are able to make its processors close to 100% CPU utilization level. The results are shown in Fig. 7.

From the experiments, we notice that the time spent for the ARM cluster to transcode one 86 MB video file, i.e. each PandaBoard processes two 10.75MB video pieces, is approximately the same as the Intel workstation to process four 86 MB video files. Thus, the processing capacity of the Intel workstation is around 16 ((4*86MB)/(2*10.75MB))=16 times of a single PandaBoard. It can be interpreted that in order to provide comparable video transcoding capacity to the Intel workstation, 16 PandaBoards are needed.

From Fig. 7, we can see that the EE of ARM cluster

⁹MEncoder: <http://en.gentoo-wiki.com/wiki/Mencoder>

Table III
COMPARISON BETWEEN ARM CLUSTER AND INTEL
WORKSTATION

Experiments	EE ratio (ARM cluster/Intel)	No. of PandaBoards	Price diff. (ARM cluster/Intel)
Web server throughput	1.3	12	1.16
In-memory database	2.6-9.5	1.35-4.2	1.43-1.63
Video transcoding	1.21	16	1.12

and Intel workstation are both ascending as the number of video clips increases. The acceleration of the ARM cluster is sharper than the Intel workstation. However, two video pieces in parallel already hit the performance roof of a single PandaBoard. Thus, the most realistic EE ratio of ARM cluster/Intel is 1.21 (0.051MB/Joule for the ARM cluster, and 0.042 MB/Joule for the Intel workstation), in which the processing capacity of ARM processors and Intel processor is fully utilized. This low EE ratio (1.21) can be interpreted that the ARM cluster does not achieve significant energy savings against the Intel workstation in video transcoding.

V. IMPLICATIONS FOR DATA CENTER DESIGN

A. Energy-efficiency

Recall from Section IV, we know that power consumption of the Intel workstation increases as the CPU utilization level increases. However, the relation is non-linear, but rather step-like, because of the Enhanced Intel SpeedStep Technology. However, even with the advanced dynamic voltage and frequency scaling technology, the EE ratio of ARM/Intel for the three experiments are larger than 1, meaning the ARM cluster is more energy-efficient than the Intel workstation. The detailed EE ratios are summarized in Table III.

The 'EE ratio (ARM cluster/Intel)' column demonstrates that different application shows significantly different EE ratio. The in-memory database application has the biggest advantage. The full table scanning, which is dominated by read operations, is representative in the database application, showing 9.5 times energy-efficient. The other operations, including update, insert, and delete, demonstrate less advantage than the scanning operation. However, the difference of ARM and Intel is still in the scale of 2.6 to 3.0. The dynamic Web server measurements, and static Web server measurements for small sizes (1 KB, 4 KB, and 10 KB) present similar results to the video transcoding application. The EE ratio of the ARM cluster against the Intel workstation is ranging from 1.2 to 1.4 (we use the average of 1.2 and 1.4, i.e. 1.3, in Table III) for the Web server measurements, whilst 1.21 for the video transcoding measurements. In the static Web server measurements, compared with small file sizes, the ARM cluster shows larger benefits for large file sizes (30 KB, 50 KB, and 100 KB) against the Intel workstation (cf. Fig. 1). The EE ratio

is approximately 1.5 when both the ARM cluster and the Intel workstation are at full capacity. Recall that in Section III, PandaBoard is configured with a 100 Mbps Ethernet interface card, whilst the Intel workstation is configured with a 1000 Mbps Ethernet interface card. The ARM cluster (four PandaBoards) can provide 400 Mbps maximum network capacity. Scale the EE ratio of 1.5 with the network capacity difference 2.5 (1000Mbps/400Mbps), we can get an EE ratio of 4.25 (ARM cluster/Intel workstation) if the ARM cluster is also configured with 1000Mbps network capacity.

The number of ARM processors needed to provide comparable performance as the Intel processor is listed in the column of 'No. of PandaBoards' in Table III. The number shown in the 'In-memory database' application is simply a ratio of the completion time of PandaBoard vs. Intel workstation. Because of the natural complexity of databases in general, the actual number might be slightly larger than the numbers shown in Table III for database application.

In summary, ARM-based processors are advantageous in the applications that are naturally distributed, and computationally lightweight. When the applications are becoming more and more computation-intensive, the advantages of ARM processors diminish. To date, Intel processors are on average more powerful than ARM processors, whilst their energy-efficiency is the opposite. In the future, the performance of ARM processors will increase and, meanwhile, the EE of general-purpose computing processors will improve, possibly resulting into these two worlds approaching each other.

B. Cost Comparison of ARM Cluster and Intel Workstation

From the previous analysis we see that to be able to provide comparable performance as an Intel workstation, multiple ARM processors (forming an ARM cluster) are needed. In this subsection, we discuss the feasibility of building data centers using ARM clusters from the perspective of cost, including both capital expenditure and operational expenses.

We use the Hamilton's monthly cost model [2] for a 15 megawatts data center as the reference. Be noted that although Hamilton's model is dated back to 2009, it remains to be one of the widely used cost models for estimating a data center's cost. With Hamilton's data, we can create an estimate for the overall cost (C) distribution of a data center: (1) Server cost (S): 53.32%; (2) Fully burdened cost of power (P): 37.47%; (3) Building cost (B): 4.15%; (4) Other infrastructure cost (O): 5.06%.

The cost model of a data center consisting of ARM clusters and Intel workstations can be denoted as follows:

$$\begin{aligned} C_{Intel} &= S_{Intel} + P_{Intel} + B_{Intel} + O_{Intel} \\ C_{ARM} &= S_{ARM} + P_{ARM} + B_{ARM} + O_{ARM} \end{aligned} \quad (2)$$

Amongst them, $P_{ARM} = P_{Intel}/R_{EE}$. To simplify the analysis, we assume that the costs from building and other

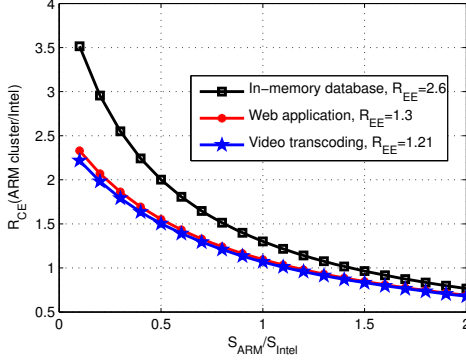


Figure 8. Cost-efficiency ratio of ARM cluster/Intel as a function of the price difference of ARM cluster/Intel

infrastructure are the same for data centers built from ARM clusters and Intel workstations. This is based on the assumption that the selection of different processors does not have a major effect on the physical size of the data center. Thus, the cost-efficiency (CE) ratio, R_{CE} , of data centers built from ARM clusters and Intel workstations is:

$$R_{CE} = C_{Intel}/C_{ARM} = 1.86/(S_{ARM}/S_{Intel} + 0.7/R_{EE} + 0.16) \quad (3)$$

Equation (3) shows that the CE ratio of data centers is affected by the ratio of price difference and EE ratio of ARM cluster vs. Intel workstation. A graphical presentation of (3) is shown in Fig. 8.

Figure 8 depicts that as the price difference ratio of the ARM cluster and the Intel workstation, S_{ARM}/S_{Intel} , increases, the CE ratio, R_{CE} , decreases progressively. To make the ARM cluster based data center more cost-efficient than the data center built from Intel workstations, the ARM cluster should be less than 1.16 times, 1.43 times, 1.12 times (for Web server, in-memory database, and video transcoding, respectively) of the price of the Intel workstation. The results are shown in the column of 'Ratio of price diff. (ARM cluster/Intel)' in Table III.

C. Cost Comparison of ARM Processor and Intel Processor

Because the ARM cluster consists of multiple ARM processors (cf. 'No. of PandaBoards' in Table III), we further break down the cost of the ARM cluster in this subsection. In real-world product environment, the SD card used in the PandaBoard will possibly be replaced by centralized HDD or SSD for the cluster, and there likely be other integrations as well, e.g. memory sharing and flash-based disk caching [5]. To simplify the analysis, we assume the other components cost the same for the ARM cluster and the Intel workstation, the primary cost difference results from the processors.

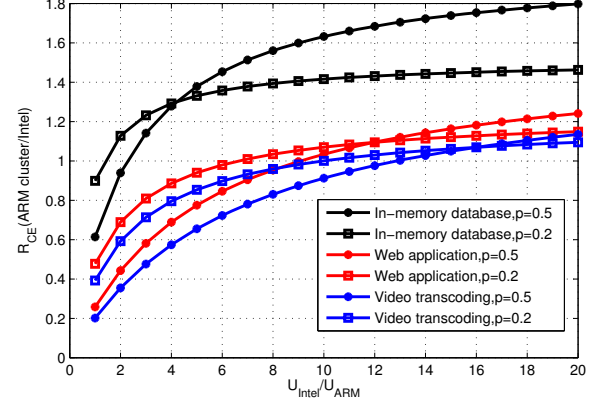


Figure 9. Cost-efficiency ratio of ARM cluster/Intel as a function of the unit price difference of a single processor Intel/ARM

$$\begin{aligned} S_{ARM} &= S_{ARM_proc} + S_{ARM_other} \\ S_{Intel} &= S_{Intel_proc} + S_{Intel_other} \end{aligned} \quad (4)$$

Amongst them,

$$\begin{aligned} S_{Intel_other} &= S_{ARM_other} = ((1-p)/p) * S_{Intel_proc} \\ S_{ARM_proc} &= N_{ARM} * U_{ARM} \\ S_{Intel_proc} &= U_{Intel} \end{aligned} \quad (5)$$

Wherein p stands for the cost percentage of the Intel processor at the overall Intel workstation hardware cost; N_{ARM} denotes the number of ARM processors required (refer to Table III) to provide comparable performance to the Intel workstation; U_{ARM} and U_{Intel} represent unit price of an ARM processor and an Intel processor, respectively. Because we solely use a single Intel processor to compare with an ARM cluster that consists of multiple ARM processors, S_{Intel_proc} is equivalent to the unit price of the Intel processor.

Put (4) and (5) into (3), we acquire the following equation:

$$R_{CE} = 1.86/(p * N_{ARM} * U_{ARM}/U_{Intel} + 0.7/R_{EE} + 1.16 - p) \quad (6)$$

Figure 9 is a graphical representation of (6). Be noted that to make the figure easier to read, we use unit price difference of Intel/ARM, U_{Intel}/U_{ARM} , as x-axis, rather than U_{ARM}/U_{Intel} . Because the unit price of an Intel processor is generally larger than an ARM processor. The same as in Fig. 8, we use the worst case, i.e. $R_{EE} = 2.6$, to represent the in-memory database application.

Not surprisingly, Fig. 9 demonstrates that as the unit price difference of an Intel processor and an ARM processor increases, the CE ratio of a data center consisting of ARM clusters against a data center made up of Intel workstations

grows. On the other hand, as the cost of the processor in the overall cost increases, e.g. p from 0.2 to 0.5, the acceleration of R_{CE} increases (sharper curves), although the starting value is slightly lower. This can be explained by the fact that as the cost of the processor increasingly dominates a single server, when the price difference of an Intel and ARM processor grows, the difference of the overall server cost for the whole data center (Intel vs. ARM) is growing too.

Let us take a look at the tipping points where the CE of ARM clusters overtakes that of Intel workstations. When $p = 0.2$, the tipping points occur at 1.33, 6.64, and 9.95 for the in-memory database, Web application, video transcoding, respectively. That is equivalent to say that in order to be more cost-efficient for a data center built from ARM clusters than built from Intel workstations, an Intel processor should be more than 1.33, 6.64, and 9.95 times as expensive as an ARM processor, which is highly feasible at the current market. Assume $U_{Intel}/U_{ARM} = 10$, and $p = 0.2$, then the CE ratio of ARM cluster against Intel workstation is 1.43, 1.27, and 1.0, respectively, for the in-memory database, Web application, and video transcoding applications.

Thus, it can be concluded that from the cost perspective, ARM cluster based data centers show great advantage in cost for computationally lightweight applications, e.g. in-memory database. For computation-intensive applications, e.g. dynamic Web server application and video transcoding, the cost advantage of ARM cluster progressively diminishes.

VI. CONCLUSION

In this paper, we analyzed data centers built from ARM clusters and Intel workstations from both the energy-efficiency and cost-efficiency perspectives. For the energy-efficiency analysis, we conducted a set of measurements that covered diversified applications, including Web server throughput measurements, in-memory database, and video transcoding. Through the measurements, we made observations that the aforementioned applications in general are more energy-efficient in the ARM cluster than in the Intel workstation. The difference of the energy-efficiency varies from 1.21 to 9.5 in various applications. Multiple ARM processors are needed to provide comparable performance to an Intel workstation. We also noticed that for the Intel processor, which adopts dynamic voltage and frequency scaling technique, the power consumption is not linear to the CPU utilization level, but rather step-like with significant power changes. Whilst for the PandaBoard, a linear model fits well with the power consumption. Finally, we utilized certain monthly cost model of data centers to analyze the cost-efficiency of data centers built from ARM clusters and from Intel workstations. We concluded that ARM cluster based data centers are advantageous in computationally lightweight applications. When it comes to computation-intensive applications, the advantages of ARM cluster diminish progressively.

In the future, we will use more advanced hardware than the current PandaBoards to make the experiments closer to real-world environment. For example, replace the SD card with an HDD or SSD disk, use the state-of-the-art Cortex A15 processor, and perform simple application-level integration for the development boards.

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