TwinLiteNet$^+$: An Enhanced Multi-Task Segmentation Model for Autonomous Driving

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Abstract

Semantic segmentation is a fundamental perception task in autonomous driving, particularly for identifying drivable areas and lane markings to enable safe navigation. However, most state-of-the-art (SOTA) models are computationally intensive and unsuitable for real-time deployment on resource-constrained embedded devices. In this paper, we introduce TwinLiteNet$^+$, an enhanced multi-task segmentation model designed for real-time drivable area and lane segmentation with high efficiency. TwinLiteNet$^+$ employs a hybrid encoder architecture that integrates stride-based dilated convolutions and depthwise separable dilated convolutions, balancing representational capacity and computational cost. To improve task-specific decoding, we propose two lightweight upsampling modules-Upper Convolution Block (UCB) and Upper Simple Block (USB)-alongside a Partial Class Activation Attention (PCAA) mechanism that enhances segmentation precision. The model is available in four configurations, ranging from the ultra-compact TwinLiteNet$^+_{\text{Nano}}$ (34K parameters) to the high-performance TwinLiteNet$^+_{\text{Large}}$ (1.94M parameters). On the BDD100K [1] dataset, TwinLiteNet$^+_{\text{Large}}$ achieves 92.9% mIoU for drivable area segmentation and 34.2% IoU for lane segmentation-surpassing existing state-of-the-art models while requiring $11\times$ fewer floating-point operations (FLOPs) for computation. Extensive evaluations on embedded devices demonstrate superior inference speed, quantization robustness (INT8/FP16), and energy efficiency, validating TwinLiteNet$^+$ as a compelling solution for real-world autonomous driving systems. Code is available at https://github.com/chequanghuy/TwinLiteNetPlus.

Keywords: Self-Driving Car, Lane segmentation, Drivable segmentation, BDD100K, Light-weight model, Embedded devices

1. Introduction

The emergence of deep learning methodologies has driven significant growth in the field of autonomous vehicles, where visual perception plays a central role. Among various sensors, cameras remain the most cost-effective and offer high-resolution RGB data for scene understanding. Compared to LIDAR and Radar, which provide depth but are costly and color-insensitive, cameras offer a practical trade-off between cost computation and semantic detail. As a result, camera-based perception has become a dominant focus in the development of real-time driving systems, particularly those powered by convolutional neural networks.

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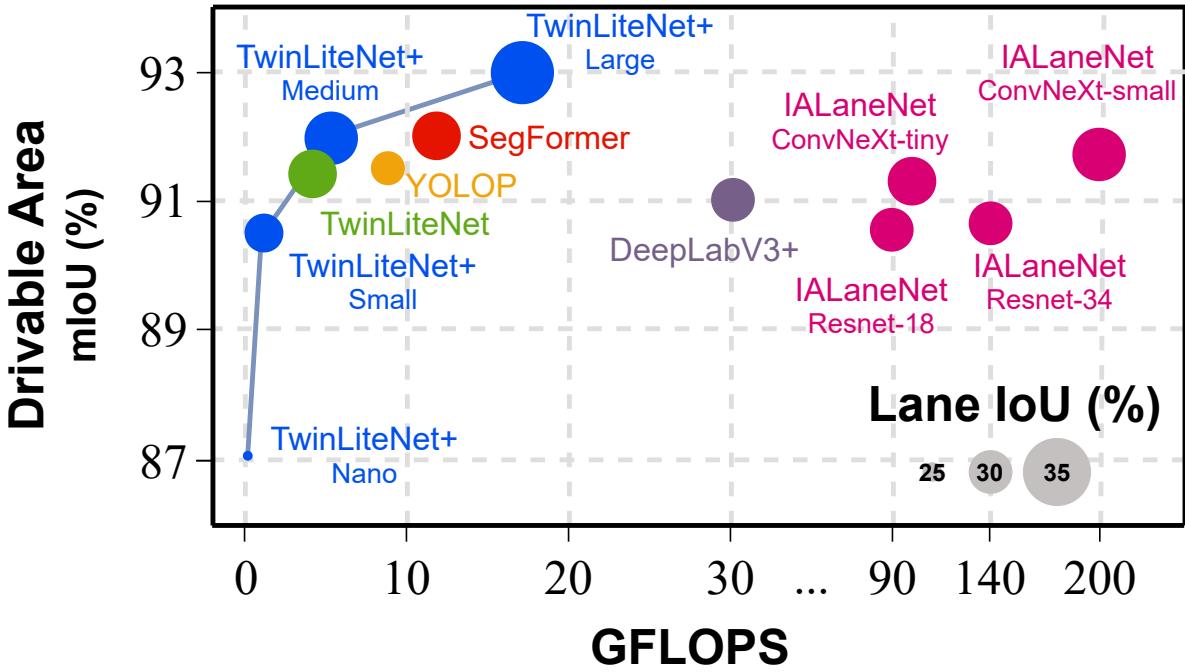
Figure 1: Comparison of evaluation metrics mIoU (%) (for Drivable Area Segmentation) - IoU (%) (for Lane Segmentation) - GFLOPs of various models on the BDD100K dataset. The x-axis represents the number of GFLOPs of the model, the y-axis represents the mIoU (%) for the Drivable Area Segmentation task, and the radius of the circle indicates the IoU (%) for the Lane Segmentation task (the larger the radius, the higher the accuracy).

In Advanced Driver Assistance Systems (ADAS) [2, 3, 4], camera-based panoptic driving perception serves as a critical component. By capturing comprehensive semantic information about the surrounding environment from images, vehicles can make optimal driving decisions. Prior studies [5, 6, 7, 8, 9, 10, 11, 12] have highlighted that segmentation plays a fundamental role in enabling ADAS to react promptly and accurately. Specifically, (1) *Drivable area segmentation* identifies regions where the vehicle can safely operate, thereby supporting precise control decisions. (2) *Lane segmentation* provides detailed insights into lane structure and positioning, assisting the vehicle in maintaining or changing lanes safely. While models are trained on large-scale datasets [13, 14, 15, 16, 17, 18] such as Cityscapes [19] offer detailed scene-level semantic labels, their granularity is often less relevant for immediate control decisions. In contrast, directly segmenting drivable regions and lanes provides more targeted and operationally helpful outputs for autonomous navigation.

Recent research has increasingly shifted from single-task models [5, 6, 7, 8, 9] to multi-task learning models [10, 11, 12], which aim to address multiple segmentation tasks concurrently. These models exploit shared encoder representations to reduce computational redundancy while maintaining task-specific decoder branches to preserve accuracy. However, achieving high performance often needs architectural complexity models, which may be impossible in real-world deployment. Despite being designed for real-time applications, many existing multi-task approaches [10, 20, 21, 22] are evaluated primarily on high-end GPUs, ignoring the strict constraints posed by embedded systems-such as limited processing power, energy efficiency, and memory capacity.

In this work, we introduce TwinLiteNet$^+$, a model tailored for real-time operation with optimal power consumption and hardware resources, proficient in simultaneously segmenting lanes and drivable areas. This model demonstrates competitive precision compared to models with similar tasks. There are four principal contributions of our research:

- We introduce TwinLiteNet$^+$, a lightweight and computation-efficient multi-task model designed for drivable area and lane segmentation. The encoder leverages a hybrid design of stride-based dilated convolutions and depthwise dilated separable convolutions to balance receptive field size and computational cost. In the decoder, we introduce Upper Convolution Block (UCB) and Upper Simple Block (USB) modules, which enhance upsampling efficiency without introducing heavy computation, making the architecture suitable for real-time inference.

- TwinLiteNet$^+$ is implemented in four configurations-Nano, Small, Medium, and Large-ranging from just 0.03M parameters / 0.57 GFLOPs (Nano) to 1.94M parameters / 17.58 GFLOPs (Large). This range of configurations enables flexible deployment across devices with varying computational capabilities, from ultra-low-power embedded systems to higher-end edge devices.

- Experimental results on the BDD100K dataset show that TwinLiteNet$^+_{\text{Large}}$ achieves 92.9% mIoU for drivable area segmentation and 34.2% IoU for lane segmentation, outperforming state-of-the-art lightweight models while maintaining low model complexity.

- We deploy TwinLiteNet$^+$ on real-world embedded devices such as NVIDIA Jetson TX2 and Jetson Xavier, demonstrating real-time inference performance with low latency and efficient energy consumption. Furthermore, we show that the model is highly robust under INT8 and FP16 quantization settings.

The remainder of the paper is represented as follows: We evaluate relevant models in Section 2 to grasp the benefits and drawbacks in the tasks of Drivable Area Segmentation, and Lane Segmentation with Multi-task approaches. The proposed TwinLiteNet$^+$ presents an architecture with methods to boost model performance in Section 3. In Section 4, we conduct experiments on the BDD100K dataset, and the results show that our TwinLiteNet$^+$ models outperform on latency and power efficiency. In the final Section, we provide some conclusions and future development directions.

2. Related Work

2.1. *Semantic Segmentation for autonomous driving*

Semantic segmentation is a fundamental subfield in computer vision that aims to assign a class label to each pixel in an input image. Unlike tasks such as image classification or object detection, semantic segmentation provides fine-grained information by precisely identifying the shape and boundaries of each object within a scene. Research in this area has primarily focused on scene understanding [13, 14, 15, 16, 17, 18, 23], with models typically trained and evaluated on densely annotated datasets such as Cityscapes [19]. Modern segmentation models are often built upon deep learning architectures and further enhanced through the integration of attention modules [24, 25, 26, 27], which help the model focus on informative regions and improve spatial representation learning. Although these approaches have achieved high performance in modeling complex scene contexts, they are not well suited for real-time applications such as autonomous driving, where computational efficiency are critical. In such scenarios, a more practical approach is to focus on task-relevant functional regions-such as drivable areas and lane segmentation-to enable timely and reliable driving decisions.

2.1.1. *Signle-task Approaches*

Drivable area segmentation enables models to identify navigable regions of the road directly. Several existing approaches [8, 7] handle the drivable area as a single unified class, encompassing both direct and alternative drivable areas. In contrast, more advanced models [28, 29, 30, 31, 32, 33] have demonstrated the ability to distinguish between direct and alternative areas when trained on comprehensive datasets such as BDD100K, thereby offering a more understanding of the drivable space. However, segmenting the road into fine-grained components such as individual lanes-particularly differentiating between vertical lanes and parallel lanes (e.g., stop lines, crosswalks)-requires lane detection models. Parashar et al.[9] proposed Spatial CNN (SCNN) with a new neural network architecture by generalizing traditional deep layer-by-layer to slice-by-slice convolution in feature mapping, allowing information to propagate across pixels along rows and columns within a layer despite time-consuming. On the other hand, Enet-SAD [6] utilizes a self-attention-guided filter method to assist low-level feature maps in learning from high-level feature maps, or recently, road marking methods [34, 35, 36, 37] has also brought much attention from the community. A novel detector CLRerNet [38] along with a proposed LaneIoU metric are presented to improve the confidence score further.

Although previous research highlighted the initial success of models in the single-task domain, the advantage of leveraging a model to address multiple tasks has led to recent studies demonstrating that a multi-task strategy is more appropriate for real-world applications, particularly when deployed on devices with limited computing capabilities, such as embedded systems. This method allows models to strike a balance between efficiency and complexity while concurrently performing two tasks: segmentation of the driver's area and lane segmentation. Motivated by these advantages, we propose a multi-task architecture with a shared encoder and dual decoders, targeting both drivable area and lane segmentation tasks simultaneously.

2.2. *Multi-task Approaches*

In recent years, multi-task learning has gained considerable attention in autonomous driving, particularly for jointly addressing segmentation-related tasks such as drivable area segmentation, lane segmentation, and scene parsing. By leveraging shared representations among these spatially correlated tasks, multi-task frameworks can improve model generalization while significantly reducing computational overhead-an essential consideration for real-time applications. The availability of large-scale datasets such as BDD100K [1] and NYUv2 [39] has further accelerated research in this direction, enabling the development and benchmarking of various segmentation-based multi-task models. Several studies extend to auxiliary segmentation tasks, combining semantic segmentation with scene classification [40, 31] or depth estimation [41, 42] to enhance environmental understanding. Others have adopted dual-task configurations, such as jointly performing drivable area and lane segmentation [12, 11, 10, 43, 16, 15, 44], which are critical for navigation and path planning.

Among prior multi-task segmentation approaches, some methods [15, 16] repurpose single-task segmentation backbones and adapt them to multi-task settings. At the same time, [43, 44] are initially designed for joint detection and segmentation, yet provide segmentation-only configurations. However, these models are not optimized explicitly for segmentation synergy, often resulting in limited performance for multi-task segmentation. In contrast, models like IALaneNet [10] explicitly focus on inter-task feature fusion using attention mechanisms at the task level. These methods demonstrate improved cooperation between segmentation branches but are limited by complex architectures and high computational costs, making them less suitable for real-time or embedded deployment. To address the limitations of practical deployment, lightweight models such as Twin-LiteNet and BILane [12, 11] have been proposed. TwinLiteNet, with only 0.4M parameters, is

optimized for real-time inference on embedded platforms, though its shallow decoder constrains performance in challenging lane scenarios. BILane [11] improves upon this with boundary-aware and interactive attention modules in a compact 1.4M-parameter design. However, its segmentation accuracy remains not as strong compared to TwinLiteNet despite using approximately 3.5 times more parameters and relying on higher input image resolution. These works clearly show a trade-off between segmentation accuracy and inference speed. This motivates the need for a multi-task segmentation model that can balance accuracy and efficiency.

Inspired by TwinLiteNet [12], the proposed TwinLiteNet$^+$ introduces a more powerful yet efficient architecture by enhancing both the encoder and decoder. The decoder is improved with additional convolutional layers after transposed convolutions to reconstruct fine-grained features better, while the encoder is designed to optimize computational efficiency without compromising feature extraction capability. Moreover, TwinLiteNet$^+$ comes in four scalable configurations, enabling flexible deployment across a wide range of hardware platforms-from high-performance GPUs to resource-constrained embedded systems.

2.3. *Optimizing Deep Learning Deployment on Embedded Devices*

In recent years, deploying deep learning models on embedded devices has attracted considerable attention within the artificial intelligence community. The computation on these devices is distinguished by its ability to execute processes directly on units that are both cost-effective and task-specific. Despite this advantage, such capabilities are constrained by significant limitations in terms of computational power and storage capacity, presenting substantial challenges for the deployment of deep learning models on these platforms. To address these limitations, several model compression techniques have been proposed, such as 8-bit quantization [45], pruning [46], and knowledge distillation [47]. Among these, quantization is widely favored for its simplicity and hardware-friendliness. It reduces model precision to lower bit widths (e.g., INT8 or FP16), significantly decreasing memory usage and inference latency. Post-training quantization (PTQ) allows models trained in 32-bit floating-point to be quantized without retraining, whereas quantization-aware training (QAT) simulates quantization effects during training and typically yields higher accuracy. In contrast, pruning requires careful exploration of pruning schedules and sensitivity analysis across layers, often requiring iterative retraining to restore accuracy. This process is time-consuming and highly dependent on manual tuning or costly search algorithms, and it may not be generalized well across architectures. Similarly, knowledge distillation introduces a complex teacher-student training pipeline where a compact model (student) is trained to mimic the output distribution of a larger pre-trained model (teacher). This multi-stage training not only adds overhead but also does not offer guarantees about interpretability or alignment with the original model's decision boundaries.

Howard et al. introduce MobileNet [48], a class of efficient neural network architectures tailored for embedded and mobile vision applications, leveraging depthwise separable convolutions to reduce both parameter count and computational complexity significantly. Based upon this foundation, some studies have shown that depthwise dilated separable convolutions outperform standard dilated convolutions in classification tasks, achieving 67.9% accuracy with only 123M FLOPs-compared to 69.2% accuracy with 478M FLOPs using standard dilation-highlighting that the latter offers only marginal gains in accuracy at nearly 4× the computational cost. Beyond architectural improvements, numerous model compression and optimization strategies have been proposed for low-resource deployment [49, 50]. Frameworks such as TensorFlow Lite, TensorRT, NCNN, and MNN [51] have played a pivotal role in facilitating deployment by supporting quantization, operator fusion, and backend-specific accelerations.
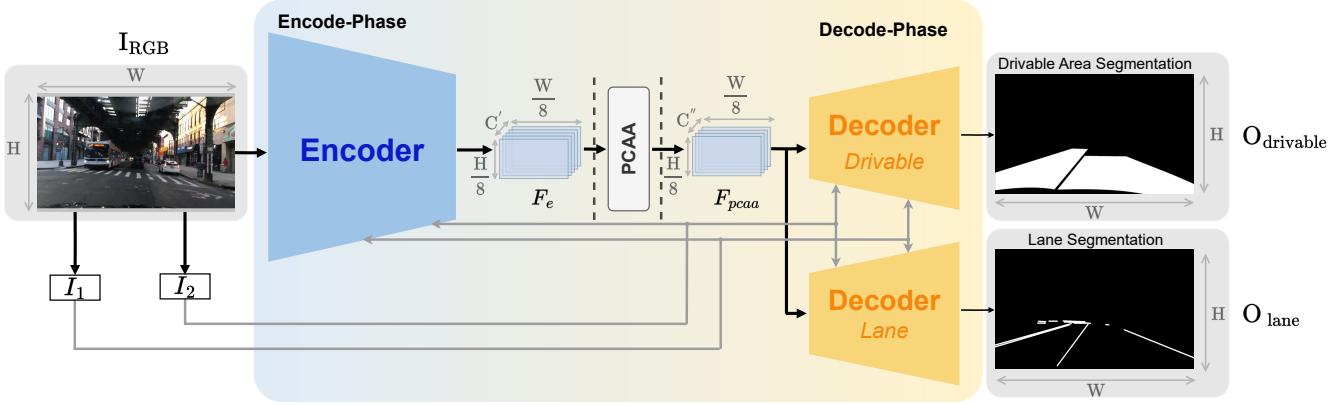
Figure 2: The TwinLiteNet$^+$ architecture comprises two phases. During the Encode phase, the input image passes through an Encoder block followed by a Partial Class Activation Attention mechanism. In the Decode phase, the output from the Encoder is channeled through two identical yet independent Decoder blocks, transforming the feature maps into two separate segmentation maps.

Despite significant progress, achieving an optimal trade-off between accuracy, latency, and computational efficiency remains a persistent challenge-especially in real-time applications. While state-of-the-art models often attain impressive accuracy, their deployment on resource-constrained devices is limited by substantial latency and memory overhead. This trade-off is particularly critical in embedded and edge scenarios, where computational resources are inherently limited. In this study, we introduce a computation-efficient model specifically designed for deployment on such low-computation devices without resorting to architecture search techniques like pruning or additional training procedures such as knowledge distillation. Instead, the proposed model exhibits strong performance under low-precision inference settings, made possible through model compression via quantization (Sec. 4.5). Our architecture integrates a carefully optimized combination of dilated convolutions and depthwise separable convolutions within the encoder, balancing representational capacity and computational efficiency. This design not only preserves high segmentation accuracy but also achieves low inference latency, rendering it well-suited for real-time deployment in practical environments.

3. Proposed method

This paper introduces TwinLiteNet$^+$, a model specifically engineered for segmenting drivable areas and lanes. Inspired by the preceding TwinLiteNet [12], our study aims to enhance the model by refining both the encoder and decoder components. In particular, the proposed decoder is designed to effectively leverage information compared to its predecessor while still maintaining a low computational resource utilization. Moreover, the encoder integrates depthwise dilated separable convolutions, thereby optimizing the inference time of the model which is suitable for real-time implementation. TwinLiteNet$^+$ operates in two primary phases: the Encode-phase and the Decode-phase, incorporating a Partial Class Activation Attention (PCAA) module [26] which enhances segmentation precision and efficiency by focusing on key areas like drivable zones and lanes. While several attention mechanisms such as DANet [24], SE [25], and CBAM [27] have been proposed to enhance feature representations by modeling spatial and/or channel-wise dependencies, they typically rely on global feature statistics or self-attention across the entire feature map without explicitly incorporating semantic class information. In contrast, PCAA generates attention maps guided by partial class activation maps, which embed category-level semantics. This enables
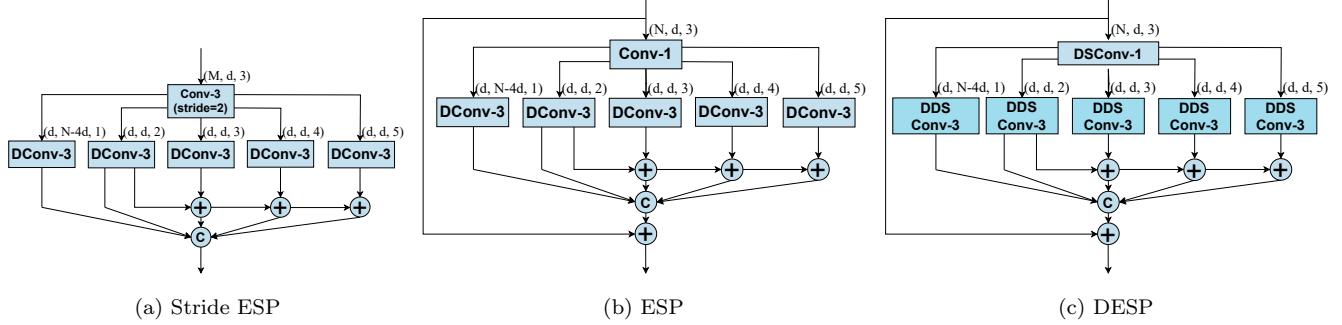
Figure 3: This figure presents variants of ESP blocks within the Encoder. The convolutional layers are designated as Conv-n (standard $n \times n$ convolution), DConv-n ($n \times n$ dilated convolution) in Stride ESP (Fig 3a) and ESP (Fig 3b), and DSConv-n ($n \times n$ depthwise separable convolution), DDSConv-n ($n \times n$ depthwise dilated separable convolution) in Stride DESP (Fig 3c), and are described in terms of (*input channels*, *output channels*, *dilation level*), where $dilation\ rate = 2^{dilation\ level - 1}$. These blocks consolidate feature maps employing a Hierarchical Feature Fusion (HFF)[17], which is notable for its computational efficiency and its ability to eliminate grid-like artifacts resulting from dilated convolutions. The Stride ESP (a) not only accomplishes downsampling but also converts the depth of the feature map from M to N, whereas ESP (Fig 3b) and DESP (Fig 3c) maintain the original dimensions of the feature map. The main difference between the ESP and DESP modules lies in the use of depthwise dilated separable convolution (DDSConv-n) layers in DESP instead of dilated convolution (DConv-n). In this design, each depthwise dilated separable convolution layer applies depthwise dilated convolutions with different *dilation rate* to extract spatial features, followed by a pointwise convolution to fuse information across channels.

PCAA to focus selectively on regions relevant to specific classes, offering both strong discriminative capability and high computational efficiency.

In the Encoding stage, the model processes the input image $\mathbf{I}_{\text{RGB}} \in \mathbb{R}^{3 \times H \times W}$ using a shared-weight Encoder block, designed to extract pertinent image features. This block leverages an extended receptive field provided by dilated convolutions, combined with the low computational demand yet high efficiency of Depthwise Convolution, thereby enhancing the model's performance while maintaining low latency. The Encoder's output $\mathbf{F}_{\text{e}} \in \mathbb{R}^{C' \times \frac{H}{8} \times \frac{W}{8}}$ is processed by the PCAA mechanism, emphasizing key features, particularly of drivable areas and lanes. PCAA operates by collecting local class representations based on partial Class Activation Maps (CAMs) and calculating pixel-to-class similarity maps within patches, a significant approach for advancing the precision and effectiveness of semantic segmentation models. Following this, a feature map $\mathbf{F}_{\text{pcaa}} \in \mathbb{R}^{C'' \times \frac{H}{8} \times \frac{W}{8}}$ is channeled into two separate Decoder blocks, each tasked with specific prediction objectives. The output of these blocks yields segmentation maps for Drivable Area Segmentation and Lane Segmentation, represented as $\mathbf{O}_{\text{drivable}}, \mathbf{O}_{\text{lane}} \in \mathbb{R}^{2 \times H \times W}$. The simple feed-forward process is outlined in Algorithm 1. The model's training integrates both Focal [52] and Tversky loss [53] functions. TwinLiteNet$^+$ is available in four configurations: Nano, Small, Medium to Large, offering adaptability based on the computational power of the underlying hardware. The comprehensive architecture of TwinLiteNet$^+$ is depicted in Figure 2.

3.1. *Encoder*

In the development of the TwinLiteNet$^+$ model, we innovate an efficient and computationally cost-effective encoder, consisting of a series of convolutional layers designed for extracting features from input images. This encoder draws inspiration from the ESPNet encoder [17], a modern and efficient network for segmentation tasks. The cornerstone of the ESPNet architecture is the ESP module, depicted in Figure 3b. The ESP unit initially projects the high-dimensional input feature map into a lower-dimensional space using point-wise convolutions (or 1×1 convolutions), subse-
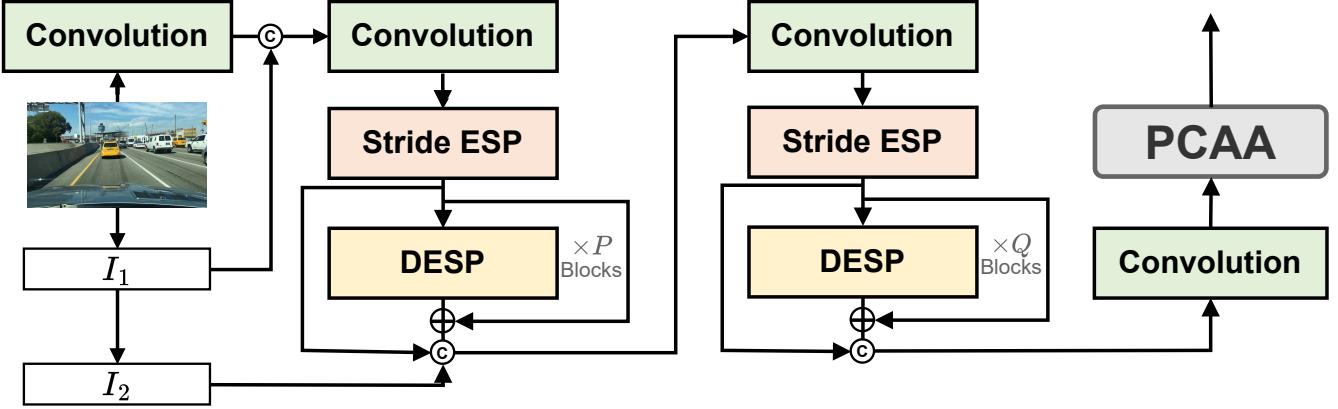
Figure 4: Comprehensive schematic of the Encoder in TwinLiteNet$^+$.

quently learning parallel representations via dilated convolutions with varying dilation rates. This differs from the use of standard convolutional kernels. The ESP module undergoes several stages, including Reduce, Split, Transform, and Merge, with its detailed implementation illustrated in Figure 3. For computations with the ESP module, the feature map first undergoes down-sampling in the Stride ESP block, where point-wise convolutions are replaced with n×n stride convolutions within the ESP module to enable nonlinear down-sampling operations, shown in Figure 3a. The spatial dimensions of the feature map are altered through down-sampling operations, changing from $\mathbf{F}_{in} \in \mathbb{R}^{M \times H' \times W'} \to \mathbf{F}_0 \in \mathbb{R}^{N \times \frac{H'}{2} \times \frac{W'}{2}}$. The ESP module in ESPNet iterates output of Stride ESP to increase the network's depth, transforming $\mathbf{F}_{i-1} \in \mathbb{R}^{N \times \frac{H'}{2} \times \frac{W'}{2}} \to \mathbf{F}_i \in \mathbb{R}^{N \times \frac{H'}{2} \times \frac{W'}{2}}$. During this phase, the feature map maintains its size and depth, thus the input and output feature maps of the ESP module are combined using element-wise summation to enhance information flow. The ESP and Stride ESP modules are followed by Batch Normalization [54] and PReLU [55] nonlinearity. The final output, $\mathbf{F}_{out} \in \mathbb{R}^{2N \times \frac{H'}{2} \times \frac{W'}{2}}$, is obtained through a concatenation operation between F_0 and F_N, effectively expanding the feature map's dimensions. This process is detailed in Equation 1.

$$\begin{cases} \mathbf{F}_0 = \text{StrideESP}(\mathbf{F}_{in}) \\ \mathbf{F}_i = \text{ESP}(\mathbf{F}_{i-1}) + \mathbf{F}_{i-1}, \quad i \in [1, N] \\ \mathbf{F}_{out} = Concat(\mathbf{F}_0, \mathbf{F}_N) \end{cases} \quad (1)$$

As previously addressed in Section 2.3, while standard dilated convolutions achieve enhanced

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Algorithm 1: Feedforward process of TwinLiteNet$^+$

Input: The input image $\mathbf{I}_{RGB}$ and two downsampled image $\mathbf{I}_1$ and $\mathbf{I}_2$ ▷ $\mathbf{I}_1$ and $\mathbf{I}_2$ are downsampling images derived from equations 3 and 4, respectively.

Output: Drivable Area Segmentation Map $\mathbf{O}_{drivable}$ and Lane Segmentation Map $\mathbf{O}_{lane}$

1: $\mathbf{F_e} \leftarrow \text{Encoder}(\mathbf{I}_{RGB}, \mathbf{I}_1, I_2)$
2: $\mathbf{F}_{pcaa} \leftarrow \text{PCAA}(F_e)$
3: $\mathbf{O}_{drivable} \leftarrow \text{Decoder}_{drivable}(\mathbf{I}_{pcaa}, \mathbf{I}_1, \mathbf{I}_2)$
4: $\mathbf{O}_{lane} \leftarrow \text{Decoder}_{lane}(\mathbf{I}_{pcaa}, \mathbf{I}_1, \mathbf{I}_2)$
5: **return** $\mathbf{O}_{lane}, \mathbf{O}_{drivable}$

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accuracy, they also bear significantly higher computational costs compared to their depthwise separable counterparts. So, in the TwinLiteNet$^+$ model, we propose using Depthwise ESP (DESP) as an alternative to the ESP module, while maintaining the Stride ESP module. The DESP is adeptly engineered to substitute standard dilated convolutional layers with depthwise separable dilated convolutional layers. This proposed approach preserves the efficacy of the Stride ESP module while markedly reducing computational expenses by substituting the ESP module with DESP, as depicted in Figure 3c. For instance, in a feature map sized $64 \times 180 \times 320$, the DESP algorithm necessitates learning merely 2,332 parameters, incurring a computational cost of 0.14 GFLOPs. Conversely, the ESP algorithm requires learning a considerably greater number of parameters, amounting to 7,872, with a related computational cost of 0.46 GFLOPs. In our proposed model, the ESP module is iterated many times. Using DESP to replace ESP reduces the model's parameters and computational costs. The computational procedures of the Stride ESP and DESP blocks are executed as outlined in Eq. 2.

$$
\begin{cases}
\mathbf{F}_0 = \text{StrideESP}(\mathbf{F}_{\text{in}}) \\
\mathbf{F}_i = \text{DESP}(\mathbf{F}_{i-1}) + \mathbf{F}_{i-1}, \quad i \in [1, N] \\
\mathbf{F}_{out} = Concat(\mathbf{F}_0, \mathbf{F}_{\text{N}})
\end{cases}
\tag{2}
$$

Moreover, our encoder block introduces efficient long-range shortcut connections between the input image and the current downsampling unit, thereby enhancing the encoding of spatial relationships and facilitating more effective representation learning. These connections initially downsample the image to align with the feature map dimensions using Average Pooling. Our encoder block consists of two downsampled images, $\mathbf{I}_1 \in \mathbb{R}^{3 \times \frac{H}{2} \times \frac{W}{2}}$ and $\mathbf{I}_2 \in \mathbb{R}^{3 \times \frac{H}{4} \times \frac{W}{4}}$ (Eqs. $3 - 4$). Figure 4 depicts the proposed Encoder Block in detail. Our Stride ESP and DESP modules are cohesively integrated via convolutional layers, succeeded by batch normalization [54] and PReLU non-linearity [55]. In the Encoder model, two computations are performed by combining Stride ESP and DESP blocks as calculated in Eq. 2. In the first calculation, after the Stride ESP block computes the solution, the DESP block will execute $\mathbf{P}$ times instead of N. After executing the DESP blocks, the final output is concatenated with the output of Stride ESP and $\mathbf{I}_2$ before being sent to the following calculation phase. Meanwhile, the DESP blocks in the second calculation are executed similarly to the first calculation, with the DESP blocks being executed $\mathbf{Q}$ times, and the final output when executing the DESP blocks is concatenated with the Stride ESP in the same calculation. The hyperparameters $\mathbf{P}$ and $\mathbf{Q}$ are determined based on the selected model config, and further specifics are delineated in Section 3.3.

$$
\mathbf{I}_1 = AvgPool(\mathbf{I}_{\text{RGB}})
\tag{3}
$$

$$
\mathbf{I}_2 = AvgPool(AvgPool(\mathbf{I}_{\text{RGB}}))
\tag{4}
$$

3.2. Decoder

In our TwinLiteNet$^+$ architecture, we implement an innovative approach by deploying multiple decoding modules, each tailored for a distinct segmentation task. This design deviates from conventional methods that typically depend on a singular output for all object categories, with the tensor output encompassing $C+1$ channels, corresponding to C classes and one additional channel for the background. Specifically, the post-processing feature map obtained from PCAA denoted as $\mathbf{F}_{pcaa} \in \mathbb{R}^{C'' \times \frac{H}{8} \times \frac{W}{8}}$, our architecture employs two separate yet structurally identical decoding
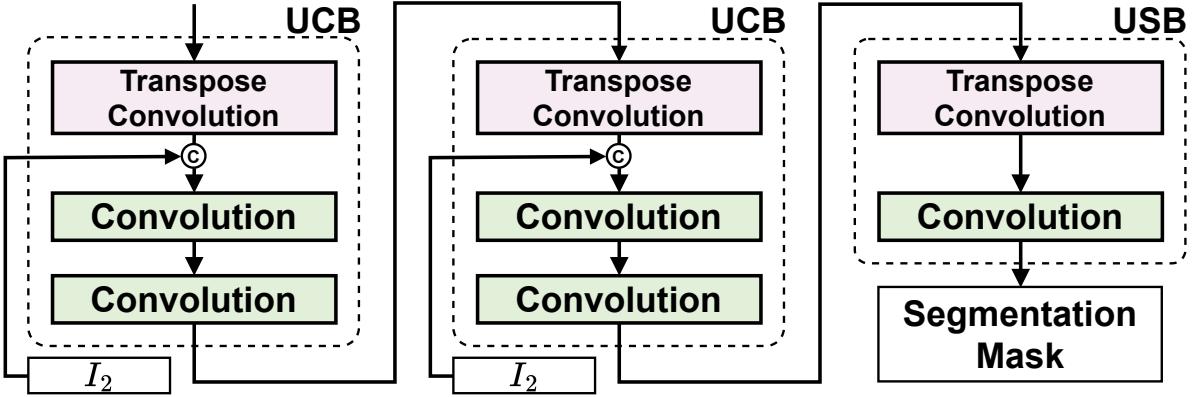
9

Figure 5: Decoder Block Design in TwinLiteNet$^+$. This illustrates the implementation of Upper Convolution Block (UCB) and Upper Simple Block (USB) within the decoder, specifically tailored for upsampling to generate segment maps for diverse tasks.

blocks. These blocks independently handle the segmentation of distinct regions and drivable lanes. Our decoder effectively reduces the depth of the feature map and employs upsampling techniques. The upsampling process within the decoder is facilitated by a combination of Transpose Convolution and Convolution operations. We introduce two novel blocks, namely the Upper Convolution Block (UCB) and Upper Simple Block (USB), both elegantly designed for upsampling purposes. The UCB comprises a Transpose Convolution followed by two subsequent Convolution operations, wherein the post-Transpose Convolution features are concatenated with the input image at a lower resolution, either I_1 or I_2. Conversely, the USB incorporates a single Transpose Convolution and one Convolution, without merging input image information, and its output constitutes the segment map as predicted by the model. We apply batch normalization and PReLU following each Transpose Convolution or Convolution layer. Integrating a Convolution layer immediately subsequent to a Transpose Convolution significantly enhances the feature learning capabilities of the Decoder, thereby facilitating the restoration of resolution lost during the downsampling process in the encoder. The detailed architecture of our model's Decoder Block is depicted in Figure 5. We have strategically designed our decoder to be simplistic, thereby ensuring minimal computational overhead for the model. The sequential application of the blocks $UCB \rightarrow UCB \rightarrow USB$ leads to a systematic change in the feature map dimensions from $\frac{H}{8} \times \frac{W}{8} \rightarrow \frac{H}{4} \times \frac{W}{4} \rightarrow \frac{H}{2} \times \frac{W}{2} \rightarrow H \times W$ for each targeted task. This modular, branched approach allows for the independent tuning of each task, facilitating the creation of optimal conditions for refining specific segmentation outcomes for various regions and drivable lanes. As a result, our model effectively differentiates and enhances features relevant to each segmentation task, culminating in an output resolution of $\mathbf{O} \in \mathbb{R}^{2 \times H \times W}$.

3.3. Model configurations

To ensure versatility and broad applicability across diverse hardware devices, we design our TwinLiteNet$^+$ model with four configurations: *Nano*, *Small*, *Medium*, and *Large*. These variants, denoted as TwinLiteNet$^+_{\text{Nano}}$, TwinLiteNet$^+_{\text{Small}}$, TwinLiteNet$^+_{\text{Medium}}$, and TwinLiteNet$^+_{\text{Large}}$, differ primarily in the number of convolutional filters and the structural hyperparameters $\mathbf{P}$ and $\mathbf{Q}$, while preserving the overall encoder-decoder architecture. This configuration hierarchy allows for a flexible trade-off between performance and computational cost. Specifically, the Nano version contains only 0.03 million parameters and requires 0.57 GFLOPs, making it highly suitable for ultra-low-power edge devices. In contrast, the Large version reaches 1.94 million parameters and 17.58 GFLOPs, offering improved accuracy at the cost of higher resource consumption. All con-

Table 1: Model architecture settings in different TwinLiteNet$^+$ model's configs: Nano, Small, Medium and Large.

Layer	Ouput Size	Output channels for TwinLiteNet$^+$			
		Nano	**Small**	**Medium**	**Large**
Conv	$\frac{H}{2} \times \frac{W}{2}$	4	8	16	32
Conv		8	16	32	64
Stride ESP		16	32	64	128
P $\times$ DESP	$\frac{H}{4} \times \frac{W}{4}$	16	32	64	128
Conv		32	64	128	256
Stride ESP		32	64	128	256
Q $\times$DESP		32	64	128	256
Conv	$\frac{H}{8} \times \frac{W}{8}$	16	32	64	128
PCAA		16	32	64	128
Conv		8	16	32	64
UCB$_{\text{drivable}}$ UCB$_{\text{lane}}$	$\frac{H}{4} \times \frac{W}{4}$	4	8	16	32
UCB$_{\text{drivable}}$ UCB$_{\text{lane}}$	$\frac{H}{2} \times \frac{W}{2}$	4	8	8	8
USB$_{\text{drivable}}$ USB$_{\text{lane}}$	$H \times W$	2	2	2	2
P, **Q**		1, 1	2, 3	3, 5	5, 7
#Param.		0.03M	0.12M	0.48M	1.94M
FLOPs		0.57G	1.40G	4.63G	17.58G

figurations share the same architectural stages but scale their complexity by adjusting the output channel widths at each stage. The encoder stages consist of stacked convolutional blocks with downsampling via Stride ESP and a repeated application of DESP determined by the hyperparameters **P** and **Q**, which control the depth and receptive field of the network. Table 1 provides a comprehensive overview of the architectural parameters and resource consumption across different model configurations.

This modular scaling strategy enables our model to adapt to varying deployment constraints without requiring changes in architecture design or retraining. In particular, the lightweight TwinLiteNet$^+_{\text{Nano}}$ proves highly effective in latency-sensitive applications, while the Medium and Large configurations deliver stronger performance in scenarios with more relaxed computational budgets.

3.4. *Loss Function*

To effectively address the specific challenges posed by pixel-wise classification in autonomous driving scenarios-particularly class imbalance and sensitivity to fine structural details-we employ a combination of Focal Loss [52] and Tversky Loss [53]. Each loss is applied independently to both segmentation heads to target complementary aspects of the task.

Focal Loss [52]: Designed to down-weight well-classified examples and focus learning on harder, misclassified pixels, Focal Loss is particularly beneficial in scenarios with significant class

imbalance-such as drivable area and lane segmentation, where background pixels dominate. For example, in lane segmentation, narrow foreground structures (i.e., lanes) are often underrepresented, making them prone to being overlooked by standard losses. Focal Loss addresses this by introducing a modulating factor $(1 - \hat{p}_i(c))^\gamma$ to the standard cross-entropy:

$$\mathcal{L}_{focal} = -\frac{1}{N} \sum_{c=0}^{C-1} \sum_{i=1}^{N} p_i(c)(1 - \hat{p}_i(c))^\gamma \log(\hat{p}_i(c)) \tag{5}$$

where, N is the number of pixels, $C = 2$ is the number of classes (foreground vs. background), $p_i(c)$ is the one-hot ground truth label for pixel i and class c, $\hat{p}_i(c)$ is the predicted probability, and γ is a focusing parameter (commonly set to 2) that reduces the impact of easy examples.

Tversky Loss [53]: An extension of Dice Loss [56], Tversky Loss introduces tunable parameters α and β to balance penalties on false positives and false negatives. This is particularly important in lane segmentation, where missing thin, elongated structures is more critical than predicting false positives. The formulation is:

$$\mathcal{L}_{tversky} = \sum_{c=0}^{C-1} \left(1 - \frac{TP(c)}{TP(c) + \alpha FN(c) + \beta FP(c)} \right) \tag{6}$$

where TP, FN, and FP denote true positives, false negatives, and false positives, respectively. Choosing $\alpha > \beta$ encourages the model to prioritize recall-an essential property for safety-critical applications like lane segmentation.

Total Loss: The total loss combines the drivable area and lane-specific losses:

$$\mathcal{L} = \mathcal{L}_{\text{drivable}} + \mathcal{L}_{\text{lane}} \tag{7}$$

Each sub-loss is a weighted combination of the Focal and Tversky losses applied to the corresponding output. Focal Loss mitigates class imbalance by encouraging the model to focus on harder pixels, while Tversky Loss enhances robustness in detecting thin structures by emphasizing recall. Together, they form a complementary loss framework that improves both the robustness and accuracy of segmentation in complex real-world driving environments.

4. Experimental

4.1. *Experiment Setup*

4.1.1. *Dataset*

The BDD100K [1] dataset was used for training and validating TwinLiteNet$^+$. With 100,000 frames and annotations for 10 tasks, it is a large dataset for autonomous driving. Due to its diversity in geography, environment, and weather conditions, the algorithm trained on the BDD100K dataset is robust enough to generalize to new settings. The BDD100K dataset is divided into three parts: a training set with 70,000 images, a validation set with 10,000 images, and a test set with 20,000 images. Since no labels are available for the 20,000 images in the test set, we choose to evaluate on a separate validation set of 10,000 images. We use data that is prepared similarly to several previous studies [6, 12] to ensure fairness in comparison.

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[1] https://bdd-data.berkeley.edu

Algorithm 2: Training and evaluation process for the proposed TwinLiteNet$^+$ model

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Input: Target end-to-end network F with parameters Θ; Training dataset τ_{train};
Validation dataset τ_{val}

1 Initialize the parameters Θ ;

2 for $epoch \leftarrow 1$ **to** $epochs$ **do**

3   **for** $each\ batch\ (x_{train}, y_{train})\ in\ \tau_{train}$ **do**

4 $y_{drivable}, y_{lane} \leftarrow y_{train}$;

5 $\hat{y}_{drivable}, \hat{y}_{lane} \leftarrow F(x_{train})$;

6 $\mathcal{L}_{drivable} \leftarrow \mathcal{L}_{drivable}^{focal} + \mathcal{L}_{drivable}^{tversky}$;

7 $\mathcal{L}_{lane} \leftarrow \mathcal{L}_{lane}^{focal} + \mathcal{L}_{lane}^{tversky}$;

8 $\mathcal{L} \leftarrow \mathcal{L}_{drivable} + \mathcal{L}_{lane}$;

9 $\Theta \leftarrow \arg\min_\Theta \mathcal{L}$;

10 $\Theta \leftarrow \text{Update}_{EMA}(\Theta)$;

11 $\hat{y}_{val} \leftarrow F(x_{val}; \Theta)$;

12 $mIoU_{drivable}, Acc_{lane}, IoU_{lane} \leftarrow Evaluate(\hat{y}_{val}, y_{val})$;

13 return $mIoU_{drivable}, Acc_{lane}, IoU_{lane}$

4.1.2. *Evaluation Metrics*

For the segmentation tasks, similar to the evaluation approach in [12, 11, 10], we assess the drivable area segmentation task using the mIoU (mean Intersection of Union) metric. In the context of lane segmentation, we measure the performance using both accuracy and IoU (Intersection over Union) metrics. However, owing to pixel imbalances between the background and foreground in lane segmentation, we opt for a more meaningful balanced accuracy metric in our evaluation. Traditional accuracy metrics may produce biased results by favoring classes with a larger number of samples. In contrast, balanced accuracy provides a fairer assessment by considering the accuracy for each class. We use the accuracy metrics provided in the study [57]. To evaluate computational efficiency, we assess the model using two standard metrics: parameters and FLOPs. In line with established conventions in the field [58, 17], we use FLOPs as the total number of multiply-add operations needed for inference.

4.1.3. *Implementation details*

To improve performance, we apply several data augmentation techniques. To address photometric distortions, we modify the hue, saturation, and value parameters of the image. In addition, we also incorporate basic enhancement techniques to handle geometric distortions such as random translation, cropping, and horizontal flipping. We train our model using the AdamW [59] optimizer with a learning rate of 5×10^{-4}, momentum of 0.9, and weight decay of 5×10^{-4}. In our TwinLiteNet$^+$, we use Exponential Moving Average (EMA) model [60] purely as the final inference model. Additionally, we resize the original image dimensions from 1280×720 to 640×384. For the loss function coefficients, we set $\alpha = 0.7$ and $\beta = 0.3$ for $\mathcal{L}_{drivable}^{tversky}$, $\alpha = 0.9$ and $\beta = 0.1$ for $\mathcal{L}_{lane}^{tversky}$, and $\alpha_t = 0.25$ and $\gamma = 2$ in $\mathcal{L}_{drivable,lane}^{focal}$. All of the specified configurations are developed based on empirical evidence. Finally, we conduct training with a batch size of 16 on an RTX A5000 for 100 epochs. The model training and evaluation process is described in Algorithm 2. During the model training process, we simultaneously train both tasks and employ EMA technique for weight updates following each backpropagation step. After each epoch, we evaluate the model on the validation set and focus on three key metrics: mean Intersection over Union for the Drivable Area

Segmentation task (mIoU), Lane Accuracy (Acc), and Intersection over Union (IoU) for the Lane Segmentation task. All experiments used the PyTorch framework on an NVIDIA GeForce RTX A5000 GPU with 32GB of RAM and an Intel(R) Core(TM) i9-10900X processor.

4.2. Main results

4.2.1. Cost Computation Performance

Table 2: Comparison between TwinLiteNet$^+$ Model's configs in FPS (in 5 different batch sizes), Parameters, FLOPs and Model size. (Parameters and FLOPs represent the number of parameters and the number of floating point operations required in each model, FPS shows the model's latency when inference.

Config	FPS (with Batch Size) ↑					#Param. ↓	FLOPs ↓ (batch=1)	Model Size ↓
	1	2	4	8	16			
Nano	237	470	921	1004	1163	0.03M	0.57G	0.06MB
Small	178	340	697	732	779	0.12M	1.40G	0.23MB
Medium	138	269	442	456	484	0.48M	4.63G	0.92MB
Large	109	186	218	220	237	1.94M	17.58G	3.72MB

Table 2 presents the computational cost outcomes of various configs of the TwinLiteNet$^+$ model. The parameters include the number of parameters (#Param.), and FLOPs indicating the computation required per inference (with a batch size of 1), along with the model's size. Frame rate (FPS) is measured across different batch sizes (1, 2, 4, 8, 16) to assess latency during inference. The results were obtained while doing inference with PyTorch FP32 (without TorchScript, or TensorRT). Results show that TwinLiteNet$^+_{Nano}$ is the lightest config with only 0.03M parameters and 0.57G FLOPs, achieving an impressive inference speed of up to 1163 FPS with a batch size of 16. Inference with larger batch sizes opens up the potential for simultaneous inference across multiple cameras, a critical capability for autonomous vehicle applications. However, transitioning from the Nano to the Large config, the parameters increase up to 1.94M and FLOPs to 17.58G, indicating a more powerful computational capability but also resulting in an increase in latency, with inference speed dropping to 237 FPS. The trade-off between accuracy and latency is evident: larger models offer higher computational potential but require more processing time. This highlights the importance of carefully balancing the need for accuracy and real-time requirements when selecting a model for specific applications.

4.2.2. Drivable Area Segmentation & Lane Detection Result

We evaluate the performance of our TwinLiteNet$^+$ models versus state-of-the-art multitask models that jointly address drivable area segmentation and lane segmentation. For a fair comparison, we exclude single-task models and those incorporating additional tasks such as object detection. Table 3 summarizes the results along with computational complexity (FLOPs) and model size (number of parameters).

The original TwinLiteNet achieves 91.3% mIoU and 31.1% IoU with only 3.9G FLOPs and 0.44M parameters, offering a strong efficiency–accuracy trade-off among lightweight models. This establishes it as a solid baseline in terms of performance and model compactness. Compared to this baseline, the results demonstrate that TwinLiteNet$^+$ consistently outperforms other lightweight multitask models across all metrics. In particular, the TwinLiteNet$^+_{Large}$ configuration achieves the highest scores in both tasks-92.9% mIoU for drivable area segmentation and 34.2% IoU for lane detection-outperforming strong baselines such as SegFormer, Sparse U-PDP, and IALaneNet.

Table 3: Performance benchmarking in mIoU (%) for Drivable Area Segmentation, IoU (%) and Acc (%) for Lane Segmentation of models with same tasks. * denotes results directly cited from [44]. The best and second best results are marked in **bold** and underline respectively.

Model	Drivable Area mIoU (%) ↑	Lane Acc (%) ↑	Lane IoU (%) ↑	FLOPS ↓	#Param. ↓
DeepLabV3+* [15]	90.9	–	29.8	30.7G	15.4M
SegFormer* [16]	92.3	–	31.7	12.1G	7.2M
R-CNNP [43]	90.2	–	24.0	–	–
YOLOP [43]	91.6	–	26.5	8.11G	5.53M
IALaneNet$_{\text{ResNet-18}}$ [10]	90.5	–	30.4	89.83G	17.05M
IALaneNet$_{\text{ResNet-34}}$ [10]	90.6	–	30.5	139.46G	27.16M
IALaneNet$_{\text{ConvNeXt-tiny}}$ [10]	91.3	–	31.5	96.52G	18.35M
IALaneNet$_{\text{ConvNeXt-small}}$ [10]	91.7	–	<u>32.5</u>	200.07G	39.97M
YOLOv8 (multi) [61]	84.2	81.7	24.3	–	–
Sparse U-PDP [44]	91.5	–	31.2	–	–
BILane [11]	91.2	–	31.3	–	1.4M
TwinLiteNet [12]	91.3	77.8	31.1	3.9G	0.44M
TwinLiteNet$^+_{\text{Nano}}$	87.3	70.2	23.3	**0.57G**	**0.03M**
TwinLiteNet$^+_{\text{Small}}$	90.6	75.8	29.3	<u>1.40G</u>	<u>0.12M</u>
TwinLiteNet$^+_{\text{Medium}}$	<u>92.0</u>	<u>79.1</u>	32.3	4.63G	0.48M
TwinLiteNet$^+_{\text{Large}}$	**92.9**	**81.9**	**34.2**	17.58G	1.94M

Importantly, TwinLiteNet$^+_{\text{Large}}$ accomplishes this with a significantly smaller model size (1.94M parameters) and moderate FLOPs (17.58G) compared to heavyweight counterparts like IALaneNet or DeepLabV3+, making it highly competitive for both accuracy and efficiency. While the TwinLiteNet$^+_{\text{Nano}}$ model exhibits lower accuracy (mIoU of 87.3%, IoU of 23.3%), it offers ultra-efficient inference, requiring just 0.57G FLOPs and 0.03M parameters, making it suitable for highly resource-constrained embedded platforms. The Small and Medium configurations offer balanced trade-offs: TwinLiteNet$^+_{\text{Medium}}$ achieves 92.0% mIoU and 32.3% IoU with only 0.48M parameters-surpassing most existing models like YOLOP and even the lightweight BILane (which has 1.4M parameters but slightly lower IoU at 31.3%).

Overall, these results underscore the scalability and practicality of TwinLiteNet$^+$. The model family provides a spectrum of choices-from highly compact and fast variants to larger, high-accuracy models-empowering developers to choose configurations that best match their target deployment environments. The clear performance advantage of TwinLiteNet$^+$ across different configurations confirms its suitability for both high-performance and real-time embedded applications in autonomous driving.

4.3. Driving perception results in different environments

The BDD100K dataset offers diverse annotations for weather conditions, times of the day, and traffic scenes, providing a comprehensive foundation for evaluating model robustness under real-world driving scenarios. To this end, we conduct a detailed analysis of TwinLiteNet$^+_{\text{Large}}$ across multiple environmental contexts. As shown in Table 4, TwinLiteNet$^+_{\text{Large}}$ demonstrates stable performance across a wide range of environmental conditions. Notably, while conditions such as nighttime, Dawn/Dusk, and rainy weather are generally considered challenging due to poor lighting or visual degradation, the model still maintains strong segmentation performance (e.g., 92.5% mIoU for nighttime, 90.2% for rainy). This is attributed, in part, to the relatively high number of training

Table 4: Performance of TwinLiteNet$^+_{\text{Large}}$ evaluated across different environmental conditions. The number of samples used in training and validation is also indicated.

Photometric scene	Training/Validation	Drivable Area	Lane
		mIoU (%) ↑	IoU (%) ↑
Weather conditions			
Clear	37,344/5,346	93.1	33.8
Overcast	8,770/1,239	93.7	35.8
Undefined	8,119/1,157	93.2	35.4
Snowy	5,549/769	91.6	31.6
Rainy	5,070/738	90.2	32.0
Partly Cloudy	4,881/738	93.3	35.3
Foggy	130/13	92.4	29.6
Times of the day			
Daytime	36,728/5,258	93.2	35.1
Night	28,108/3,929	92.5	32.9
Dawn/Dusk	5,027/778	92.9	33.9
Undefined	137/35	86.7	29.3
Traffic scenes			
City street	43,516/6,112	92.8	34.4
Highway	17,379/2,499	93.3	33.8
Residential	8,074/1,253	92.8	34.4
Parking lot	377/49	88.1	25.1
Undefined	361/53	90.3	31.0
Tunnel	129/27	89.8	28.9
Gas station	27/7	88.8	14.2

samples available for these conditions in the BDD100K dataset, which allows the model to learn more generalized representations. In contrast, the performance tends to drop more significantly in rare scenarios, such as parking lots, tunnels, or gas stations, where the dataset provides few samples (< 500 samples for the training set). In these cases, the segmentation performance declines noticeably, suggesting that data scarcity remains a limiting factor in model generalization under extreme conditions. At the same time, despite having only around 130 samples, foggy scenes still achieve competitive performance-likely because their visual characteristics are not significantly different from those of other weather conditions, allowing the model to transfer learned features effectively.

These findings highlight the importance of both data diversity and representation balance in training robust multi-task models for autonomous driving. The qualitative results under different environmental conditions are further analyzed in Sec. 4.4

4.4. Visualization

To provide a comprehensive evaluation, we conduct qualitative comparisons of different TwinLiteNet$^+$ configurations against the baseline TwinLiteNet under various environmental conditions. Specifically, we visualize segmentation outputs under (1) different times of the day-including daytime, dawn/dusk, and nighttime-as shown in Figure 6; (2) Figure 7 illustrates the results across different weather conditions, including snowy, rainy, overcast, and foggy. and (3) Figure 8 shows the
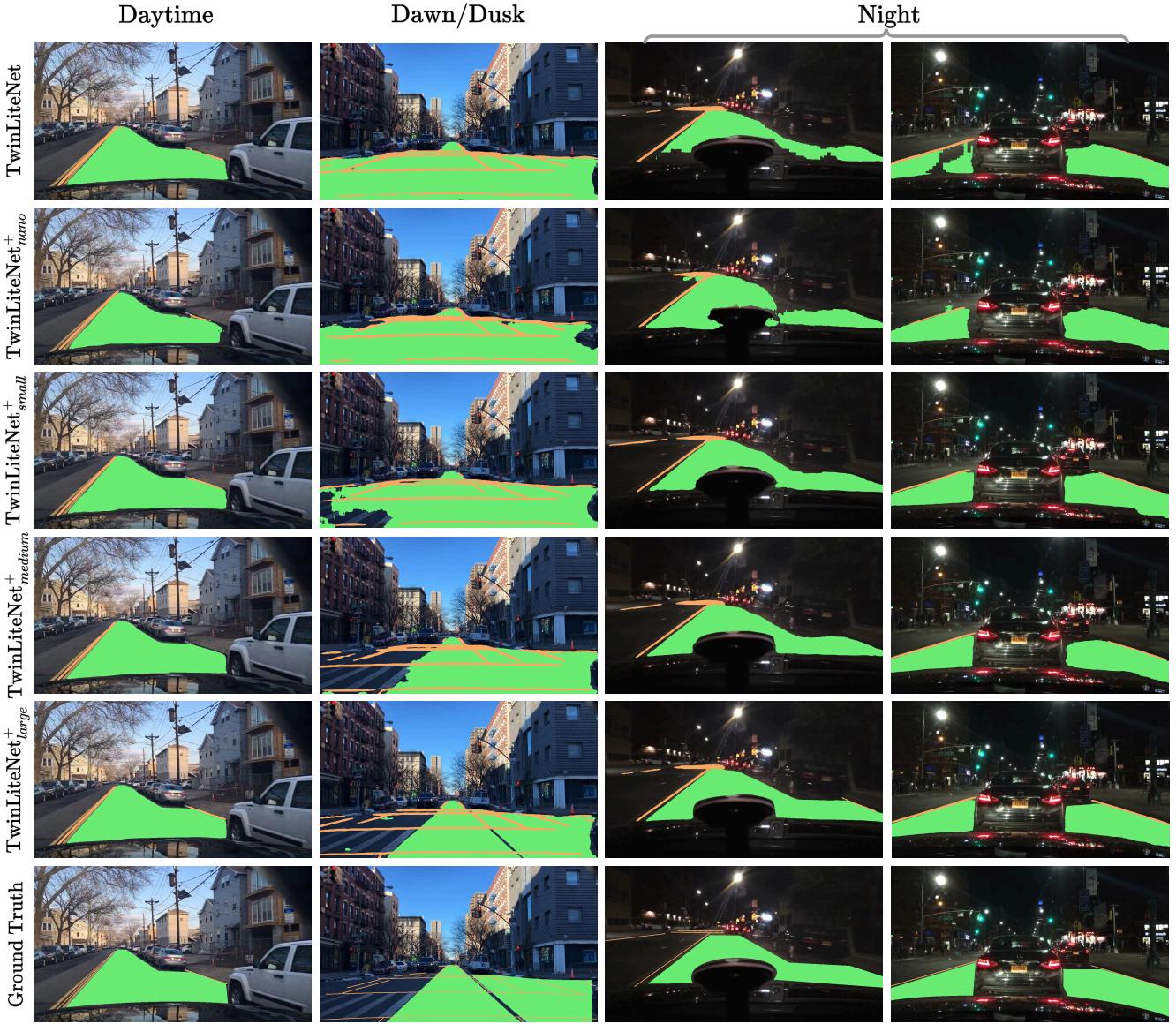
Figure 6: Qualitative results of TwinLiteNet and TwinLiteNet$^+$ at different times of the day.

results under different traffic scenes, including residential areas, tunnels, highways, and parking lots. As shown in the figures, TwinLiteNet$^+_{\text{Large}}$ consistently delivers the most accurate segmentation results, followed by TwinLiteNet$^+_{\text{Medium}}$, which achieves significant improvements over the baseline TwinLiteNet while maintaining similar computational cost. The enhanced performance of TwinLiteNet$^+$ is attributed not only to the integration of the Partial Class Activation Attention (PCAA) module-which facilitates more detailed spatial feature extraction through localized class-specific activations derived from Partial CAM-but also to the strengthened decoder design. The improved decoder incorporates additional convolutional layers after upsampling, allowing for better reconstruction of fine-grained features and contributing to smoother and more precise boundary delineation in segmentation outputs.

Furthermore, the qualitative results reveal that the baseline TwinLiteNet, as well as the lightweight configurations TwinLiteNet$^+_{\text{Nano}}$ and $^+_{\text{Small}}$, encounter challenges in complex environments. These include segmentation noise in cluttered scenes (e.g., residential, parking lot), inaccurate region segmentation (e.g., dawn/dusk), and missed detections of the small lanes (e.g.,

Figure 7: Qualitative results of TwinLiteNet and TwinLiteNet$^+$ in different weather condition.

foggy weather). In contrast, the larger configurations-TwinLiteNet$^+_{\text{Medium}}$ and TwinLiteNet$^+_{\text{Large}}$-demonstrate superior performance in these scenarios due to their greater representational capacity and deeper architecture.

While TwinLiteNet$^+_{\text{Nano}}$ and TwinLiteNet$^+_{\text{Small}}$ demonstrate lower segmentation accuracy, their lightweight architectures provide notable advantages in terms of computational efficiency and inference speed, making them highly suitable for resource-constrained embedded platforms. In contrast, higher-capacity configurations like TwinLiteNet$^+_{\text{Medium}}$ and TwinLiteNet$^+_{\text{Large}}$ consistently achieve more accurate and fine-grained segmentation results, particularly in the aforementioned challenging scenarios, due to their enhanced spatial representation capabilities and deeper model capacity. These observations highlight the flexibility and scalability of the TwinLiteNet$^+$ configs, enabling practical deployment across a wide range of autonomous driving applications-from high-performance systems to energy-efficient real-time use cases.
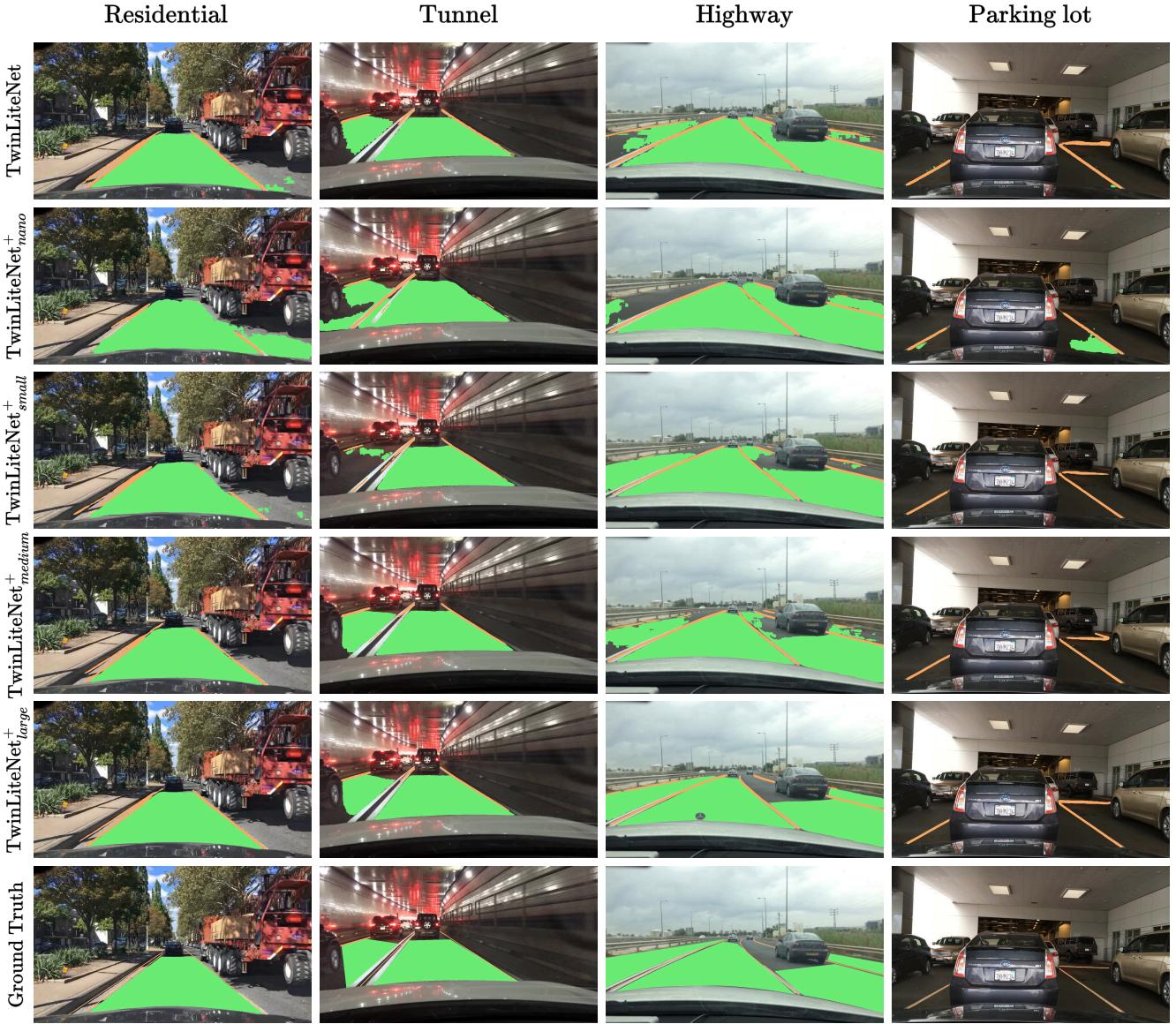
Figure 8: Qualitative results of TwinLiteNet and TwinLiteNet$^+$ in different scene condition.

4.5. *Practical Deployment Considerations*

4.5.1. *Quantization*

To evaluate the practical deployability of the TwinLiteNet$^+$ model on hardware with limited computational resources, we conducted experiments using three common inference data types: 32-bit floating point (FP32), 16-bit floating point (FP16), and 8-bit integer (INT8). Among these, FP16 can be applied directly without requiring retraining or calibration. In contrast, quantization to INT8 demands additional processing to preserve accuracy.

Specifically, for Post-Training Static Quantization (PTSQ), we followed a standard calibration procedure by sampling 500 random images from the training set to estimate activation ranges. Based on this, we applied 8-bit quantization to both weights and activations. While this approach is straightforward to integrate post-training, it resulted in reduced segmentation accuracy, particularly in lane detection, where pixel-level precision is crucial. To mitigate this problem, we employed Quantization-Aware Training (QAT), which simulates quantization effects during training. Using

Table 5: Performance benchmarking of TwinLiteNet+ across different Quantization approaches: Floating Point 16-bit (FP16) and Integer 8-bit (INT8). ↓ indicates a performance drop caused by quantization, whereas → signifies that the accuracy remains unchanged.

Config	Drivable Area mIoU (%)↑				Lane Acc (%)↑				Lane IoU (%)↑			
	FP32	FP16	INT8 PTSQ	INT8 QAT	FP32	FP16	INT8 PTSQ	INT8 QAT	FP32	FP16	INT8 PTSQ	INT8 QAT
Nano	87.3	87.3 → 0.0	86.0 ↓ 1.3	86.9 ↓ 0.4	70.2	70.1 ↓ 0.1	67.2 ↓ 3.0	69.9 ↓ 0.3	23.3	23.2 ↓ 0.1	21.8 ↓ 1.5	23.2 ↓ 0.1
Small	90.6	90.6 → 0.0	88.5 ↓ 2.1	90.2 ↓ 0.4	75.8	75.7 ↓ 0.1	74.6 ↓ 1.2	75.6 ↓ 0.2	29.3	29.3 → 0.0	28.3 ↓ 1.0	28.8 ↓ 0.5
Medium	92.0	92.0 → 0.0	91.6 ↓ 0.4	91.9 ↓ 0.1	79.1	79.1 → 0.0	77.1 ↓ 2.0	78.6 ↓ 0.5	32.3	32.2 ↓ 0.1	31.5 ↓ 0.8	31.9 ↓ 0.4
Large	92.9	92.9 → 0.0	92.7 ↓ 0.2	92.7 ↓ 0.2	81.9	81.9 → 0.0	80.2 ↓ 1.7	81.4 ↓ 0.5	34.2	34.2 → 0.0	33.6 ↓ 0.6	34.0 ↓ 0.2

the `pytorch_quantization` framework, we inserted fake quantization modules into the model's computational graph. Rather than training from scratch, we fine-tuned a pre-trained model for an additional 10 epochs, enabling it to adapt to quantization noise while maintaining training stability.

As shown in Table 5, TwinLiteNet+ maintains strong segmentation performance under all quantization settings. While INT8 quantization involves a more complex process than FP16, QAT allows the model to retain accuracy comparable to FP32 while significantly improving inference efficiency and reducing model size-critical factors for deployment on resource-constrained embedded devices.

4.5.2. Inference Performance on Embedded Devices

Furthermore, we implement our model on several embedded devices such as Jetson Xavier and Jetson TX2. TensorRT-FP32, FP16 are used respectively for inference and then measured

Table 6: Latency and Power Consumption benchmarking of TwinLiteNet+ on Embedded Devices (Jetson Xavier and Jetson TX2) in different Quantization methods.

Config	Jetson Xavier			Jetson TX2	
	INT8	FP16	FP32	FP16	FP32
Latency (ms) ↓					
Nano	$7.553_{\pm 0.046}$	$9.155_{\pm 0.092}$	$10.303_{\pm 0.222}$	$22.268_{\pm 0.156}$	$26.374_{\pm 0.058}$
Small	$10.286_{\pm 0.093}$	$12.861_{\pm 0.941}$	$15.662_{\pm 0.055}$	$33.818_{\pm 0.134}$	$41.961_{\pm 0.035}$
Medium	$15.548_{\pm 0.083}$	$20.460_{\pm 0.067}$	$27.985_{\pm 0.166}$	$61.785_{\pm 0.015}$	$84.631_{\pm 0.096}$
Large	$29.102_{\pm 0.107}$	$43.089_{\pm 0.198}$	$69.150_{\pm 0.382}$	$153.240_{\pm 0.094}$	$218.150_{\pm 0.099}$
Power (Watt) ↓					
Nano	$9.657_{\pm 2.034}$	$10.029_{\pm 2.267}$	$11.790_{\pm 2.089}$	$3.647_{\pm 0.637}$	$4.097_{\pm 0.603}$
Small	$10.926_{\pm 1.924}$	$11.086_{\pm 2.385}$	$12.732_{\pm 2.505}$	$4.043_{\pm 0.463}$	$4.513_{\pm 0.376}$
Medium	$12.427_{\pm 2.086}$	$13.585_{\pm 1.832}$	$15.496_{\pm 1.549}$	$4.496_{\pm 0.202}$	$4.747_{\pm 0.122}$
Large	$14.666_{\pm 1.632}$	$15.980_{\pm 1.187}$	$17.710_{\pm 0.594}$	$4.883_{\pm 0.057}$	$5.019_{\pm 0.051}$

the inference latency and power consumption on each device. With TensorRT-INT8, only Jetson Xavier is measured, as the Jetson TX2 isn't supported yet. To enable INT8 quantization, we adopt the Post-Training Static Quantization (PTSQ) method, as our primary focus is to assess inference efficiency rather than optimize quantization accuracy. In this process, we perform calibration using 500 randomly selected samples from the training set to estimate the activation ranges, following the setup described in Section 4.5.1. All inference experiments are performed using TensorRT with default settings, without any manual tuning or hardware-specific optimization. This setup aims to evaluate how well the model performs on various embedded devices. To minimize measurement discrepancies, we conduct five iterations, with each iteration performing 100 inferences. Results from Table 6 show that using the TwinLiteNet$^+$ model on embedded devices like Jetson Xavier and Jetson TX2 yields promising results in terms of inference latency and power consumption. Specifically, the Nano and Small configs of the model exhibited low latency and reasonable power consumption on both devices with TensorRT-INT8, highlighting the model's performance optimization capability in a limited computational environment. Although the Medium and Large configs have higher latency and power consumption, they still maintain an acceptable level, demonstrating the model's flexibility and scalability. These results not only validate the impressive performance of TwinLiteNet$^+$ but also underscore its practical potential in real-world applications, particularly in the field of autonomous vehicles and smart embedded systems.

4.6. *Directly* & *Alternative Area segmentation results*

In this section, we expand our research to include a model that focuses on the division of directly drivable and alternative areas. This approach differs from the standard drivable area segmentation, which usually combines these two distinct areas into a single area. Figure 9 illustrates the main difference between the two segmentation tasks, depicted in Figure 9b and Figure 9c, where Figure 9c is segmented into direct and alternative areas. This division of regions allows vehicles to differentiate between navigable regions and alternative routes, making it easier to change lanes or maneuver around obstacles in the region. When performing this segmentation, the controllable segmentation decoder block output has three channels instead of two. Therefore, the output of the model for the driving area segment is $\mathbf{O}_{drivable} \in \mathbb{R}^{3 \times H \times W}$. We train the model using two designs: One with a single decoder for direct and alternative driving area segmentation and another with two decoders for multi-task models (Lane segmentation and Directly & Alternative Area segmentation).

Table 7 provides a comprehensive and detailed overview of the performance of various segmentation models applied to direct region segmentation and replacement. In addition to the evaluation mIoU metric, in this study, we also assess the Pixel Accuracy (PA) and Mean Pixel Accuracy (mPA), facilitating comparison with previous research. In this experiment, we compare the TwinLiteNet$^+_{\text{Large}}$ model after modifications to demonstrate the responsiveness of our model to this task, and we name it as TwinLiteNet$^+_{\text{D&A}}$ to differentiate it from the Large one. Additionally, we experiment with the TwinLiteNet$^+_{\text{D&A}}$ model when performing multi-tasks and the TwinLiteNet$^+_{\text{D&A}}$ with only one decoding block for the driving area segmentation. The TwinLiteNet$^+_{\text{D&A}}$ models, in both multitask and single-task configurations, stand out with high performance across all three metrics, with our TwinLiteNet$^+_{\text{D&A}}$ model achieving the highest mPA of 92.1%, surpassing previous studies and competitive in other metrics. This comprehensive assessment underscores the advancements in segmentation techniques and highlights the TwinLiteNet$^+_{\text{D&A}}$ model's potential to improve accuracy and detail capture in image segmentation tasks. We present some results of the TwinLiteNet$^+_{\text{D&A}}$ model in Figure 10 to emphasize its proficiency in differentiating between di-

Table 7: Perforance benchmarking in mIoU (%), PA (%) and mPA (%) between different models in Directly & Alternative Area segmentation tasks. The best and second best results are marked in **bold** and underline respectively.

Model	Directly & Alternative Area Segmentation		
	mIoU (%) ↑	PA(%) ↑	mPA(%) ↑
DeepLabv3+ [15]	**84.73**	–	–
PSPNet [7]	84.13	–	–
Pizzati et al. [28]	82.62	–	–
ShuDA-RFBNet [29]	82.67	–	–
Resnet+ASPP+FPN [30]	<u>84.58</u>	**97.09**	91.14
Resnet+FPN [30]	82.70	96.51	91.42
Resnet+ASPP+top-down [30]	82.80	96.60	90.68
Resnet+top-down [30]	82.44	96.24	88.39
Lee [31]	83.34	–	–
Sun et al. [32]	83.01	–	–
IDS-MODEL [33]	83.63	–	–
TwinLiteNet$^+_{\text{D\&A}}$ (single-task)	83.9	96.9	<u>92.0</u>
TwinLiteNet$^+_{\text{D\&A}}$ (multi-task)	84.3	<u>97.0</u>	**92.1**

(a) Ground truth (b) Drivable Area Segmentation (c) Directly & Alternative Area segmentation

Figure 9: Examples of Ground truth visualization for Directly & Alternative Area segmentation task.

rectly drivable and alternative paths under various lighting conditions, from daylight to nighttime scenarios.

4.7. *Ablation study*

4.7.1. *Multi-task versus single-task*

To evaluate the effectiveness of the multitask learning strategy, we compare the performance of the TwinLiteNet$^+_{\text{Large}}$ model in multitask and single-task configurations. In the single-task settings, we retain only the relevant decoder-either for drivable area or lane segmentation-while removing the other to isolate performance. The results are summarized in Table 8.

For the drivable area segmentation task, the multitask version slightly outperforms its single-task counterpart, achieving a 0.3% gain in mIoU. This improvement suggests that shared representations with the lane segmentation task positively influence the learning process by providing complementary structural cues. For the lane segmentation task, multitask learning maintains the same lane accuracy (81.9%) but experiences a slight drop of 0.2% in IoU, which may result from representational interference between the tasks. These findings indicate that while multitask
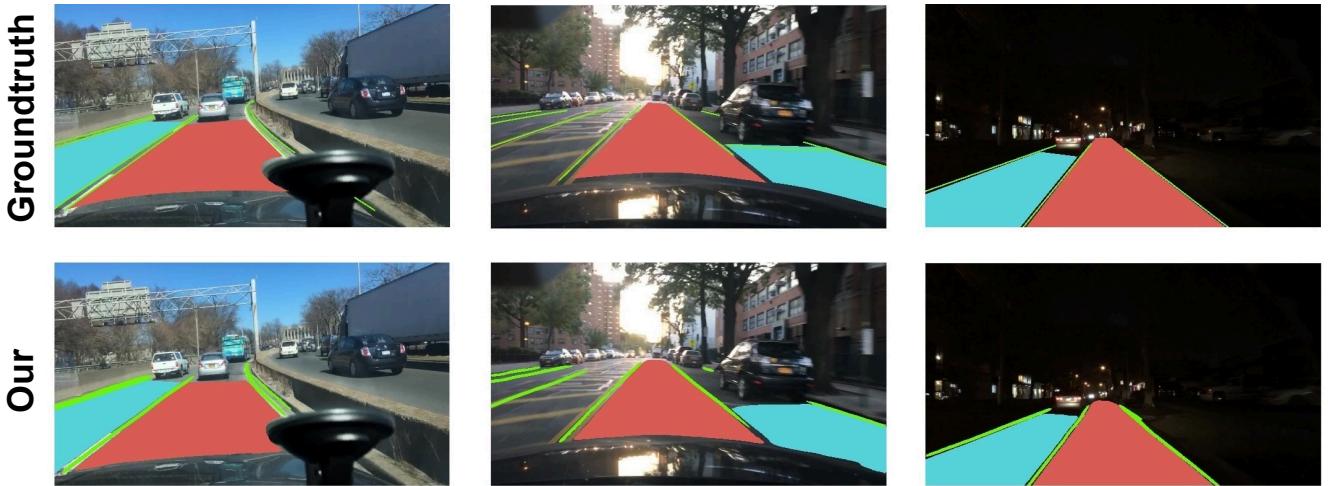
Figure 10: Results visualization of TwinLiteNet$^+_{D\&A}$ for Directly & Alternative Area segmentation. Red regions are directly drivable area, the blue ones are alternative and the lanes are green.

Table 8: TwinLiteNet$^+$ model's evaluation between Multitasking Learning versus Single-Task Learning approach. The best results are marked in **bold**. ↑ indicates increasing, ↓ indicates decreasing, and → represents no change. Red denotes negative impact, while blue highlights gains achieved through multi-task training.

Method	Drivable Area	Lane		Parameter ↓	FLOPs ↓
	mIoU (%) ↑	Acc (%) ↑	IoU (%) ↑		
Drivable Area (only)	92.6	✘	✘	1.91M	16.97G
Lane (only)	✘	81.9	34.4	1.91M	16.97G
Multi-task	**92.9**	**81.9**	34.2	1.94M	17.58G
	↑ 0.3	→ 0.0	↓ 0.2	↑ 0.03	↑ 0.61

learning introduces minor trade-offs-particularly for tasks sensitive to spatial precision-it also offers measurable advantages in feature sharing and overall model compactness.

In terms of efficiency, the multitask model incurs only a marginal increase in both parameter count (+0.03M) and computational cost (+0.61 GFLOPs) compared to the single-task variants. This slight overhead primarily stems from the addition of a single extra decoder to support the second task, while the encoder is shared between both. In contrast, deploying two separate single-task models would require duplicating the entire backbone, leading to a significantly higher computational cost and memory footprint. Thus, the multitask approach not only enables joint optimization and feature sharing but also offers a more resource-efficient alternative to running independent models. These findings reinforce the practical value of multitask learning for real-time autonomous driving applications, where both accuracy and efficiency are critical.

4.7.2. The ablations in different experimental settings

To better understand the contribution of each component in the proposed TwinLiteNet$^+$ architecture, we perform an ablation study based on the TwinLiteNet$^+_{Large}$ configuration. Each experiment isolates a specific module to evaluate its impact on segmentation performance and model complexity, with quantitative results summarized in Table 9. Six modified variants are constructed as follows: (1) *Tversky Loss:* removed by replacing the combined objective with Focal Loss alone for both segmentation branches; (2) *DESP:* replaced with the original ESP module from the base-

Table 9: TwinLiteNet$^+_{Large}$ Model's evaluation with different experimental settings. Across different variants of TwinLiteNet$^+$, the symbols ↑, → and ↓ indicate changes in both performance metrics and computational cost. Specifically, ↑ represents an improvement in accuracy (mIoU, Acc, IoU) or an increase in computational overhead, while ↓ indicates a reduction. Additionally, red-colored values highlight negative changes, whereas blue-colored values indicate positive improvements.

| | Drivable Area | Lane | | FLOPs ↓ | #Param. ↓ |
	mIoU (%) ↑	Acc (%) ↑	IoU (%) ↑		
TwinLiteNet$^+_{Large}$	**92.9**	<u>81.9</u>	**34.2**	17.58G	1.94M
w/o Tversky Loss	<u>92.7</u>	79.7	31.1	17.58G	1.94M
	↓ 0.2	↓ 2.2	↓ 3.1	→ 0.0	→ 0.0
w/o DESP proposed	**92.9**	**82.2**	**34.2**	22.19G	2.78M
	→ 0.0	↑ 0.3	→ 0.0	↑ 4.61	↑ 0.84
w/o Robust Decoder	92.4	81.1	33.3	**16.78G**	<u>1.90M</u>
	↓ 0.5	↓ 0.8	↓ 0.9	↓ 0.80	↓ 0.04
w/o Multiple Decoder	91.3	79.9	32.1	<u>16.99G</u>	1.91M
	↓ 1.6	↓ 2.0	↓ 2.1	↓ 0.59	↓ 0.03
w/o PCAA Module	92.5	81.4	33.8	17.42G	**1.82M**
	↓ 0.4	↓ 0.5	↓ 0.4	↓ 0.16	↓ 0.12
w/o EMA	<u>92.7</u>	81.7	<u>33.9</u>	17.58G	1.94M
	↓ 0.2	↓ 0.2	↓ 0.3	→ 0.0	→ 0.0

line TwinLiteNet; (3) *Robust Decoder:* disabled by reverting to the simple decoder design of the TwinLiteNet baseline, thus not use the UCB and USB upsampling proposed modules; (4) *Multiple Decoder:* replaced with a shared single decoder head producing a unified three-channel output $\mathbf{O} \in \mathbb{R}^{3 \times H \times W}$ for both tasks; (5) *PCAA Module:* removed by bypassing the attention mechanism and directly linking the encoder output to the decoder; and (6) *EMA (Exponential Moving Average):* deactivated by using the model's raw weights instead of the smoothed exponential averages accumulated during training.

Experimental findings show that each component plays an important role in the model's effectiveness. The removal of Tversky Loss results in a few performance drops in drivable area segmentation. However, it is significant in lane segmentation, highlighting its crucial role in managing class imbalance and improving recall for thin and sparse structures. Substituting DESP with the baseline ESP architecture slightly increases lane segmentation accuracy. However, it introduces a notable rise in FLOPs and parameter count, underscoring the importance of depthwise separable convolution in achieving efficiency. Eliminating any of the Robust Decoder, Multiple Decoder, or PCAA modules leads to consistent degradation across both drivable area and lane segmentation metrics, confirming their importance in enhancing spatial detail, semantic refinement, and task-specific decoding. Lastly, omitting EMA leads to minor reductions in performance, suggesting its stabilizing influence on model convergence and generalization.

The results from the ablation experiments demonstrate that each component in the design of TwinLiteNet$^+$ plays a vital role-not only enhancing accuracy in both segmentation tasks but also optimizing computational cost.

Table 10: Comparison of segmentation performance across single-task and multi-task models. The best and second best results are marked in **bold** and <u>underline</u> respectively.

Model	Drivable Area	Lane	Params ↓
	mIoU (%) ↑	IoU (%) ↑	
Drivable Area Segmentation (Only)			
PSPNet [7]	89.6	✗	–
MultiNet [8]	71.6	✗	–
R-CNNP$_{DA\text{-}Seg}$ [43]	90.2	✗	–
YOLOP$_{DA\text{-}Seg}$ [43]	92.0	✗	–
YOLOv8$_{segda}$ [61]	78.1	✗	3.26M
YOLO-D [62]	92.4	✗	–
Lane Segmentation (Only)			
ENet [5]	✗	14.6	–
ENET-SAD [6]	✗	16.0	–
SCNN [9]	✗	15.8	–
YOLOv8$_{segll}$ [61]	✗	22.9	3.26M
YOLO-L [62]	✗	28.1	–
Drivable Area and Lane Segmentation			
DeepLabV3+ [15]	90.9	29.8	15.4M
SegFormer [16]	92.3	31.7	7.2M
R-CNNP [43]	90.2	24.0	–
YOLOP$_{Seg\ Only}$ [43]	91.6	26.5	5.53M
IALaneNet$_{ConvNeXt-small}$ [10]	91.7	<u>32.5</u>	39.9M
YOLOv8$_{Multi}$ [61]	84.2	24.3	–
Sparse U-PDP$_{w/o\ Detection}$ [44]	91.5	31.2	–
TwinLiteNet [12]	91.3	31.1	0.44M
Drivable Area and Lane Segmentation + Vehicle Detection			
HybridNets [20]	90.5	31.6	13.8M
YOLOP [43]	91.5	26.2	7.9M
DRMNet [63]	92.2	27.0	8.09M
YOLOPv2 [64]	**93.2**	27.3	38.9M
A-YOLOM(n) [57]	90.5	28.2	4.43M
A-YOLOM(s) [57]	91.0	28.8	13.61M
YOLOPX [21]	**93.2**	27.2	32.9M
CenterPNets [65]	92.8	32.1	28.6M
Sparse U-PDP [44]	<u>92.9</u>	32.4	12.05M
CFFM [66]	92.8	31.1	-
TriLiteNet$_{base}$ [67]	92.4	29.8	2.35M
YOLOPv3 [22]	**93.2**	28.0	30.2M
TwinLiteNet$^+_{Nano}$	87.3	23.3	**0.03M**
TwinLiteNet$^+_{Small}$	90.6	29.3	<u>0.12M</u>
TwinLiteNet$^+_{Medium}$	92.0	32.3	0.48M
TwinLiteNet$^+_{Large}$	<u>92.9</u>	**34.2**	1.94M

4.8. *More comparison*

In Table 10, we present a comprehensive comparison of the proposed TwinLiteNet$^+$ model against a diverse set of representative methods selected based on task relevance. These include: (1) single-task models, which focus exclusively on either lane segmentation (e.g., [5, 6, 9, 57, 62]) or drivable area segmentation (e.g., [7, 8, 43, 57, 62]); (2) and models designed explicitly for drivable area and lane segmentation [12, 10, 68, 15, 16], which share the same task formulation as our method; (3) multi-task models that jointly perform drivable area, lane, and object detection, such as [20, 43, 64, 22, 21, 57, 65, 67, 66, 44]. This selection ensures that our evaluation captures related approaches, from task-specific to comprehensive multi-task perception models.

The results indicate that TwinLiteNet$^+$ achieves highly competitive performance, particularly within the lightweight model category. Notably, TwinLiteNet$^+_{\text{Nano}}$ and TwinLiteNet$^+_{\text{Small}}$ exhibit excellent trade-offs between model size and accuracy, with parameter counts of only 0.03M and 0.12M, respectively-making them well-suited for deployment on resource-constrained embedded systems. While single-task models are typically optimized for a specific objective, they lack the capacity to leverage complementary information across tasks, as discussed in Section 4.7.1. In contrast, the multitask learning strategy employed in TwinLiteNet$^+$ enhances segmentation performance by enabling effective feature sharing, allowing it to outperform dedicated single-task counterparts. On the other hand, multitask models that incorporate object detection often require significantly more complex architectures and higher computational overhead. Thus, a multitasking design focused solely on segmentation tasks-such as TwinLiteNet$^+$-achieves a favorable balance between accuracy, efficiency, and architectural simplicity, making it more suitable for real-world applications on embedded platforms.

While TwinLiteNet$^+_{\text{Large}}$ achieves a strong mIoU of 92.9% for drivable area segmentation, it falls slightly short of the 93.2% achieved by high-capacity models such as YOLOPv2 [64], YOLOPv3 [22], and YOLOPX [21]. However, these models have a large number of parameters, exceeding 30 million, rendering them less practical for embedded deployment. Nevertheless, TwinLiteNet$^+_{\text{Large}}$ achieves the highest lane segmentation IoU in the entire benchmark (34.2%), outperforming the second-best IALaneNet [10] (32.5%), despite IALaneNet requiring over 39.9M parameters-more than 20 times that of TwinLiteNet$^+$Large.

These results provide a broader perspective by evaluating TwinLiteNet$^+$ against both single-task and multi-task approaches, including those that include object detection, further ensuring the effectiveness and scalability of our proposed lightweight model.

5. Discussion and Conclusion

5.1. *Limitations and future work*

Although TwinLiteNet$^+$ achieves a reasonable balance between accuracy and computational efficiency, there are still several limitations that should be addressed in future research. *First*, the model is currently trained and evaluated under general environmental conditions and has not been optimized for specific scenarios. As a result, its performance tends to degrade in adverse weather conditions or cases with limited training samples. *Second*, TwinLiteNet$^+$ currently focuses on only two perception tasks: drivable area segmentation and lane detection. While this design helps maintain a compact and efficient architecture, it lacks the comprehensiveness required by more advanced autonomous driving systems, which typically demand simultaneous handling of multiple tasks such as object detection, depth estimation, or traffic sign recognition. *Third*, although the model is lightweight and efficient, it relies on manually designed architectural configurations. The

lack of neural architecture search (NAS) techniques limits its adaptability to diverse deployment requirements in real-world settings.

Addressing these limitations will be essential further to enhance the model's performance and practical applicability. Doing so will not only improve TwinLiteNet$^+$ itself but also contribute to the advancement of more intelligent, efficient, and reliable multi-task perception systems for autonomous driving.

5.2. Conclusion

In this study, we presented TwinLiteNet$^+$, a novel and efficient multi-task segmentation model designed for drivable area and lane detection. By enhancing both the encoder and decoder architecture while maintaining a lightweight design, TwinLiteNet$^+$ achieves a strong balance between segmentation accuracy and computational efficiency. The model is offered in four scalable configurations, making it adaptable to a wide range of hardware-from high-performance GPUs to resource-constrained embedded systems. Extensive experiments on the BDD100K dataset demonstrate that TwinLiteNet$^+$ not only delivers competitive accuracy compared to existing methods but also ensures real-time performance suitable for practical deployment. These results highlight the model's potential as a reliable perception module in intelligent driving systems, where both efficiency and accuracy are critical. This work contributes a promising solution for real-world autonomous driving applications, where streamlined architectures and performance-aware designs are increasingly essential.

6. Acknowledgement

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