ECE M116C / CS 151B: Week 3 Section

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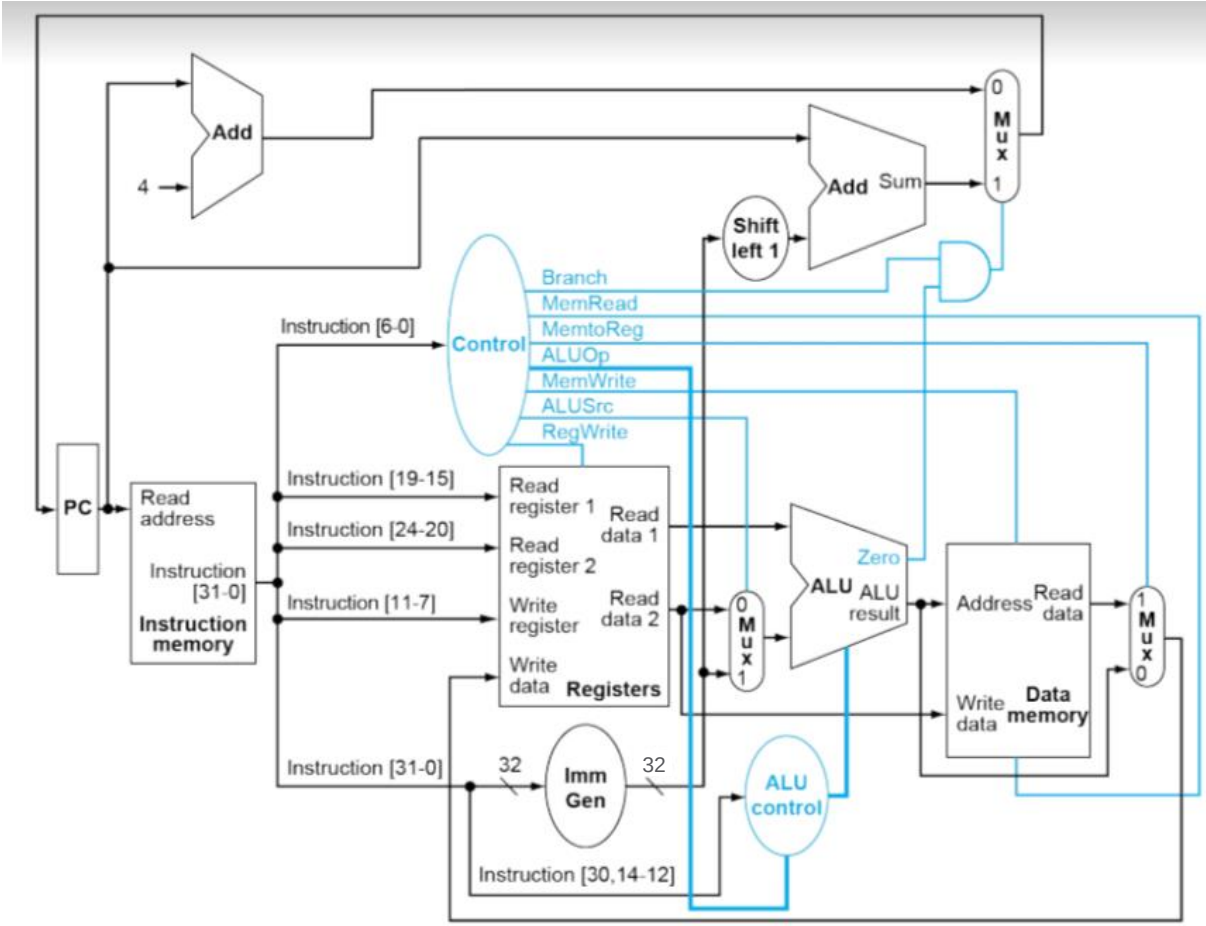
Instruction Latency



Datapath +
Controller

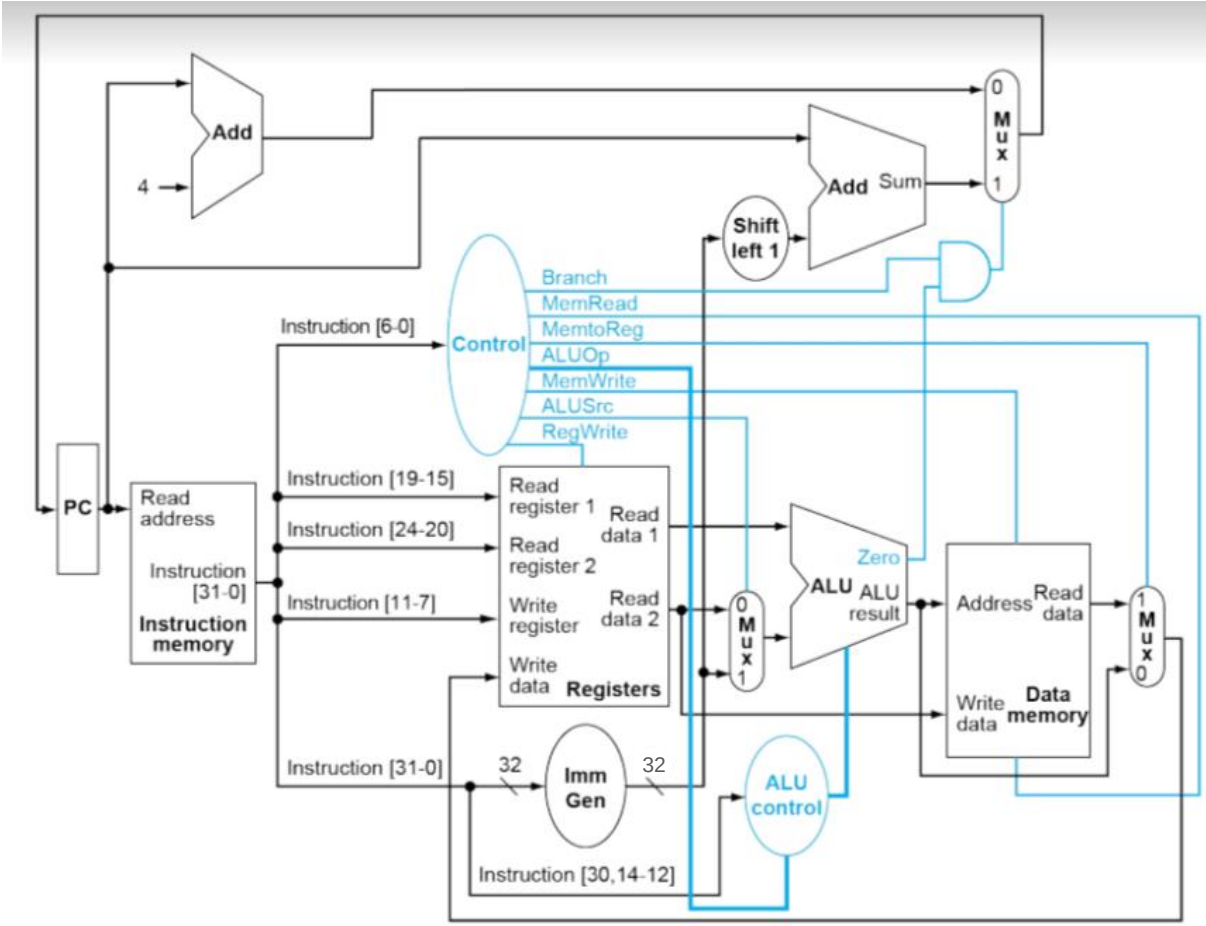
*Images were taken from Hennessy Patterson Book [1].

Latency, Clock Cycle Example

Question: What is the latency for the “beq” instruction?

Mem (I and D) (read)	Reg. File (read)	Reg. File (write)	Mux (any size)	ALU	Gate (any)
300 ps	180 ps	10 ps	20 ps	220 ps	5 ps

Imm Gen	PC (read)	Adder	PC (write)	Mem (D) (write)	Control
40 ps	20 ps	150 ps	20 ps	15 ps	60 ps



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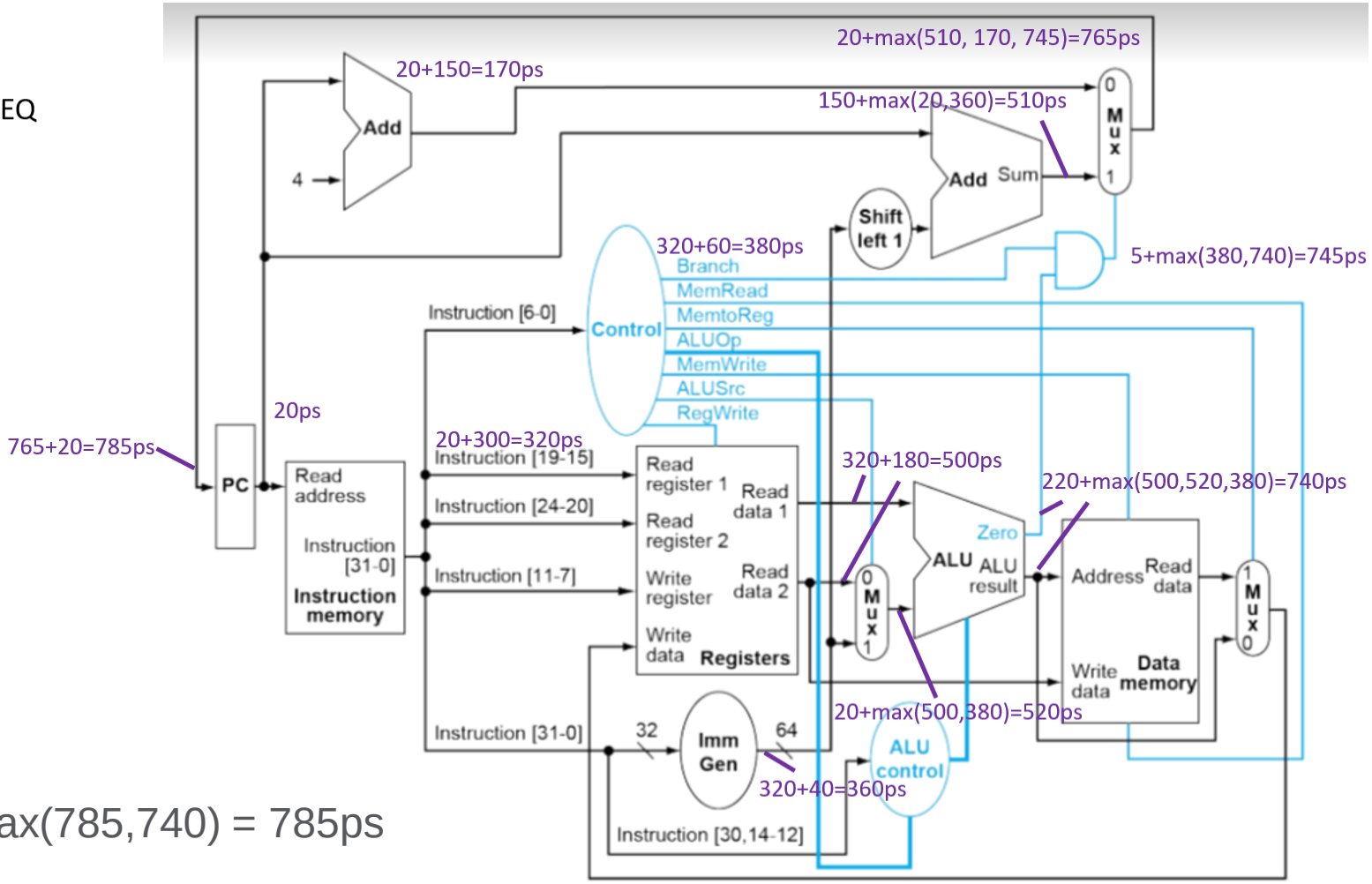
BEQ



max(785,740) = 785ps

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Performance Metrics

Iron Law: CPU Time

$$CPU\ Time = InstructionCount \times CyclePerInstruction \times CycleTime$$

CPU Time Example 1

Question: If the CPU time is 2 seconds, the processor clock speed is 1 GHz, and Cycles Per Instruction is 4, what is the Instruction Count?

$$CPU\ Time = InstructionCount \times CyclePerInstruction \times CycleTime$$

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$$CPU\ Time = InstructionCount \times CyclePerInstruction \times CycleTime$$

Answer: $2\ \text{sec} = InstructionCount * \left(4 \frac{cycles}{instruction}\right) * \left(\frac{1}{1\ GHz} * \frac{1\ GHz}{10^9\ Hz}\right)$

InstructionCount = 500 million instructions

CPU Time Example 2

Question: If the processor clock speed is 1 GHz, and 40% of the instructions take 1 cycle and 60% of the instructions take 2 cycles, and the instruction count is 500 million instructions, what is the CPU time?

$$CPU\ Time = InstructionCount \times CyclePerInstruction \times CycleTime$$

CPU Time Example 2

Question: If the processor clock speed is 1 GHz, and 40% of the instructions take 1 cycle and 60% of the instructions take 2 cycles, and the instruction count is 500 million instructions, what is the CPU time?

$$CPU\ Time = InstructionCount \times CyclePerInstruction \times CycleTime$$

Answer: $(500\ mil\ * \frac{10^6}{1\ mil}) * (0.4\ * 1 + 0.6\ * 2)\ cycles\ * (\frac{1}{1\ GHz}\ * \frac{1\ GHz}{10^9\ Hz})$

0.8 seconds

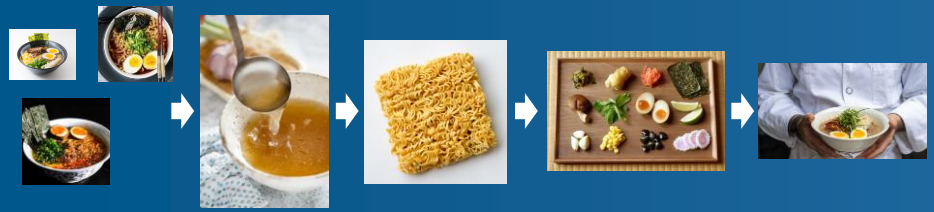
Project 1: Single Cycle CPU

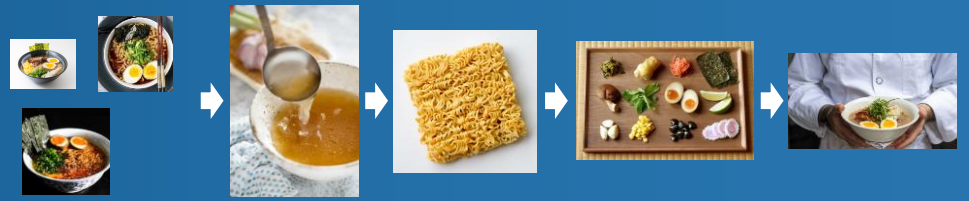
Pipelining

Thought Experiment

Approach 1:

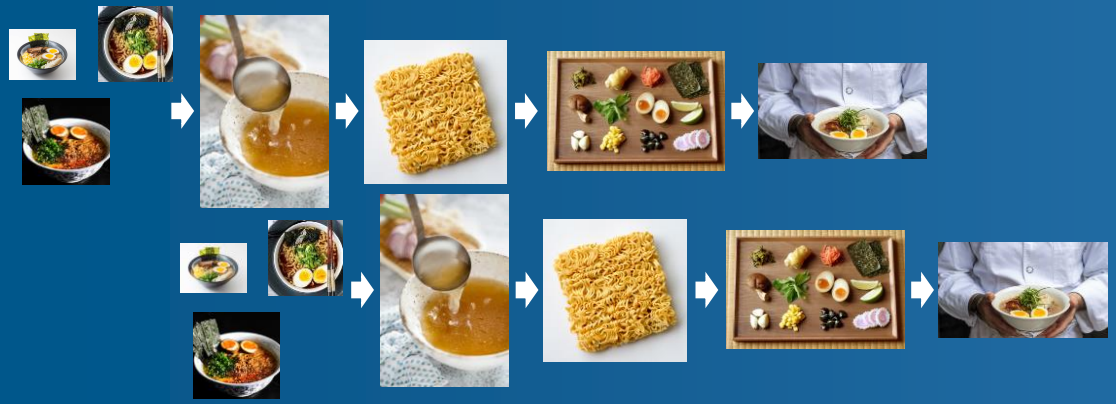
Time



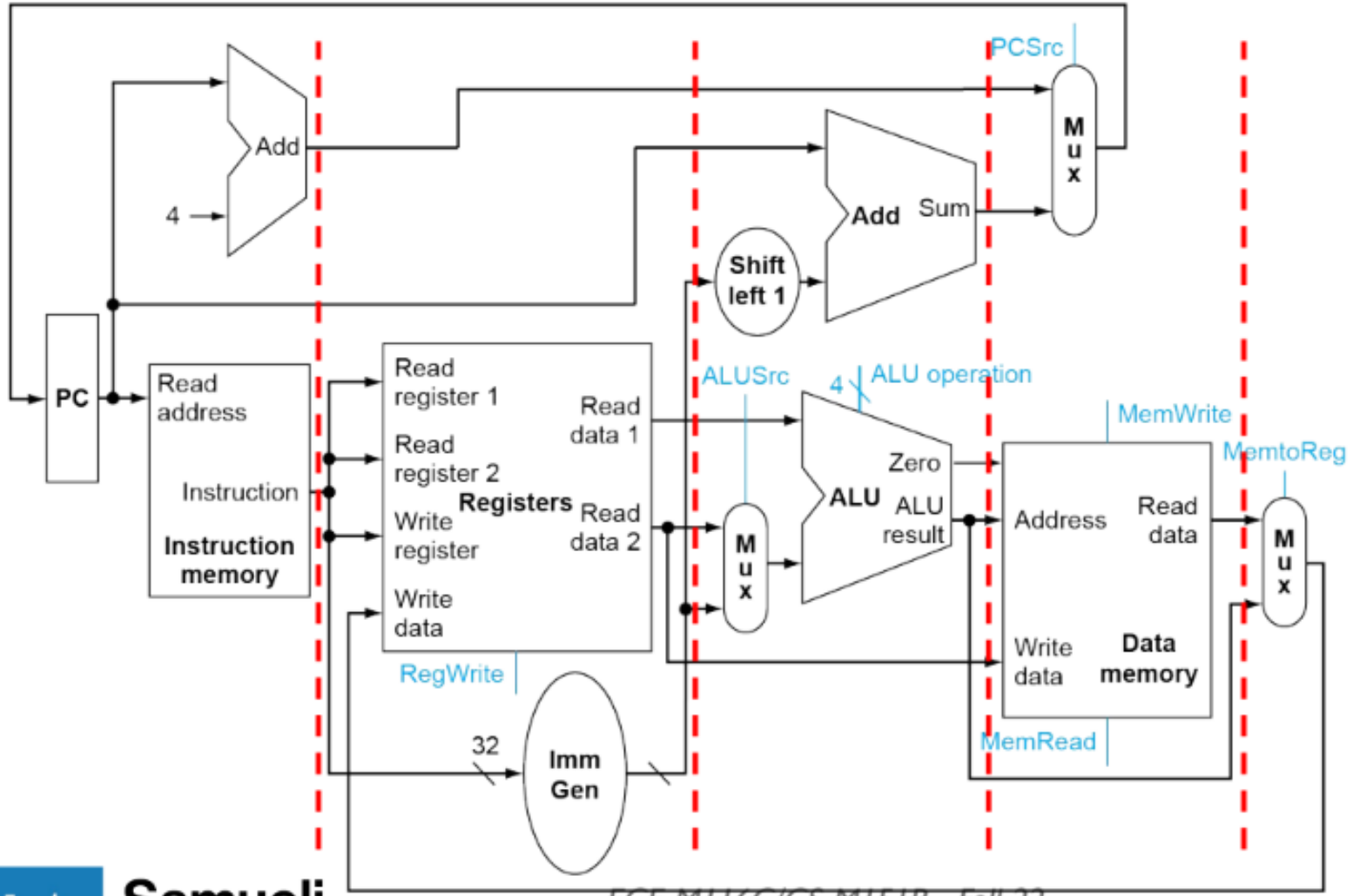


Approach 2:

Time



.....and more.....


PCSrc
Add
4
M
u
x
Add
Sum
Shift
left 1
PC
Read
address
Instruction
Instruction
memory
Read
register 1
Read
register 2
Registers
Write
register
Write
data
Read
data 1
Read
data 2
RegWrite
ALUSrc
4
ALU operation
M
u
x
ALU
Zero
ALU
result
MemWrite
MemtoReg
Address
Read
data
Write
data
Data
memory
MemRead
M
u
x
32
Imm
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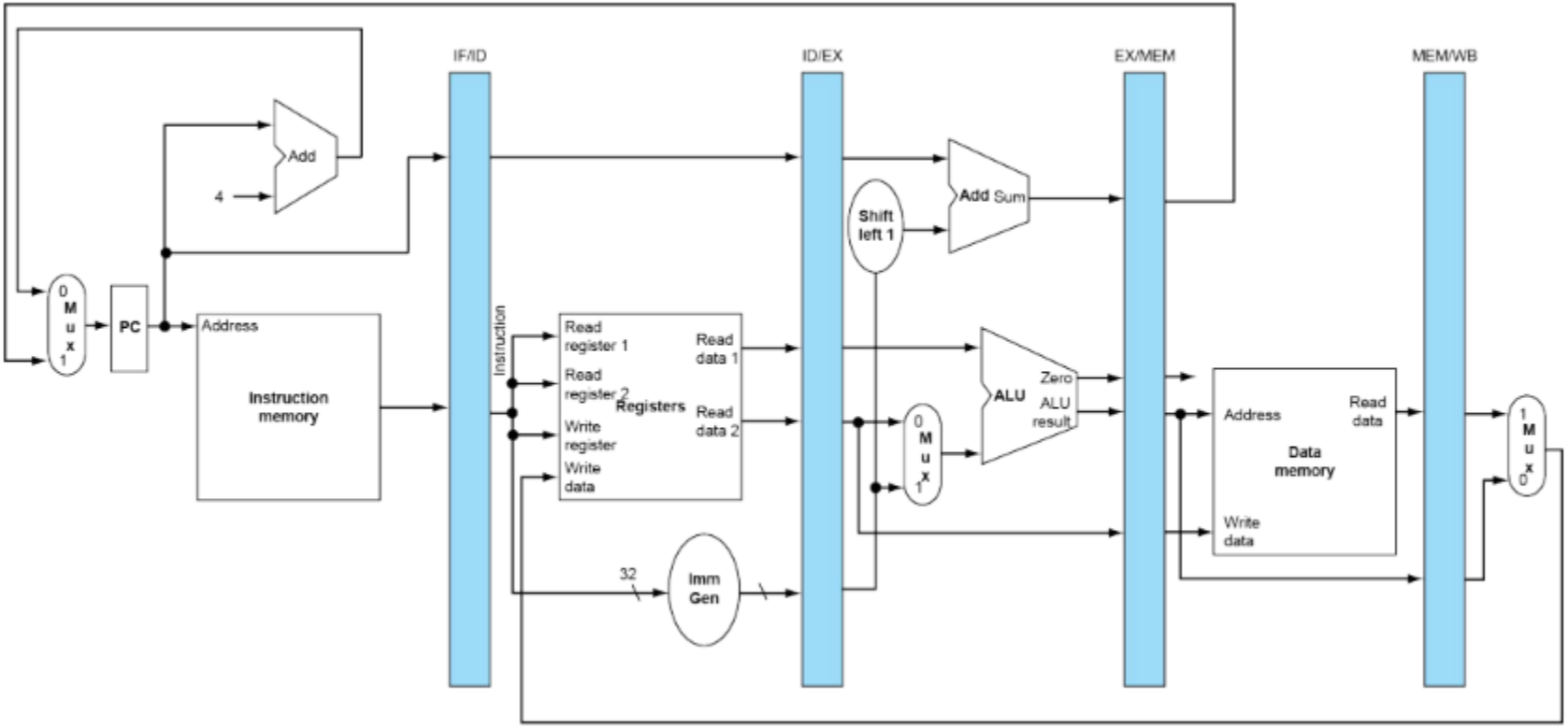
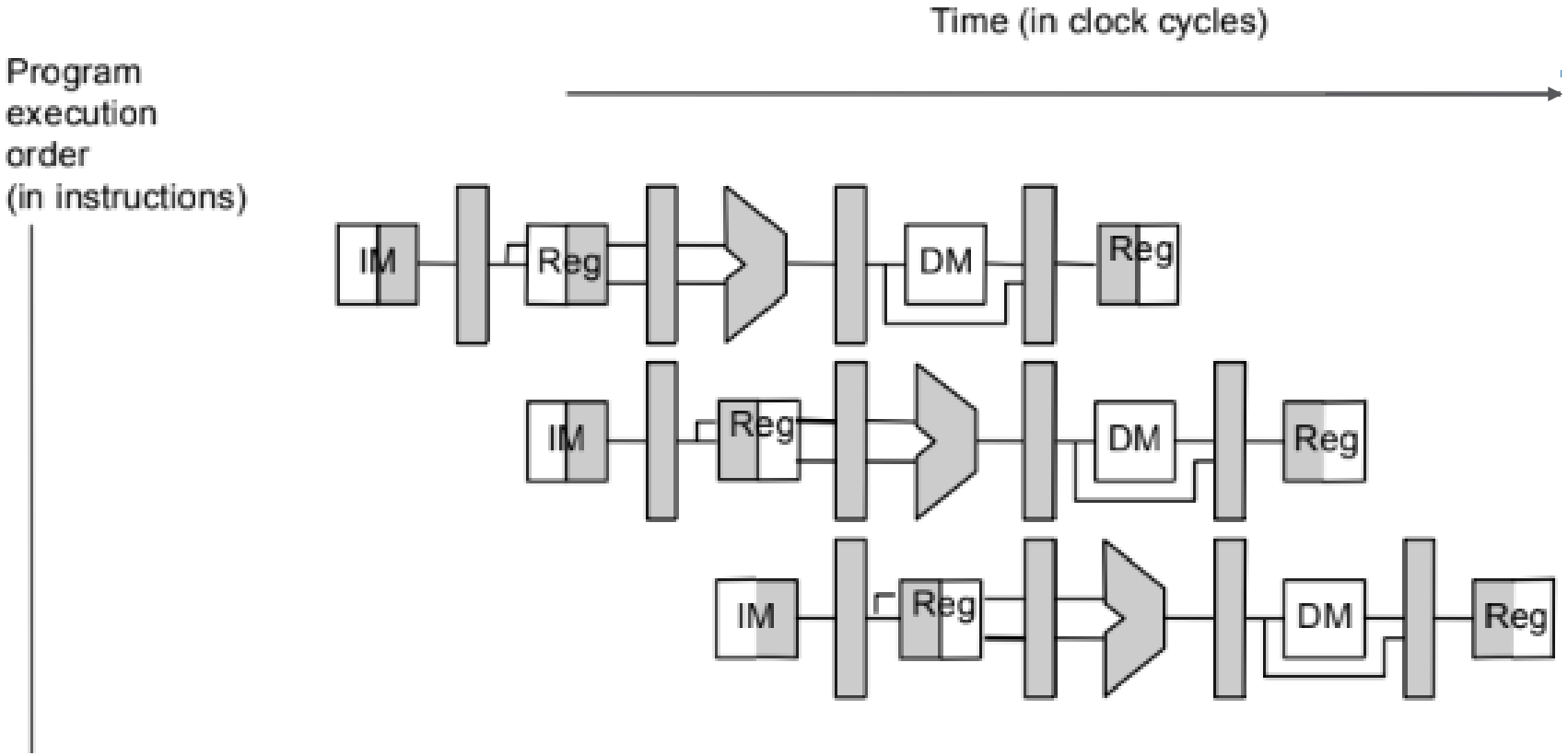

IF/ID
ID/EX
EX/MEM
MEM/WB
Add
4
M u x
0
1
PC
Address
Instruction memory
Instruction
Read register 1
Read register 2
Registers
Write register
Write data
Read data 1
Read data 2
32
Imm Gen
Shift left 1
Add Sum
ALU
Zero
ALU result
Address
Read data
Data memory
Write data


Time (in clock cycles)
Program execution order (in instructions)
IM
Reg
DM
Reg
IM
Reg
DM
Reg
IM
Reg
DM
Reg

What is between stages?

-Flip Flop

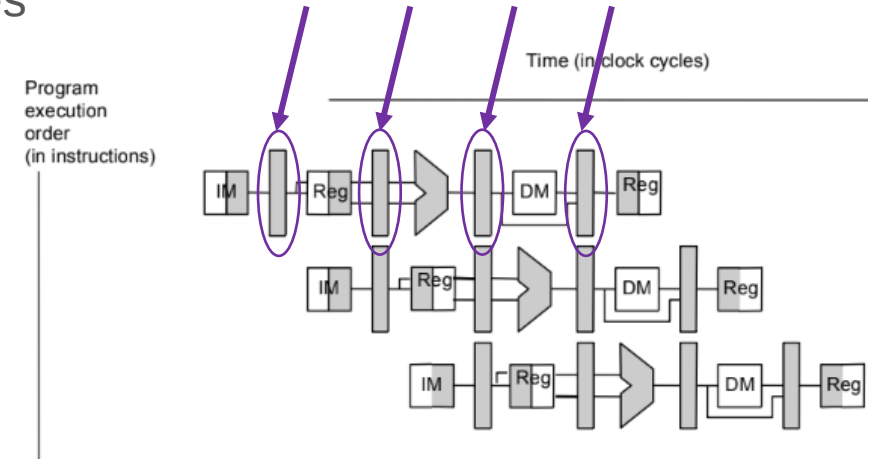
-Value out (Q) updates on next clock cycle

-Note: for this course, doesn't matter actual implementation. As long as we are synchronizing data between stages

-Values that go into Flip Flop?

-Data

-Control signals



Half Cycle?

-Data stored in register file in the writeback stage of one instruction will be ready in time for the decode stage of another instruction