7 Processes

in some way.

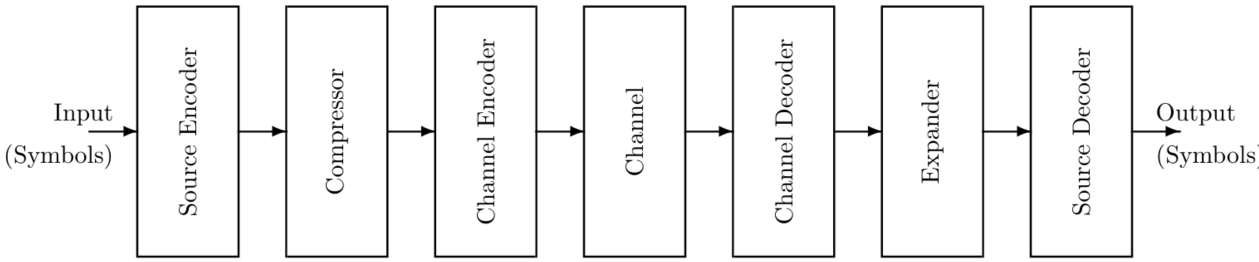

Figure 7.1: Communication system

Figure 7.1 shows the module inputs and outputs and how they are connected. A diagram like this is very useful in portraying an overview of the operation of a system, but other representations are also useful. In this chapter we develop two abstract models that are general enough to represent each of these boxes in Figure 7.1, but show the flow of information quantitatively.

Because each of these boxes in Figure 7.1 processes information in some way, it is called a **processor** and what it does is called a **process**. The processes we consider here are

5个特点，稍微了解一下

- **Discrete:** The inputs are members of a set of mutually exclusive possibilities, only one of which occurs at a time, and the output is one of another discrete set of mutually exclusive events.
- **Finite:** The set of possible inputs is finite in number, as is the set of possible outputs.
- **Memoryless:** The process acts on the input at some time and produces an output based on that input, ignoring any prior inputs.

- **Nondeterministic:** The process may produce a different output when presented with the same input a second time (the model is also valid for deterministic processes). Because the process is nondeterministic the output may contain random **noise**.
- **Lossy:** It may not be possible to "see" the input from the output, i.e., determine the input by observing the output. Such processes are called **lossy** because knowledge about the input is lost when the output is created (the model is also valid for lossless processes).

1 Types of Process Diagrams

四种类型，稍微了解一下

- **Block Diagram:** Figure 7.1 (previous page) is a block diagram. It shows how the processes are connected, but very little about how the processes achieve their purposes, or how the connections are made. It is useful for viewing the system at a highly abstract level. An interconnection in a block diagram can represent many bits.
- **Circuit Diagram:** If the system is made of logic gates, a useful diagram is one showing such gates interconnected. For example, Figure 7.2 is an *AND* gate. Each input and output represents a wire with a single logic value, with, for example, a high voltage representing 1 and a low voltage 0. The number of possible bit patterns of a logic gate is greater than the number of physical wires; each wire could have two possible voltages, so for n-input gates there would be 2^n possible input states. Often, but not always, the components in logic circuits are deterministic.
- **Probability Diagram:** A process with n single-bit inputs and m single-bit outputs can be modeled by the probabilities relating the 2^n possible input bit patterns and the 2^m possible output patterns. For example, Figure 7.3 (next page) shows a gate with two inputs (four bit patterns) and one output. An example of such a gate is the *AND* gate, and its probability model is shown in Figure 7.4. Probability diagrams are discussed further in Section 7.2.
- **Information Diagram:** A diagram that shows explicitly the information flow between processes is useful. In order to handle processes with noise or loss, the information associated with them can be shown. Information diagrams are discussed further in Section 7.6.

3 Information, Loss, and Noise

$$I = \sum_i p(A_i) \log_2 \left(\frac{1}{p(A_i)} \right)$$

$$L = \sum_j p(B_j) \sum_i p(A_i \mid B_j) \log_2 \left(\frac{1}{p(A_i \mid B_j)} \right)$$

$$M = I - L$$

$$0 \le M \le I$$

$$0 \le L \le I$$

$$
\begin{aligned}
N &= \sum_i p(A_i) \sum_j p(B_j \mid A_i) \log_2 \left(\frac{1}{p(B_j \mid A_i)} \right) \\
&= \sum_i p(A_i) \sum_j c_{ji} \log_2 \left(\frac{1}{c_{ji}} \right)
\end{aligned}
$$

mples

above for loss show analogous results. What may not be obvious l information M plays exactly the same sort of role for noise ise to other information measures are like those for loss above, ne:

$$J = \sum_i p(B_j) \log_2 \left(\frac{1}{p(B_j)} \right)$$

$$N = \sum_i p(A_i) \sum_j c_{ji} \log_2 \left(\frac{1}{c_{ji}} \right)$$

$$M = J - N$$

$$M = J - N \tag{7.24}$$

$$0 \leq M \leq J \tag{7.25}$$

$$0 \leq N \leq J \tag{7.26}$$

It follows from these results that

$$J - I = N - L \tag{7.27}$$

7.3.1 Example: Symmetric Binary Channel

For the SBC with bit error probability ε, these formulas can be evaluated, even if the two input probabilities $p(A_0)$ and $p(A_1)$ are not equal. If they happen to be equal (each 0.5), then the various information measures for the SBC in bits are particularly simple:

$$I = 1 \text{ bit} \tag{7.28}$$

$$J = 1 \text{ bit} \tag{7.29}$$

$$L = N = \varepsilon \log_2 \left(\frac{1}{\varepsilon}\right) + (1-\varepsilon) \log_2 \left(\frac{1}{1-\varepsilon}\right) \tag{7.30}$$

$$M = 1 - \varepsilon \log_2 \left(\frac{1}{\varepsilon}\right) - (1-\varepsilon) \log_2 \left(\frac{1}{1-\varepsilon}\right) \tag{7.31}$$

The errors in the channel have destroyed some of the information, in the sense that they have prevented an observer at the output from knowing with certainty what the input is. They have thereby permitted only the amount of information $M = I - L$ to be passed through the channel to the output.

7.4 Deterministic Examples

5 Capacity

$$C = W M_{max}$$

以对称二进制信道（SBC）为例来说明M_{max}：

对称二进制信道介绍

在对称二进制信道中，输入符号集为$\{0,1\}$，输出符号集也为$\{0,1\}$。存在一个交叉概率p，即当输

出为1的概率是p；当输入为1时，输出为0的概率也是p，而正确传输的概率为$1-p$。

计算不同输入概率分布下的互信息M

设输入X取0的概率为π，则取1的概率为$1-\pi$；输出为Y。根据互信息公式

$I(X;Y)=\sum_x\sum_y p(x,y)\log\frac{p(x,y)}{p(x)p(y)}$，先计算联合概率分布$p(x,y)$：

- 当$x=0,y=0$时，$p(0,0)=(1-p)\pi$；当$x=0,y=1$时，$p(0,1)=p\pi$。
- 当$x=1,y=0$时，$p(1,0)=p(1-\pi)$；当$x=1,y=1$时，$p(1,1)=(1-p)(1-\pi)$。

将这些概率代入互信息公式进行计算，得到互信息M（即$I(X;Y)$）是关于π的函数：

$I(X;Y)=H(Y)-H(Y|X)$

其中$H(Y)$是输出Y的熵，$H(Y|X)$是已知输入X时输出Y的条件熵。计算可得：

$H(Y)=-\sum_y p(y)\log_2 p(y)$

$$H(Y|X) = -\sum_x \sum_y p(x,y) \log_2 p(y|x)$$

由于信道的对称性，$H(Y|X) = -[\pi \log_2 p + (1-\pi) \log_2 p] = \pi h(p) + (1-\pi) h(p) = h(p)$，其中 $h(p) = -p \log_2 p - (1-p) \log_2 (1-p)$是二进制熵函数。

所以$I(X;Y) = H(Y) - h(p)$，它随着π变化。

求M_{max}

通过对$I(X;Y)$关于π求极值（或者从信息论原理可知），当$\pi = 0.5$（即输入0和1的概率相等）时，$H(Y)$取得最大值1（因为此时输出的不确定性最大），此时互信息$I(X;Y)$也取得最大值$1-h(p)$。这个最大值$1-h(p)$就是M_{max}。

也就是说，在对称二进制信道中，当输入符号0和1以等概率出现时，输入和输出之间的互信息达到最大，这个最大互信息值就是M_{max}，它在计算信道容量等方面有重要应用，比如该信道容量$C = W(1-h(p))$（W为在输出端能够检测到输入状态的最大速率）。

一图胜千言：