Computer Architecture Lab
Assignment 6

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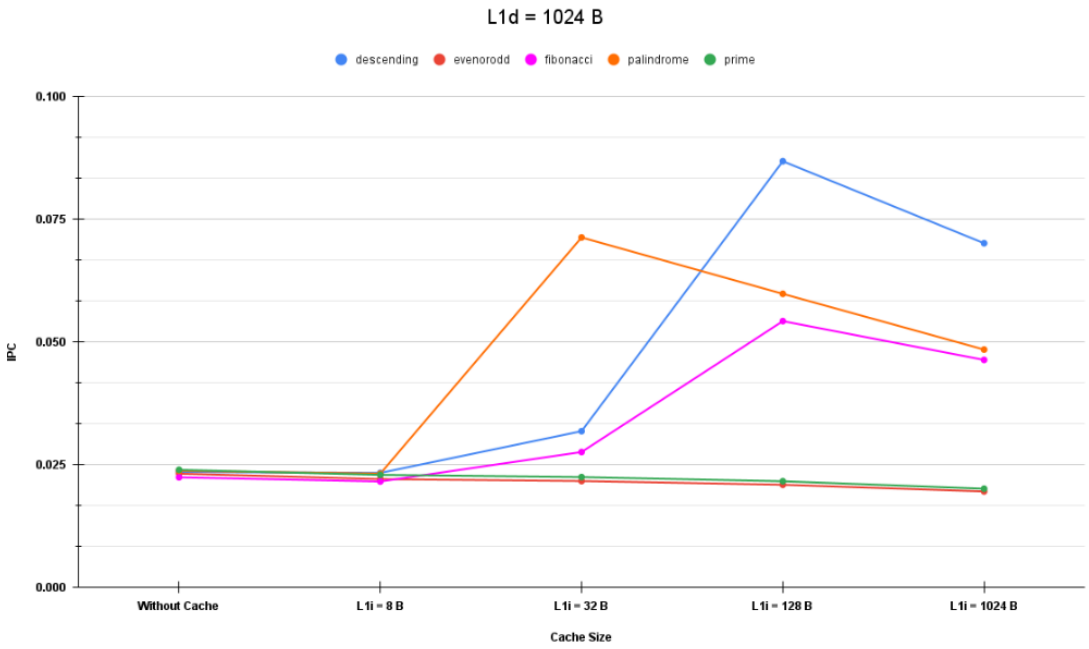
The size of the L1d-cache fixed at 1KB

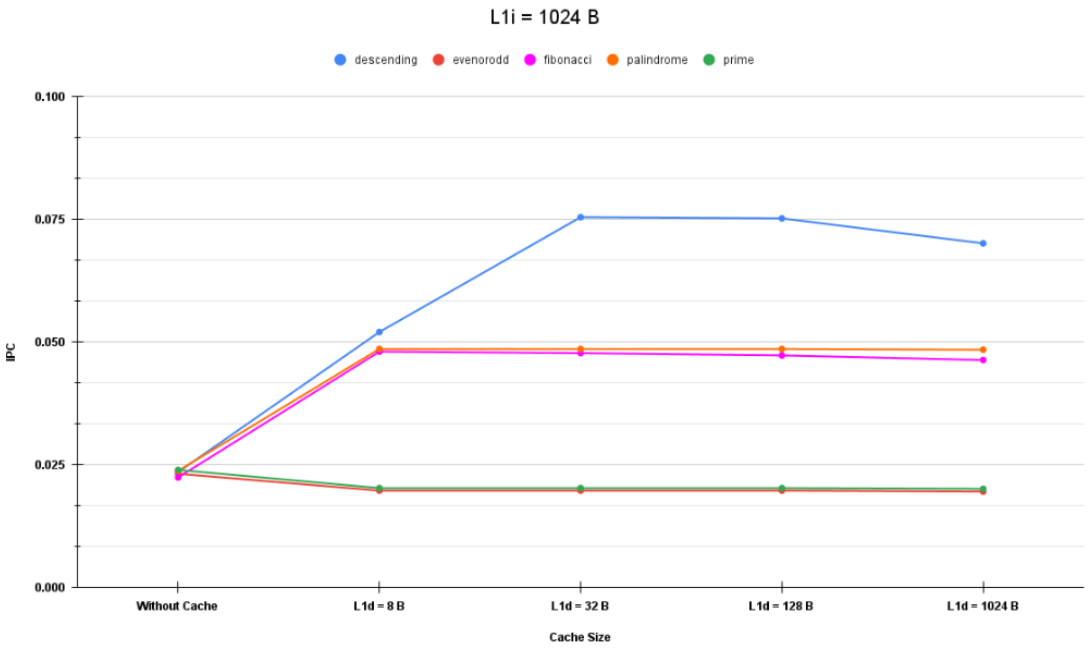
Program	without cache	L1i = 8B	L1i = 32B	L1i = 128B	L1i = 1024B
descending.asm	0.0235	0.0233	0.0318	0.0869	0.0701
evenorodd.asm	0.0232	0.0220	0.0217	0.0209	0.0195
fibonacci.asm	0.0224	0.0216	0.0276	0.0543	0.0464
palindrome.asm	0.0238	0.0232	0.0713	0.0598	0.0485
prime.asm	0.0239	0.0229	0.0224	0.0216	0.0201



Hit rate and latency both rise as the capacity of the L1i cache does.There will be an optimum size of L1i cache where IPC is highest.

The size of the L1i-cache fixed at 1KB

Program	without cache	L1d = 8B	L1d = 32B	L1d = 128B	L1d = 1024B
descending.asm	0.0235	0.0521	0.0755	0.0752	0.0701
evenorodd.asm	0.0232	0.0197	0.0197	0.0197	0.0195
fibonacci.asm	0.0224	0.0481	0.0478	0.0473	0.0464
palindrome.asm	0.0238	0.0486	0.0486	0.0486	0.0485
prime.asm	0.0239	0.0202	0.0202	0.0202	0.0201



Here also the latency increases with increment in cache size and hit rate also increases. There will be an optimum size of L1d cache where IPC is maximum.