Computer Architecture Lab Assignment 6

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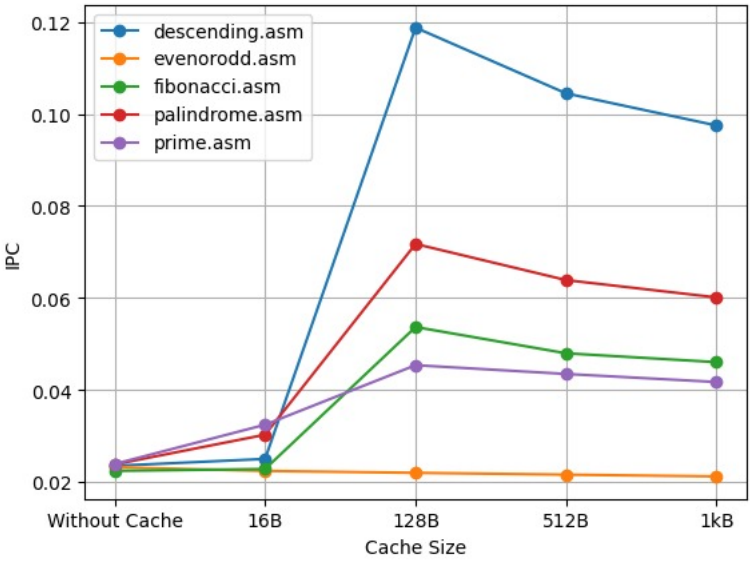
The size of the L1d-cache fixed at 1KB

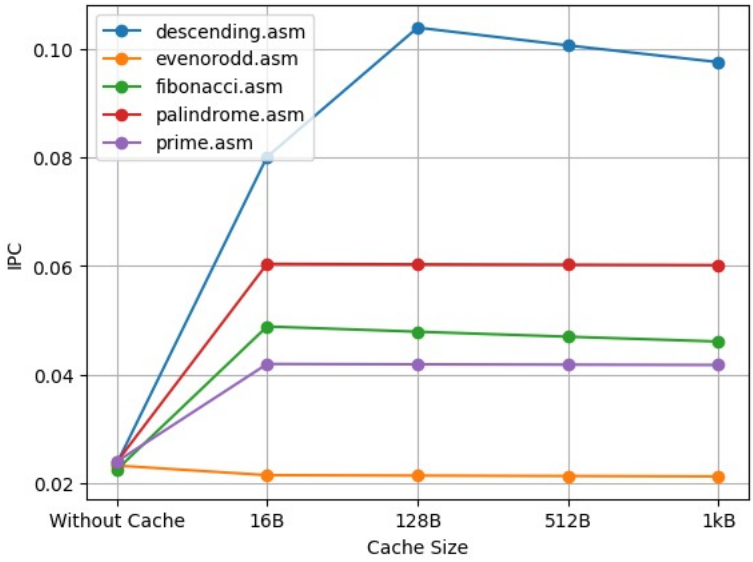
Program	Without Cache	L1i = 16B	L1i = 128B	L1i = 512B	L1i = 1kB
`descending.asm`	0.0235	0.025002256	0.11878216	0.10448887	0.09750088
`evenorodd.asm`	0.0232	0.02238806	0.021978023	0.021582734	0.021201413
`fibonacci.asm`	0.0224	0.022807017	0.053682037	0.04797048	0.046044864
`palindrome.asm`	0.0238	0.030265596	0.07174231	0.063885264	0.0601227
`prime.asm`	0.0239	0.03243848	0.045383412	0.04347826	0.04172662

Hit rate and latency both rise as the capacity of the L1i cache does. There will be an optimum size of L1i cache where IPC is highest.



The size of the L1i-cache fixed at 1KB

Program	Without Cache	L1i = 16B	L1i = 128B	L1i = 512B	L1i = 1kB
`descending.asm`	0.0235	0.0800578	0.10386202	0.100580975	0.09750088
`evenorodd.asm`	0.0232	0.021428572	0.021352313	0.021276595	0.021201413
`fibonacci.asm`	0.0224	0.048811015	0.047852762	0.04693141	0.046044864
`palindrome.asm`	0.0238	0.060344826	0.060270604	0.06019656	0.0601227
`prime.asm`	0.0239	0.041907515	0.041847043	0.041786745	0.04172662



Here also the latency increases with increment in cache size and hit rate also increases. There will be an optimum size of L1d cache where IPC is maximum.

Toy-benchmark that shows significant performance improvement when the L1i-cache is increased from 16B to 128B

L1i
16B - 0.027904216
128B - 0.31057268

Toy-benchmark that shows significant performance improvement when the L1d-cache is increased from 16B to 128B

L1d
16B - 0.030095352
128B - 0.1684938