ASM CHART FOR THE IMAGE FILTER

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S00

x<='0'

Start=1 — 0

S_wait

start='1' — 0

Start=1 → 1

done<='1'; busy<='0'

filter_type='1' → 1

busy<='1'; read_s_rom<='1'
ts<=0

busy<='1'; read_s_rom<='1'
ts<=16;

S0

1

x='0' — 0 → co=157 — 1 → ro=117

x='0' → 1

c0<=0;ro<=0;
x<='0'; address_to_write<=32768

co<=co+1;
address_to_write<=address_to_write+1

ro<=ro+1;co<=0;
address_to_write<=address_to_write+1;

S1 control_to_mac<='0'; write_s_ram<='0'; read_s_ram<='1'; address_rom<=ts; address_ram<=ro*160+co;
data1_to_mac<=0; data2_to_mac<=0

S2 control_to_mac<='0'; write_s_ram<='0'; read_s_ram<='1'; address_rom<=ts+1; address_ram<=ro*160+co+1;
data1_to_mac<=data_from_ram; data2_to_mac<=data_from_rom;

S3 control_to_mac<='1'; write_s_ram<='0'; read_s_ram<='1'; address_rom<=ts+2; address_ram<=ro*160+co+2;
data1_to_mac<=data_from_ram; data2_to_mac<=data_from_rom;

S4 control_to_mac<='1'; write_s_ram<='0'; read_s_ram<='1'; address_rom<=ts+3; address_ram<=ro*160+co+160;
data1_to_mac<=data_from_ram; data2_to_mac<=data_from_rom;

S5 control_to_mac<='1'; write_s_ram<='0'; read_s_ram<='1'; address_rom<=ts+4; address_ram<=ro*160+co+161;
data1_to_mac<=data_from_ram; data2_to_mac<=data_from_rom;

S6 control_to_mac<='1'; write_s_ram<='0'; read_s_ram<='1'; address_rom<=ts+5; address_ram<=ro*160+co+162;
data1_to_mac<=data_from_ram; data2_to_mac<=data_from_rom;

S7 control_to_mac<='1'; write_s_ram<='0'; read_s_ram<='1'; address_rom<=ts+6; address_ram<=ro*160+co+320;
data1_to_mac<=data_from_ram; data2_to_mac<=data_from_rom;

S8 control_to_mac<='1'; write_s_ram<='0'; read_s_ram<='1'; address_rom<=ts+7; address_ram<=ro*160+co+321;
data1_to_mac<=data_from_ram; data2_to_mac<=data_from_rom;

S9 control_to_mac<='1'; write_s_ram<='0'; read_s_ram<='1'; address_rom<=ts+8; address_ram<=ro*160+co+322;
data1_to_mac<=data_from_ram; data2_to_mac<=data_from_rom;

S10 control_to_mac<='1'; write_s_ram<='0'; read_s_ram<='1'; data1_to_mac<=data_from_ram;
data2_to_mac<=data_from_rom;

S11 control_to_mac<='1'; write_s_ram<='1'; read_s_ram<='0'; data1_to_mac<=0; data2_to_mac<=0;

data_to_ram<=0 ← 1 — data_from_mac < 0

data_to_ram<=data_from_mac (14 downto 7) ← 0
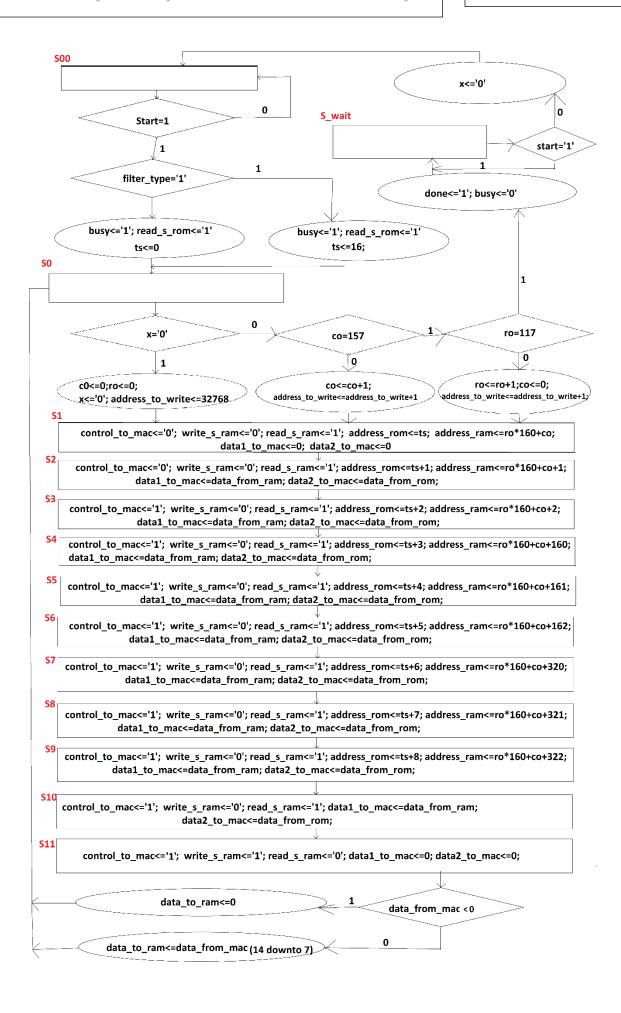
NOTE: This ASM chart defines the working of part_d component. It shows the control signal given by part_d to the other components. The term used in this chart have the same meaning as in the VHDL code. The signal meanings are explained in the design overview part.