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DIGITAL CLOCK

ASSIGNMENT 2- COL 215

EXPLANATION OF VHDL CODE

In this section, I will explain the VHDL code for the digital clock. There are 10 components in my model. The explanation of the code for each of the entity is given below.

Architecture manual1 of Entity manual:

Explanation of the ports: 'Clk' takes the input from the output of the master clock. 'Resetn' initialises all the signals to initial states. 'w' takes input from a push button if user wants to manually set the time. 'z' gives the output if the user wants to set the time manually.

Explanation of the signals: 'temp' stores that the push button is pressed and it transfers this information to 'temp1' at the next positive clock edge.

Explanation of the code: The asynchronous command by the user to manually set time is turned into synchronous output as the 'temp1' signal is updated only at the rising clock edge and the output 'z' depends on 'temp1'.

Architecture setting1 of Entity setting:

Explanation of the ports:'Clk' takes input from the master clock. 'Resetn' is used to initialise the system to initial state. 'w' takes the input of the push button. 's' takes the input if the user has selected for setting the time manually. 'z' gives the output which digit will be changed.

Explanation of the signals: 'state', 'state1' are state_type signals which denotes the state the component is in at the instant.

Explanation of the code: This architecture implements the FSM model shown in 1st pdf of this assignment. Since the user presses the push button asynchronously the 'state' signal changes at the instant the user presses the button but its effect on the output is shown only through 'state1' which is updated only at the rising clock edge. Thus, the component acts synchronously.

Architecture incrementer1 of Entity incrementer:

Explanation of the ports: 'Clk' takes input from the master clock. 'Resetn' is used to initialise the system to initial state. 'w' is the input corresponding to the push button. 'mode' states which digit is to be incremented. 'h0','h1','m0','m1','s0','s1' gives the output as the time set by the user.

Explanation of the signals: 'state' stores the state the component is in corresponding to its FSM. 'curr_mode' stores the digit to be changed. 'th0','th1','tm0','tm1','ts0','ts1' stores the current time manually set. 't' and 'count' just states that 0.2 sec has been completed.

Explanation of the code: The overall working of the code is based on the FSM model shown in the 1st PDF of this assignment. It distinguishes between the long push and short push by noting the time for which the button was pressed. If pressed for more then 0.8 sec, it is treated as long push.

Architecture clock1 of Entity clock

Explanation of the ports: 'Clk' takes input from the master clock. 'Resetn' is used to initialise the system to initial state. H0_in, H1_in, M0_in, M1_in, S0_in, S1_in takes manual time set by user if user wants to set the time manually. H0_out, H1_out, M0_out, M1_out, S0_out, S1_out gives the current time. H1 stands for tens digit of hour and H0 stands for ones digit of hour. Similarly for minutes and seconds.

Explanation of the signals: th0,th1,tm0,tm1,ts0,ts1 stores the time that is assigned to the output terminals. 'count' is used to compute 1 sec from 250 Hz master clock.

Explanation of the code: The 'count' signal just keep counting the just of rising edges of the master signal and after every 250 cycles, time is increased by one.

Architecture mode1 of Entity mode:

Explanation of the ports: 'Clk' takes input from the master clock. 'Resetn' is used to initialise the system to initial state. 'w' takes input from user to select the mode in which the time is to be displayed. H0, H1, M0, M1, S0, S1 are inputs from the clock entity. x1,x0,y1,y0 are the 4 outputs corresponding to the mode. 'blink' output says the mode in which the decimal point has to blink.

Explanation of the signals: 'temp' stores the mode till the next rising clock edge. 'temp1' takes the value from 'temp' at the rising edge.

Explanation of the code: The user gives the input asynchronously, but the output is synchronous since the output depends on the 'temp1' signal which is updated only at the rising clock edge.

Architecture seg_decoder1 of seg_decoder:

Explanation of the ports: 'x' is the input in digit in binary form. 'y' is the output corresponding to cathodes of 7-segment display.

Explanation of the code: It simply matches the binary form to corresponding form required for 7-segment display.

Architecture clk_display1 of Entity clk_display:

Explanation of the ports: 'clk' takes input from the master clock. 'resetn' is used to initialise the system to initial state. 'y' is the output that goes to the multiplexer to select one active digit during that cycle. 'z' is the output to the anode that which anode should be active during the cycle.

Explanation of the signals:'ty' and 'tz' temporarily stores the output.

Explanation of the code: At every clock edge (i.e. every 4 ms), the component changes the active display sequentially.

Architecture clk250Hz1 of Entity clk250Hz:

Explanation of the ports: 'Clk' takes input from the clock on the basys board. 'Resetn' is used to initialise the system to initial state. 'clk_out' outputs the reduced frequency clock signal.

Explanation of the signals: 't' stores the current output. 'count' maintains the no. of cycles completed by the clock provided on the basys board.

Explanation of the code: The component simply toggles the output after every 40000 cycles of the clock provided by the basys board.

Architecture decimal1 of Entity deci:

Explanation of the ports: 'clk' takes input from the master clock. 'resetn' is used to initialise the system to initial state. 'blink' takes the input if the decimal point is to blinked in the current mode. 'display_no' states which out of 4 seven-segments display is active in the current cycle.

Explanation of the signals: 't' stores if the decimal should be 'on' or 'off' at the current instant. 'count' helps to toggle 't' at frequency of 2Hz by maintaining no. of cycles completed by master clock.

Explanation of the code: The code gives a '0' (low voltage at cathode) output when decimal should be bright and '1' (high voltage at cathode) when it is not bright.

Architecture multiplexer 1 of Entity multiplexer:

Explanation of the ports: x1, x0, y1, y0 are the four digits that are to be displayed. 's' gives which digit should be active in the current cycle. 'X' gives the corresponding digit.

Explanation of the code: It simply selects the output based on the input signal 's'.

Architecture digi_clock of Entity digital_clock:

Explanation of the ports: 'CLK', 'RESET', 'SET_TIME', 'PLUS', 'MODE', 'CHANGE_DIGIT' are inputs from the basys board. 'OUT_ANODE','OUT_CATHODE','OUT_DECIMAL' are outputs for the cathodes and anodes.

Explanation of the signals: all the signals in this component just carry the information between different terminals of different components.

Explanation of the code: This describes the connection between all the components that makes the model a working model.