COL 215 ASSIGNMENT 1

Name- Aniket Gupta

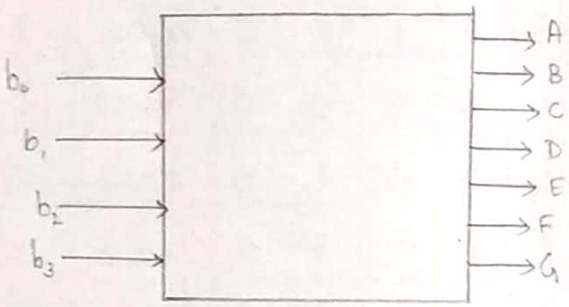
Entry No.- 2019CS10327

Problem-2

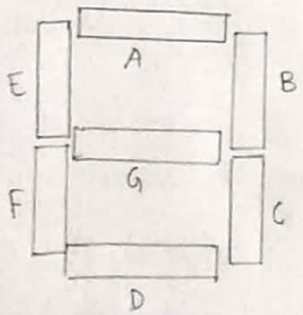
My Entry No.- 2019CS10327

$\Rightarrow M = 20190327$

$\Rightarrow S = \{0, 1, 2, 3, 7, 9\}$



Representation of a binary to seven segment convertor



A Representation of the digital board on which the digits will appear. Output 1 from any output terminal makes the corresponding segment lighten up.

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The table showing the different inputs and the corresponding required outputs is as follow:

← INPUTS →						← OUTPUTS →						
Dec	Binary	b_3	b_2	b_1	b_0	A	B	C	D	E	F	G
0	0000	0	0	0	0	1	1	1	1	1	1	0
1	0001	0	0	0	1	0	1	1	0	0	0	0
2	0010	0	0	1	0	1	1	0	1	1	0	1
3	0011	0	0	1	1	1	1	1	1	0	0	1
4	0100	0	1	0	0	0	1	1	0	0	1	1
5	0101	0	1	0	1	1	0	1	1	0	1	1
6	0110	0	1	1	0	1	0	1	1	1	1	1
7	0111	0	1	1	1	1	1	1	0	0	0	0
8	1000	1	0	0	0	1	1	1	1	1	1	1
9	1001	1	0	0	1	1	1	1	1	0	1	1

For the first design, (i.e., 7 separate circuits, each with 4 inputs and one output), we will draw the truth table corresponding to the seven segments separately, and then find a simplified (ie) logical expression for each segment using Karnaugh Map.

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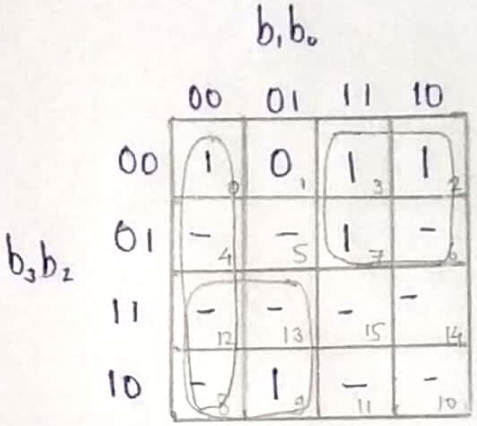
Circuit for segment - A

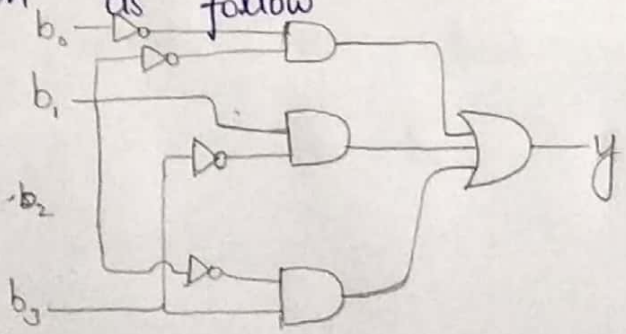
	b_3	b_2	b_1	b_0	y
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	-
5	0	1	0	1	-
6	0	1	1	0	-
7	0	1	1	1	1
8	1	0	0	0	-
9	1	0	0	1	1



From the Kernough Map, the logical expression for the segment A is

$$y = \boxed{(b_1 \cdot b_3') + (b_1' \cdot b_3) + (b_1' \cdot b_0')}$$

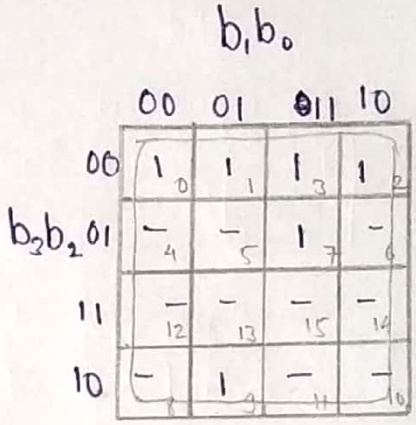
The logical circuit for segment - A is can be drawn as follow



~~Cost function =~~

Circuit for Segment B

	b_3	b_2	b_1	b_0	y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	-
5	0	1	0	1	-
6	0	1	1	0	-
7	0	1	1	1	1
8	1	0	0	0	-
9	1	0	0	1	1



From the Kernough Map

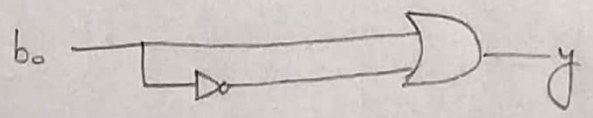
$$\boxed{y = 1}$$

which means, the output should always be 1.

It can be shown in many ways.

One way to show $y = 1$ is $y = b_0 + b_0'$

logic circuit



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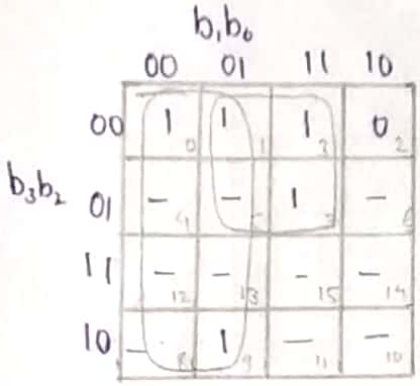
Circuit for segment c

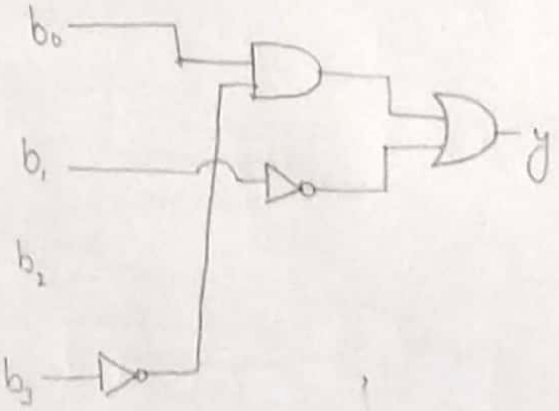
	b_3	b_2	b_1	b_0	y
0	0	0	0	0	1
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	-
5	0	1	0	1	-
6	0	1	1	0	-
7	0	1	1	1	1
8	1	0	0	0	-
9	1	0	0	1	1



Kernaugh Map for segment c gives.

$$y = (b_0 \cdot b_3') + b_1'$$

The logic circuit for segment c



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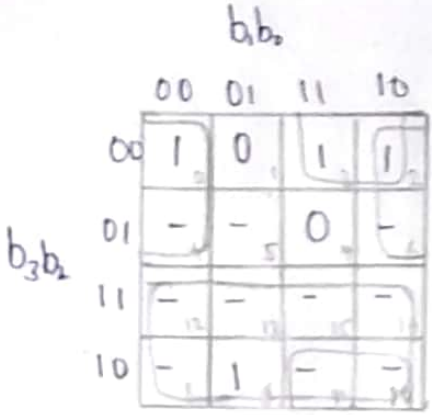
Circuit for segment D

	b_3	b_2	b_1	b_0	y
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	-
5	0	1	0	1	-
6	0	1	1	0	-
7	0	1	1	1	0
8	1	0	0	0	-
9	1	0	0	1	1

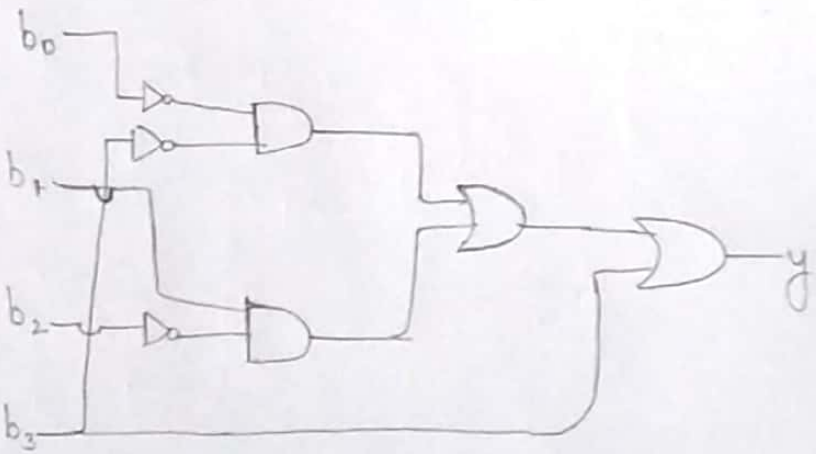


Kernaugh Map for segment D

gives

$$y = (b_3' \cdot b_0') + (b_1 \cdot b_2') + b_3$$

logic circuit for segment D



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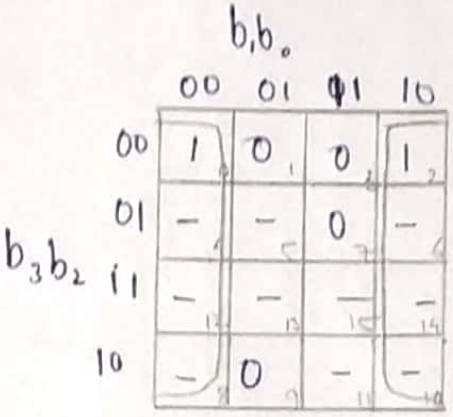
Circuit for segment E

	b_3	b_2	b_1	b_0	y
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	0
4	0	1	0	0	-
5	0	1	0	1	-
6	0	1	1	0	-
7	0	1	1	1	0
8	1	0	0	0	-
9	1	0	0	1	0



From the Kernaugh table, the expression for segment E is

$$y = b_0'$$

logic circuit for segment E

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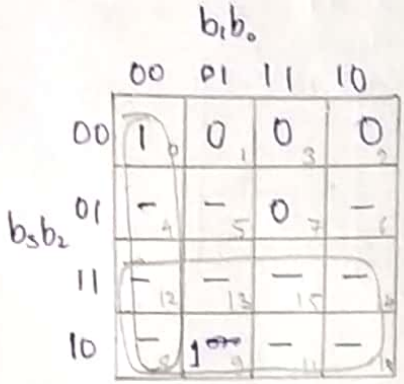
Circuit for segment F

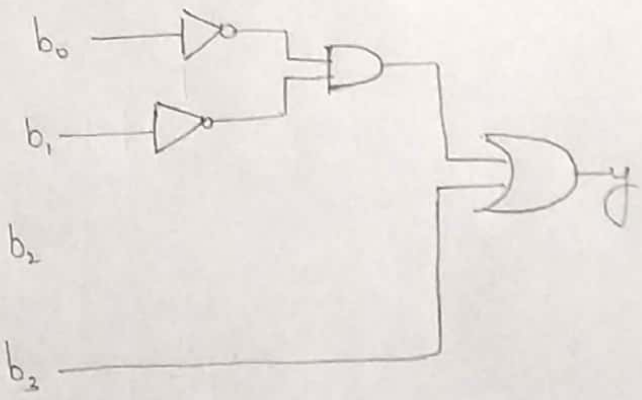
	b_3	b_2	b_1	b_0	y
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	0
3	0	0	1	1	0
4	0	1	0	0	-
5	0	1	0	1	-
6	0	1	1	0	-
7	0	1	1	1	0
8	1	0	0	0	-
9	1	0	0	1	1



The kernaugh map gives

$y = b_1' \cdot b_0' + b_3$

Logic circuit for segment F



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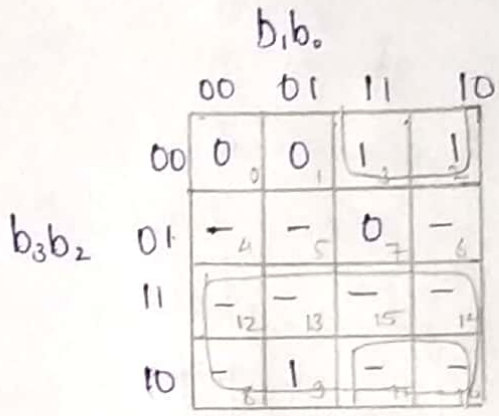
Circuit for segment G

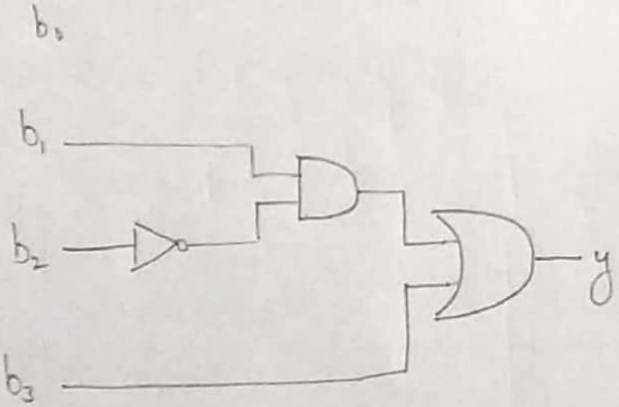
	b_3	b_2	b_1	b_0	y
0	0	0	0	0	0
1	0	0	0	1	0
2	0	0	1	0	1
3	0	0	1	1	1
4	0	1	0	0	-
5	0	1	0	1	-
6	0	1	1	0	-
7	0	1	1	1	0
8	1	0	0	0	-
9	1	0	0	1	1



The kernaugh Map gives

$$y = (b_1 \cdot b_2') + b_3$$

Thus, the logic circuit for segment G is



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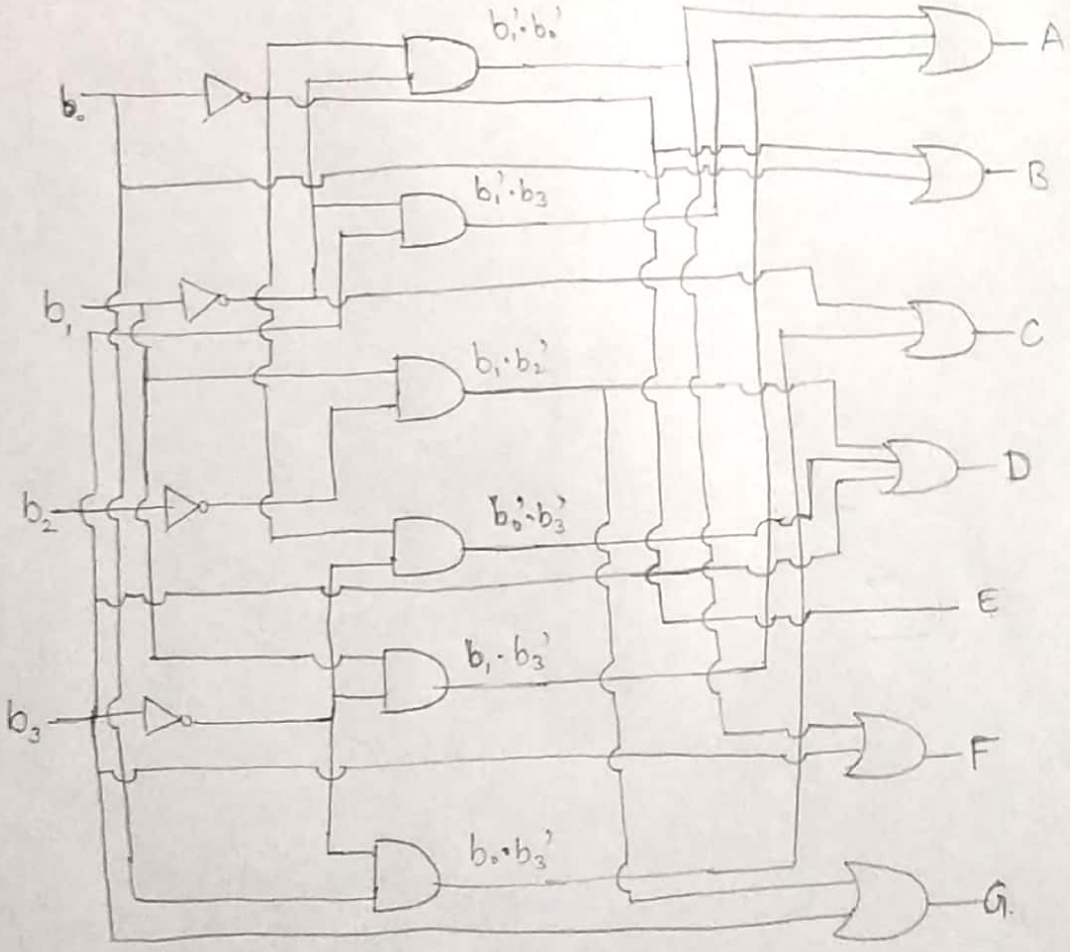
Design 2 with sharing of gates

In this, we will use the expressions derived in the separate circuit case. The terms which have occured multiple times will be replaced by their single use. Note, term $b_1 \cdot b_2'$ has occured both in segments D and G. Similarly, $b_1' \cdot b_3'$ occurs both in segments A and F. Such parts can be shared in a combined circuit.



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