COL215 ASSIGNMENT 1

NAME – ANIKET GUPTA

ENTRY NO. – 2019CS10327

PROBLEM 2: DESCRIPTION OF THE PROCEDURE

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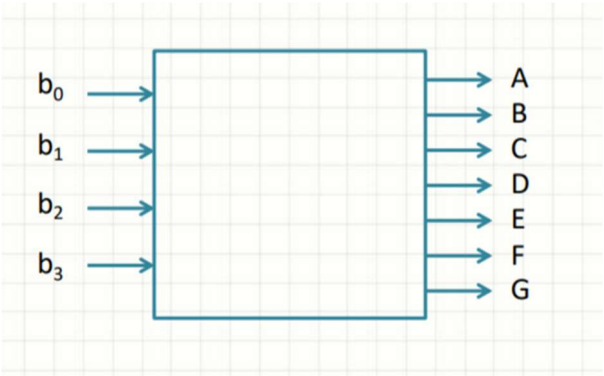
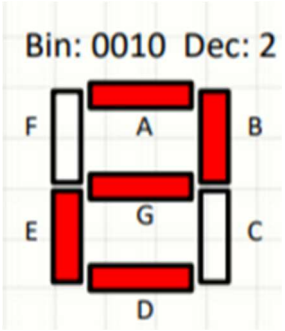
Thus, M = 20190327

S = {0,1,2,3,7,9}

NOTE: I have added the below pictures just for clarity (taking an example when we represent the digit 2)





PROCEDURE FOR THE FIRST MODEL WITH 7 SEPARATE CIRCUITS, EACH WITH 4 INPUTS AND ONE OUTPUT:

- First of all, the table for the inputs and the outputs for the different digits in S is drawn. This shows that we feed the digits in the binary representation to the four input terminals respectively. For example, if we want to represent 3, then we give the inputs 0,0,1,1 to b_3 ,b_2 ,b_1 ,b_0 respectively. This will cause the output terminals A ,B ,C ,D and G to give 1 as output and the other remaining terminals to give 0 as output. The table is shown below:

DEC	BIN	A	B	C	D	E	F	G
0	0000	1	1	1	1	1	1	0

1	0001	0	1	1	0	0	0	0
2	0010	1	1	0	1	1	0	1
3	0011	1	1	1	1	0	0	1
4	0100	-	-	-	-	-	-	-
5	0101	-	-	-	-	-	-	-
6	0110	-	-	-	-	-	-	-
7	0111	1	1	1	0	0	0	0
8	1000	-	-	-	-	-	-	-
9	1001	1	1	1	1	0	1	1

- For each segment in the output, make separate truth table showing the inputs and the outputs. This is required so that we can analyse the different segments separately.
- Now draw a Karnaugh map for each of the segments using the truth table separately. Drawing Karnaugh map helps to minimise the no. of gates used. Thus, the logical expression becomes simpler than the canonical form.
- While using a Karnaugh map, first group all the 1s (can also include " - ") together in minimum possible number of rectangles whose sides are the power of 2 (i.e. sides of the rectangles can be 1,2,4,8,16……). This helps to group the product terms together that can be simplified.
- Then, each of the rectangles in the Karnaugh map corresponds to a product term in the logical expression.
- Finally, represent all the logical circuits corresponding to the 7 outputs separately using AND, OR, and NOT gates. In this way, all the seven segments act independent of each other.

FOR THE SECOND MODEL WITH SHARING OF GATES:

PROCEDURE:

- First, look for the terms, in the logical expressions for the different segments derived in the first model, that are repeating themselves in different segments.
- The parts of the circuit corresponding to those terms can be drawn only once and used by more than one segments. This is the main method to reduce the number of gates used and thus the total cost.

- Combine all the above separate models by reusing the repeated parts. This gives a 4-input, 7-output logical circuit.