Experiment No.10
Implement Memory design.
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Date of Performance:
Date of Submission:

Aim: To implement Memory design

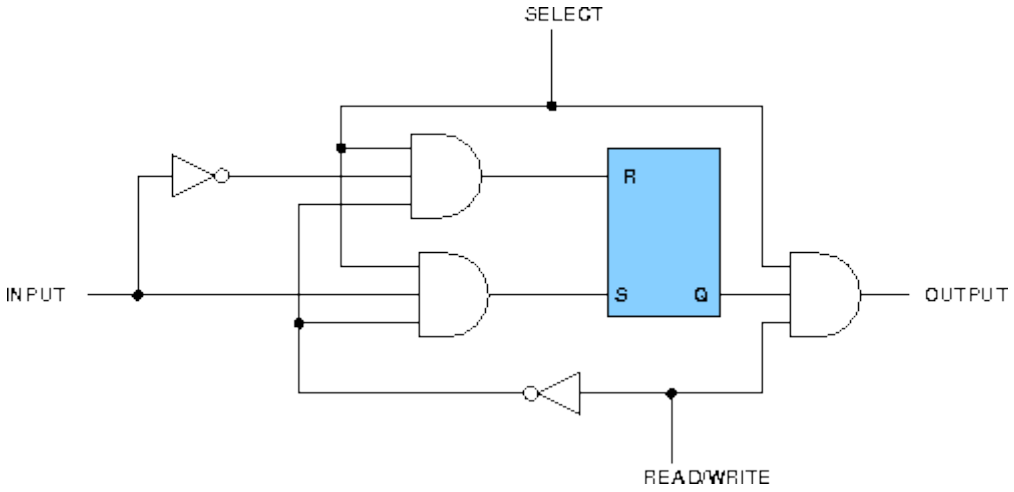
Objective : Objective of 4 bit arithmetic logic unit (with AND, OR, XOR, ADD operation):

1. To understand behaviour of arithmetic logic unit from working module.
2. To Design an arithmetic logic unit for given parameter.

Theory:

Design of Memory :

A memory unit is a collection of storage cells together with associated circuits needed to transform insformation in and out of the device. Memory cells which can be accessed for information transfer to or from any desired random location is called random access memory(RAM). The block diagram of a memory unit-

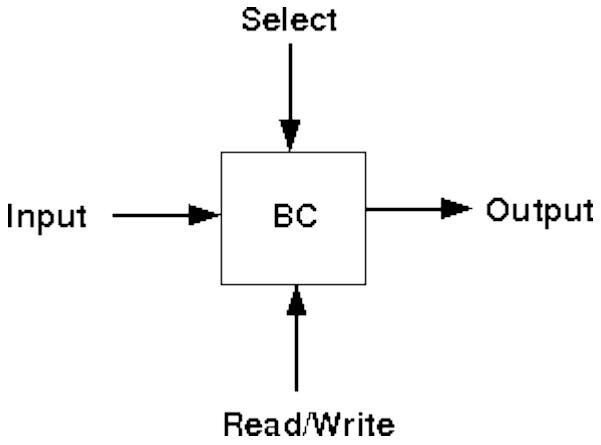


Internal Construction: The internal construction of a random-access memory of m words with n bits per word consists of m*n binary storage cells and associated decoding circuits for selecting individual words. The binary cell is the basic building block of a memory unit.

RAM Design:

Design of a RAM cell :

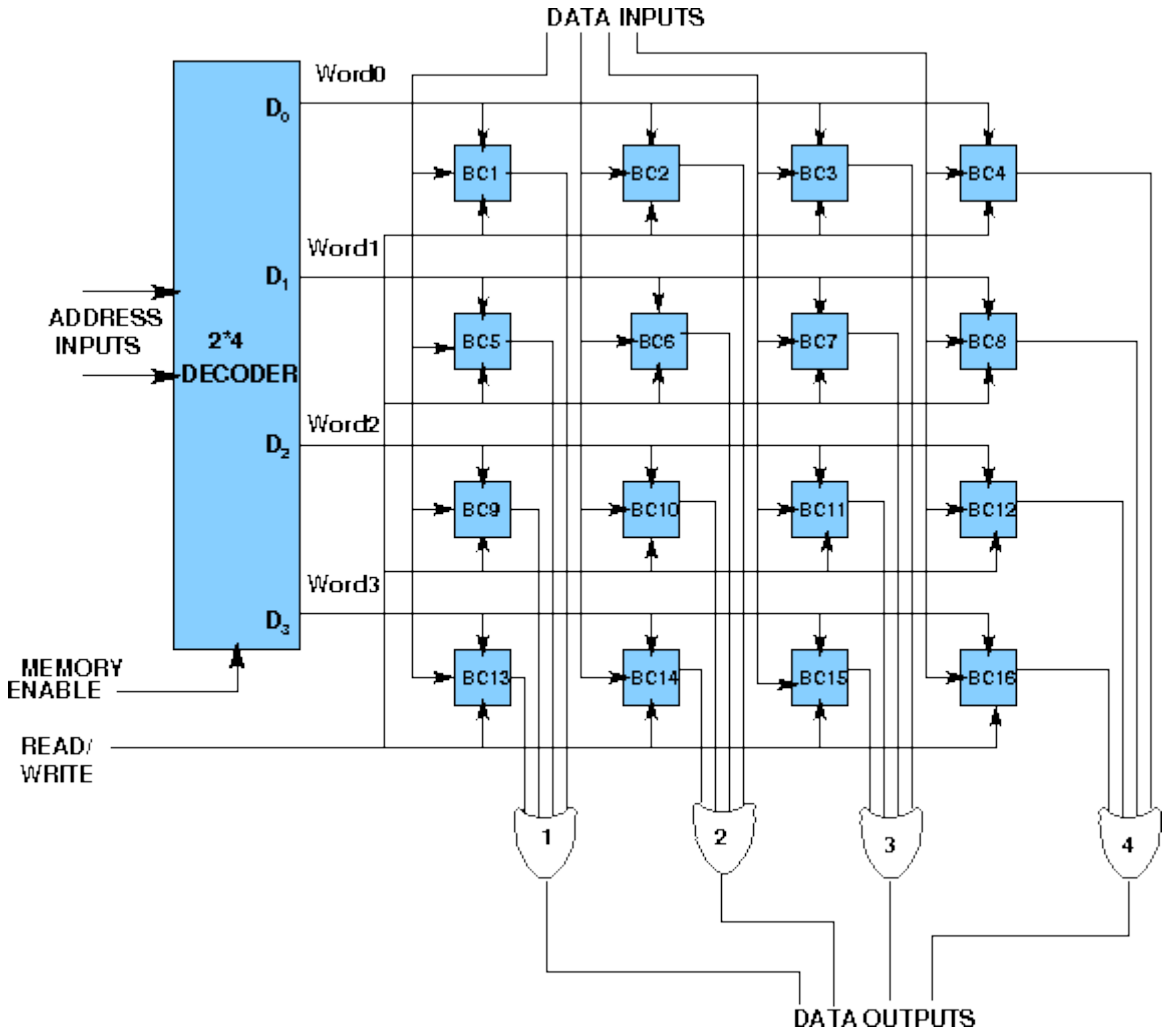
The binary cell has three inputs and one output. The select input enables the cell for reading or writing and the reda/write input determines the cell operation when it is selected. A 1 in the read/write input provides the read operation by forming a path from the flip-flop to the output terminal. A 0 in the read/write input provides the write operation by forming a path from the input terminal to the flip-flop. the logic diagram is-



Design of a 4X4 RAM :

The logical construction of a small RAM 4X3 is shown below. It consists of 4 words of 3 bits each and has a total of 12 binary cells. Each block labeled BC represents the binary cell with its 3 inputs and 1 output. The block diagram of a binary cell-

A memory with 4 words needs two address lines. The two address inputs go through a 2*4 decoder to select one of the four words. The decoder is enabled with the memory enable input. When the memory enable is 0, all outputs of the decoder are 0 and none of the memory words are selected. With the memory enable at 1, one of the four words is selected, dictated by the value in the two address lines. Once a word has been selected, the read/write input determines the operation. the logic diagram is-



Design Issues :

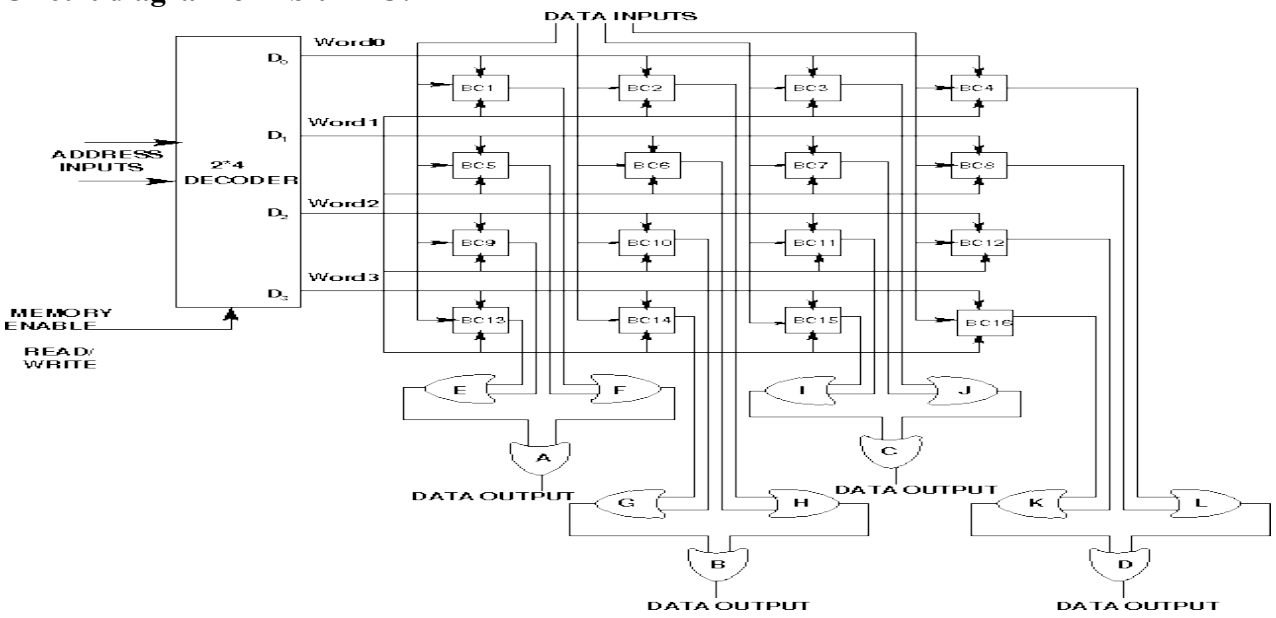
A basic RAM cell has been provided here as a component which can be used to design larger memory units. An IC memory consisting of 4 words each having 3 bits has been aslo provided.

Procedure

1. Procedure to perform the experiment:Design of 4X3 RAM memory:
2. Start the simulator as directed.This simulator supports 5-valued logic.To design the circuit we need 12 binary RAM cell, 9 OR gate, 7 bit switch (to give input,which will toggle its value with a double click), 3 bit display (to see the output), wires.
3. The pin configuration of a component is shown whenever the mouse is hovered on any canned component of the palette or press the 'show pinconfig' button. Pin numbering starts from 1 and from the bottom left corner (indicated with the circle) and increases anticlockwise.
4. For a binary RAM cell input is in pin-5, output is in pin-4 and select is pin-8, Read/Write is in pin-6, for read operation give 1 input to Read/Write pin. For write operation give 0 input to Read/Write pin.

5. For a 'decoder with enable', input A is in pin-6, B is in pin-5, output D0 is in pin-4, D1 is in pin-3, D2 is in pin-2, D3 is in pin-1 and Enable is in pin-8
6. Click on the 'decoder with enable' component (in the Other Components drawer in the pallet) and then click on the position of the editor window where you want to add the component (no drag and drop, simple click will serve the purpose), likewise add 12 binary RAM cell (from the Other Components drawer in the pallet), 9 OR gates (from Logic Gates drawer in the pallete), 7 bit switches (which will toggle its value with a double click), 3 bit displays (from Display and Input drawer of the pallet,if it is not seen scroll down in the drawer)
7. To connect any two components select the Connection menu of Palette, and then click on the Source terminal and click on the target terminal. According to the circuit diagram connect all the components, connect 2 bit switches to the inputs of the 'decoder with enable' (which will act as address input), 1 bit switch to the enable pin of the 'decoder with enable' (which will act as memory enable input), connect a bit switch to the Read/Write(R/W') line, 3 bit switches to the data inputs line, 3 bit displays to the data output line and OR gates according to the diagram shown in the circuit diagram. after athe connection is over click the selection tool in the pallete.
8. To see the circuit working, Do some read or write operation by properly setting the R/W', memory enable then give input and check the output. suppose you give, R/W'=1, memory enable=1, address input=01, data input=101, then it will be a read operation and you will not see 101 as output, it will store 101 in the word-1. now again set, R/W'=0, memory enable=1, address input=01, then it will be a write operation and you will see 101 as the content of word-1 on the output display.

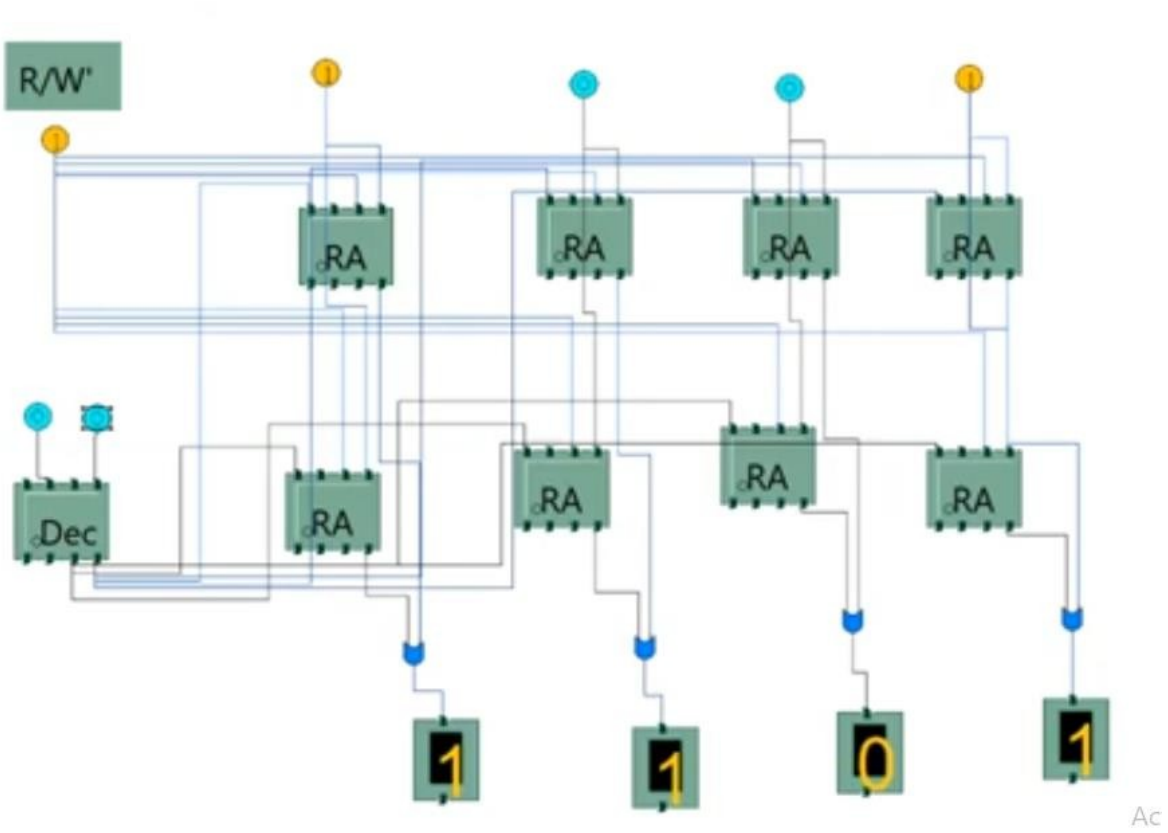
Circuit diagram of 4 bit ALU:



Components required :
For Designing a RAM Cell
To build a RAM Cell, we need :
AND Gate(2 input)-6
NOT Gate-2
RS Flip Flop-1

For Designing a 4X3 RAM
To build a 4X3 RAM, we need :
OR Gate(2 input)-11
RAM Cell-12
2X4 Decoder with Enable-1

Screenshots of Memory design:



Conclusion:

In this experiment, we designed a 4-bit arithmetic logic unit (ALU) capable of performing AND, OR, XOR, and addition operations. Through the implementation, we gained insights into the ALU's behavior and functionality, reinforcing our understanding of digital logic design. This hands-on experience demonstrated the critical role of ALUs in computational tasks and their integration within broader computer architectures.