



AY: 2024-25

Class:	SE	Semester:	<u>TIT</u>
Course Code:	CSC304	Course Name:	DLCA

Name of Student:	Archita Deepak Gupta
Roll No. :	19
Assignment No.:	03
Title of Assignment:	Analyze the truth table of digital component
Date of Submission:	06/09/24
Date of Correction:	06/09/24

## Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Completeness	5	4
Demonstrated Knowledge	3	3
Legibility	2	2
Total	10	9

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Completeness	5	3-4	1-2
Demonstrated Knowledge	3	2	1
Legibility	2	1	0

Checked by

Name of Faculty :

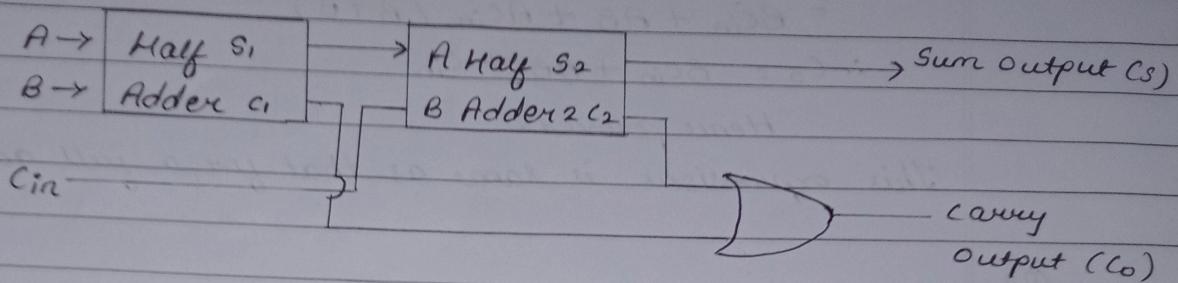
Signature

: Bharat

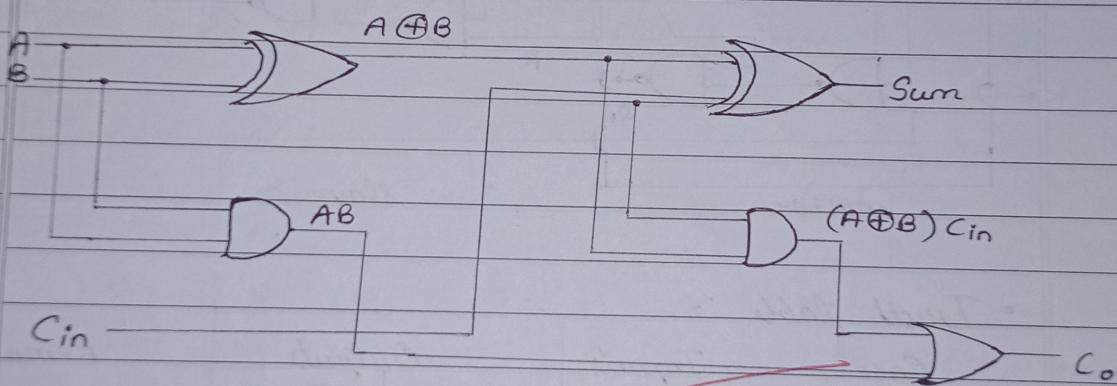
Date

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- Q1. A full adder circuit can be constructed using two half adders.



- A full adder can be implemented using two half adders and an OR gate as shown.
- Now, let us prove that this circuit acts as a full adder.



$$\text{Here } S = (A \oplus B) \oplus C_{in} = A \oplus B \oplus C_{in}$$

- This expression is same as that obtained for the full adder.
- Thus, the sum output has been successfully implemented by the circuit.

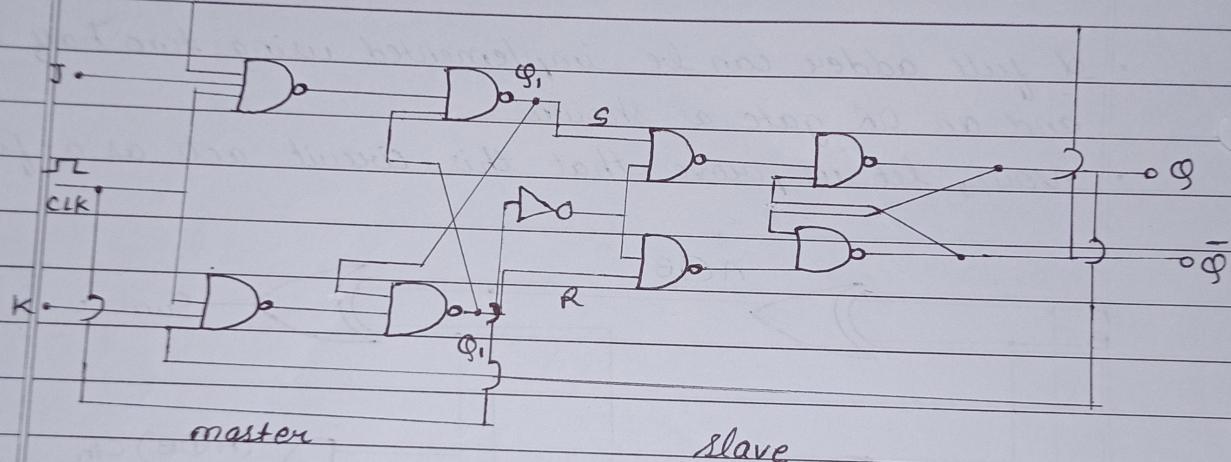
$$\begin{aligned}
\text{Now } C_o &= (A \oplus B) C_{in} + AB \\
&= (\bar{A}B + A\bar{B}) C_{in} + AB \\
&= \bar{A}BC_{in} + A\bar{B}C_{in} + AB \\
&= \bar{A}BC_{in} + A\bar{B}C_{in} + AB(1 + C_{in}) \\
&= \bar{A}BC_{in} + A\bar{B}C_{in} + AB + ABC_{in} \\
&= BC_{in}(\bar{A} + A) + A\bar{B}C_{in} + AB \\
&= BC_{in} + A\bar{B}C_{in} + AB
\end{aligned}$$

$$\begin{aligned}
 &= BC_{in} + A\bar{B}C_{in} + AB(1 + C_{in}) \\
 &= BC_{in} + A\bar{B}C_{in} + AB + ABC_{in} \\
 &= BC_{in} + AB + AC_{in}(\bar{B} + B) \\
 \therefore C_0 &= BC_{in} + AB + C_{in}
 \end{aligned}$$

Hence proved.

This expression is same as that for a full adder.

Q2.

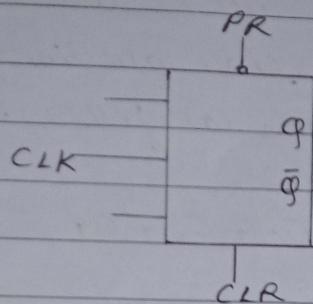


• Truth table :-

Case	Inputs			Outputs		Remark
	CLK	J	K	Q <sub>n+1</sub>	Q̄ <sub>n+1</sub>	
I	X	0	0	Q <sub>n</sub>	Q̄ <sub>n</sub>	No change
II	↑ (1)	0	0	Q <sub>n</sub>	Q̄ <sub>n</sub>	No change
III	↑ (1)	0	1	0	1	Reset
IV	↑ (1)	1	0	1	0	Set
V	↑ (1)	1	1	Q <sub>n</sub>	Q̄ <sub>n</sub>	Toggle.

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JK flip flop with preset and clear inputs



Inputs			Output	Operation performed
CLK	PR	CLR		
1	1	1	$Q_{n+1}$	Normal JK FF
X	0	1	1	FF is set
X	1	0	0	FF is reset

Q3. Truth table:

	Binary Inputs			Gray outputs		
	B <sub>2</sub>	B <sub>1</sub>	B <sub>0</sub>	G <sub>2</sub>	G <sub>1</sub>	G <sub>0</sub>
0	0	0	0	0	0	0
1	0	0	1	0	0	1
2	0	1	0	0	1	1
3	0	1	1	0	1	0
4	1	0	0	1	1	0
5	1	0	1	1	1	1
6	1	1	0	1	0	1
7	1	1	1	1	0	0

$$G_2 = O_4 + O_5 + O_6 + O_7$$

$$G_1 = O_2 + O_3 + O_4 + O_5$$

$$G_0 = O_1 + O_2 + O_5 + O_6$$

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- But the outputs of IC 74138 are active low
- Hence we will have to convert these questions in terms of inverted "0" outputs as follows:

$$G_2 = \bar{O}_4 + \bar{O}_5 + \bar{O}_6 + \bar{O}_7 = \overline{\bar{O}_4 + \bar{O}_5 + \bar{O}_6 + \bar{O}_7}$$

$$\text{But } \bar{A} + \bar{B} = \bar{A} \cdot \bar{B}$$

$$\therefore G_2 = \overline{\bar{O}_4 \cdot \bar{O}_5 \cdot \bar{O}_6 \cdot \bar{O}_7} \quad \text{--- (1)}$$

$$\text{Similarly } G_1 = \overline{\bar{O}_2 \cdot \bar{O}_3 \cdot \bar{O}_4 \cdot \bar{O}_5} \quad \text{--- (2)}$$

$$\text{and } G_0 = \overline{\bar{O}_1 \cdot \bar{O}_2 \cdot \bar{O}_5 \cdot \bar{O}_6} \quad \text{--- (3)}$$

