Vidyavardhini's College of Engineering and Technology

Department of Artificial Intelligence & Data Science

AY: 2024-25

Class:	SE	Semester:	III
Course Code:	CSC304	Course Name:	DLCA

Name of Student:	Archita Deepak Gupta
Roll No. :	19
Assignment No.:	05
Title of Assignment:	Apply concept of cache parameter.
Date of Submission:	
Date of Correction:	

Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Completeness	5	4
Demonstrated Knowledge	3	3
Legibility	2	1
Total	10	8

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Completeness	5	3-4	1-2
Demonstrated Knowledge Legibility	3	2	1
Legibility	2	1	0

Checked by

Name of Faculty :

Signature : Bharat

Date : 11/10/24

Ass-5

Q1. Consider a 4-way set associative mapped cache with block size 4KB. The size of the main memory is 16 GB and there are 10 bits in the tag.
Find: 1) Size of cache memory
2) Tag directory size.

Soln. Given:
Cache type: 4-way set associative
Block size: 4KB
main memory: 16 GB
Tag size: 10 bits.

main memory size = 16 GB = 2^{34} bytes.
Block size = 4KB = 2^{12} Bytes

Since the block size is 4KB, we need 12 bits to select a word.

word bits = 12 bits.

Tag	Set	Word
10 bits	12 bits	12 bits

From the cache layout
Tag = 10 bits
Set = 12 bits
word = 12 bits
Total address bits = 34 bits.

a) Cache size $= 2^{12} \times 4 \times 2^{12}$
$= 2^{26}$ bytes
$= 64$ mB

b) Tag directory size $= 2^{12} \times 4$
$= 2^{12}$ entries
$= 16K$ entries

Q2. The diagram shows an instruction stored in memory address 200 and 201. The address part of instruction has value 500. The computer has a processor register by name R1 having value 400 calculate & find the effective address and contents of Ac register for all the addressing modes discussed in the previous topic

(i) Register mode
(ii) Register indirect mode
(iii) Direct address mode
(iv) Indirect address mode
(v) Relative mode
(vi) Index mode
(vii) Intermediate mode.

	Address	memory	
PC = 200	200	load to Ac	mode
	201	Address = 500	
R1 = 400	202	Next instruction	
XR = 100	400	700	
	600	900	
Ac	800	300	

DATE:

Given:

PC (program counter) = 200

R1 = 400

XR = 100

AC (Accumulator)

Memory values

Address	loaded to AC	memory
200	Address = 500	
201	Next instr	
399		450
400		700
500		800
702		325
800		300

(i) Register mode:

- Effective Address: No memory look up, data is directly in the register.
- AC content: value in register
- Result : The value of R1 = 400

(ii) Register indirect mode:

- Effective Address: The address stored in the register
- AC content: value of R1
- Result : R1 = 400
  memory address = 700

(iii) Direct Address mode.

- Effective Address: The address is given directly by instruction.
- Ac contents: memory address = 500
- Result: PC = 200
  Memory Address = 500
  content of AC = 800

(iv) Indirect Address mode.

- Effective Address: The address stored at the given memory address
- Ac contents: value stored at final effective address
- Result: Content of 500 = 800
  content of memory address 800 = 300

(v) Relative mode

- Effective Address: The address is relative to program counter (PC)
- Ac contents: value stored at effective address
- Result: Effective address = 700
  memory content at 700 = 800

vi) Inder Mode

- Effective Address: The address is given by adding an inder to the base address
- Ac contents: value stored at indered address
- Result: Base address = 500 and XR = 100
  Effective address = 600
  Memory at 600 = 900

DATE:

(vii) Immediate mode

- Effective Address : No memory address, the operand is part of the instruction itself
- Ac contents : immediate value
- Result : The instruction contains the value 500
  So Ac = 500

Addressing mode	Effective Address	Ac contents
• Register mode	–	400
• Register indirect mode.	400	700
• Direct Address mode	500	800
• Indirect Address mode	800	300
• Relative mode	700	800
• Index mode	600	900
• Intermediate mode	–	500