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## Department of Artificial Intelligence & Data Science

AY: 2024-25			
Class:	SE	Semester:	
Course Code:	csc 304	Course Name:	DLCA

Name of Student:	Archita Deepak Cupta	
Roll No. :	19	
Assignment No.:	04	
Title of Assignment:	Compare hardwired & nivroprogrammed control writ of	for CPC
Date of Submission:		
Date of Correction:		

## Evaluation

Performance Indicator	Max. Marks	Marks Obtained
Completeness	5	4
Demonstrated Knowledge	3	3
Legibility	2	1
Total	10	8 .

Performance Indicator	Exceed Expectations (EE)	Meet Expectations (ME)	Below Expectations (BE)
Completeness	5	3-4	1-2
Demonstrated Knowledge Legibility	3	2	1
Legibility	2	1	0

Checked by

Name of Faculty

vame or racuny

Signature

Date

: Bhasat : 11/10/24

write a mic	roprogram for	the instruction ADDRI, Rz
T- state	Operation	microinstructions-
T.	PC -> MAR	Provent, MARin, Read, cleary, Set Cin, Add, Tin
T2	$m \rightarrow mBR$ $PC \leftarrow PC + I$	Zout, P.Cin, Wait for memory fetch cycle.
T <sub>3</sub>	mBR -> IR	mbRout, 1Rin
T4	$R_1 \longrightarrow \infty$	Riout, Xin, CLRC
Ts	R2 -> ALU	Report, ADD, Zin
TG	$Z \rightarrow R$ ,	Zout, Rijn
T <sub>7</sub>	Check for intr	Assumption enabled intr pending CLRX, SETC, SPout, SUB, Zin
T8	SP=SP=1	Zout, Spin, MARin
T9	el-mor	Prout, MORin, WRITE
Tio	MOR-7[SP]	wait for mem access
T <sub>1</sub>	PC+13 Raddy	Pcin 19 Raddr out

	ait and				
	92. compare and contrast Hardwired control unit.				
		and contrast Hardwin			
g:	2. compane	and control unit			
	microf	uogrammed control unit	to ways		
		to be designed us	ing lunc		
Sola	control	unit can be tral unit			
	1. H	control unit can be designed using two ways  1. Hardwired control unit  2. Microprogrammed control unit.			
	2. 1	licuprogrammed conte	,		
			тісновноджи		
	Aspect	Handwined controlunit	control unit		
	- Copie	1 P 3 P 2 P 2 P 2 P 2 P 2 P 2 P 2 P 2 P 2	It was a microprogr		
	00000	Built using fixed	It wes a		
	Design	combinational logic	-an stored in a		
		in a contract of	control memory.		
		coccuite			
1	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	- 11 answated by	(Generated by jetching		
2	control	Directly generated by	microinstructions		
	Signal	hardware corcuets.	from control memory.		
	generation	hardware circuits.	prom concers		
			,		
3.	Speed.	Faster, as signals are	Slower as each		
		directly produced by	instruction involves		
		the hardward.	memory fetch		
			cycles.		
		1 111 0 1 1 - 1	maya 11- 11-1		
4.	Heribility	less flexible: hard	more flerible:		
		to modify or update	instruction set can		
		instruction sets.	be easily modified.		
5.	complexity	complex design; difficult	simpler design; easier		
		to implement for			
		large instruction to	to handle larger		
		large instruction sets	instruction sets.		
		FOR EDUCATIONAL USE			
		TOR EDUCATIONAL USE			

		722.		
1		Aspect		DATE:
			Handwired (antrol	Control unit.
	6.	Cost	Higher initial design	Lower initial cost,
			hardware design.	but requires additional memory.
	7	Performani	High performance,	moderate performance,
•			Suitable for system needing speed.	better Suited for
				vorsatility.
	8.	modification	Difficult : requires	Easien; changes can be made by undating
			-ware conceit	be made by updating microinstructions.
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