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Design of Reversible Ternary Adder/Subtractor and Encoder/Priority Encoder Circuits

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Abstract— **Ternary quantum logic plays a very important role for building high speed and efficient futuristic computers. It has several advantages over classical computing and binary quantum circuits. In this paper, the realization of basic ternary circuits for adder/subtractor, encoder and priority encoder are proposed and designed. These circuits are very essential for the construction of various computational units of quantum computers and other complex computational systems. Design of reversible circuits can be improved by reducing the quantum circuit cost. This paper uses some elementary components and typical ternary gates (generalized ternary gate, M-S gate etc.) to perform arithmetic addition, subtraction and encoding operations. Finally, it evaluates the optimum cost for each circuit.**

Keywords- Quantum Circuit, Reversible logic, Qutrits, Ternary Adder, Subtractor, Quantum cost, Ternary Priority Encoder.

I. INTRODUCTION

Nowadays, power dissipation is one of the burning issues while measuring the performance of an integrated circuit. From Landauer"s statement, each bit of information lost kTln2 joules of energy during logic computations (where k is the Boltzmann"s constant and T is the operating temperature) [11]. It gives a major impact on various technologies like VLSI, Embedded systems. However, the use of reversible/quantum logic circuit helps to reduce the temperature and evacuating the radiated heat. In reversible gate the number of inputs is equal to the number of outputs and no fan-out is permitted. Many important designs based on ternary reversible logic are needed for building various circuits of quantum computers. But till now, ternary adder/subtractor and encoder circuit designs are not proposed. In this paper, the realization of quantum reversible ternary adder/subtractor, encoder and priority encoder circuits are proposed. Furthermore, we presented the result of our designs in terms of gate count, constant inputs, and total quantum cost. Some important reversible logic with ternary gates (necessary for the proposed work) are describe below.

A. The Qubit

The basic unit of information in quantum computing is called the qubit, which is short for quantum bit. Like a bit, a qubit can also be in one of two states. In the case of a qubit, we label these two states by |0>and |1>. In quantum theory an object enclosed using the notation | > can be called a state, a vector, or a ket. While a bit in an ordinary computer can be in the state 0 or in the state 1, a qubit can exist in the state |0> or the state |1>, but it can also exist in a superposition state i.e. a state that is a linear combination of the states |0> and |1>. If we label this state |ψ>, a superposition state is written as $|\psi\rangle = \alpha|0\rangle + \beta|1\rangle$ Here α, β are complex numbers of the form z =x +iy [1].

B. Ternary Quantum Logic

Ternary quantum logic is a qutrit based logic where more than two quantum basis states are introduced, for instance {|0>, |1>, |2>}. It is simply based on 3 qudit ternary logic circuitry. A ternary logic circuit can be made by the help of several ternary (qutrit) logic gates, like basic permutative gates[2], ternary Feynman gate[2], Muthukrishnan-Stroud (M-S) gate[2], ternary Toffoli gate[2] etc. Ternary Quantum Logic is the simplest introduction of multi-valued logic which is also referred to as 3VL .To define ternary logic, let T = {0, 1, 2}. A ternary reversible logic circuit with n inputs and n outputs is also called an n-qudit ternary reversible gate can operate on ternary values. In Ternary quantum logic, the Galois-field algebraic structure will be the fundamental for constructing a unified approach to multiple-valued quantum logic.

B.1 Ternary Galois Field (GF3) Operations with M-S G

It consists of the set of elements T= {0, 1, 2} and two basic binary operations – *addition* (denoted by +) and *multiplication* (denoted by · or absence of any operator).

Tables 1 and 2: Ternary Galois Field (GF3) operations

+	0	1	2
0	0	1	2
1	1	2	0
2	2	0	1

·	0	1	2
0	0	0	0
1	0	1	2
2	0	2	1

From this concept of GF3 logic, one famous gate is introduced (Muthukrishnan-Stroud or M-S gate) [2] as follows,

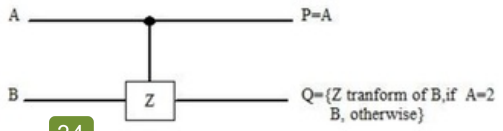

Fig. 1 Graphical representation of Muthukrishnan-Stroud (M-S) Gate

The quantum cost of a reversible gate is calculated by evaluating the number of primitive gates used to model that reversible gate [12]. The cost of each M-S Gate is 1[2].

B.2 Permutative Gates

Any transformation of the qudit state represented by a 3×3 unitary matrix specifies a valid 1-qudit ternary quantum gate. Transforms $Z(+1)$ and $Z(+2)$ shift the qudit states by 1 and 2, respectively. Transform $Z(12)$ permutes the qudit states 1 and 2 , $Z(01)$ permutes the qudit states 0 and 1 , and $Z(02)$ permutes the qudit states 0 and 2 without affecting the other qudit state. The input-output relationships of these 1-qudit gates are shown in truth table form. The ternary reversible 1-qudit gates are elementary gates and can be theoretically realized using quantum technology. 1-qudit ternary unitary permutative transforms [2] are shown below.

$$Z(+1) = \begin{pmatrix} 0 & 0 & 1 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{pmatrix} \qquad Z(+2) = \begin{pmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 1 & 0 & 0 \end{pmatrix}$$

$$Z(12) = \begin{pmatrix} 1 & 0 & 0 \\ 0 & 0 & 1 \\ 0 & 1 & 0 \end{pmatrix} \qquad Z(01) = \begin{pmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & 0 & 1 \end{pmatrix}$$

$$Z(02) = \begin{pmatrix} 0 & 0 & 1 \\ 0 & 1 & 0 \\ 1 & 0 & 0 \end{pmatrix}$$

Table 3: Truth table of 1-qudit ternary reversible gates

Input	Output				
	+1	+2	12	01	02
0	1	2	0	1	2
1	2	0	2	0	1
2	0	1	1	2	0

The cost of each Permutative Gate is 1.

A Ternary Toffoli Gate

The ternary 3-qutrit Toffoli gate in the universal ternary quantum get set is shown [2].

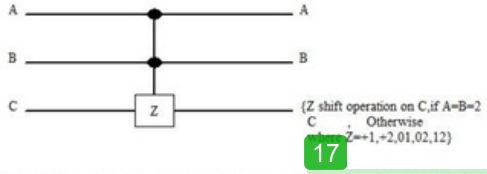

Fig. 2 Graphical representation of Ternary Toffoli- Gate

The cost of each Toffoli Gate is 5[2].

Ternary Shift operations.

Six 1×1 ternary Shift gates are proposed in [10]. Operations and symbols of these gates are shown in Fig. 1, where the addition and multiplication are over Galois Field 3 (GF3).

Gate Name	Gate Symbol and Operation(Addition and Multiplication are over GF3)
Buffer	x — x
Single-Shift	x — x'=x+1
Dual-Shift	x — x"=x+2
Self-Shift	x — x'''=2x
Self-Single-Shift	x — x#=2x+1
Self-Dual-Shift	x — x^=2x+2

Fig. 3 Ternary Shift operations

Generalized Ternary Gate

The Generalized Ternary gate (GTG) is described in [9] as shown in Fig. 4. Here, input A is the controlling input and input B is the controlled input. The output P is equal to the input A. The controlling input A controls a conceptual ternary multiplexer (a conditional gate) that can be realized using quantum technology such as ion traps. If A = 0, then the output Q is the x shift of the input B. Similarly, if A = 1, then the output Q is the y shift of the input B and if A = 2, then the output Q is the z shift of the input B. Here shift means all ternary shift operations including the buffer which is nothing but a simple quantum wire. Depending on the six possible Shift gates for each of the three positions of x, y, and z, there are 6^3= 216 possible GTGs. As the Conditional gate and the Shift gates are realizable in quantum technology, the GTGs are truly realizable ternary quantum gates. The cost of each GTG is 5[11].

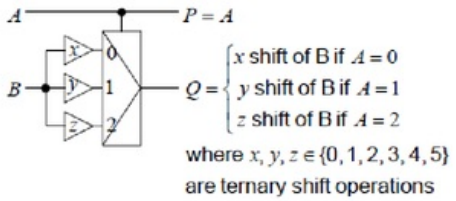

Fig. 4 Generalized Ternary Gate

In this paper, the designs of a ternary half adder circuit, a ternary full adder circuit, a ternary half subtractor circuit and a ternary full subtractor circuit have been shown with the help of generalized ternary gates. Also in this paper, the design of a reversible 9×2 ternary encoder circuit and a reversible 9×2 ternary priority encoder circuit have been shown with the help of ternary M-S Gates.

II. Literature Survey

In the paper named "Design of Reversible Quantum Ternary Multiplexer and Demultiplexer" by Mozammel H. A. Khan, the realization and design of ternary reversible 2×9 decoder, 9×1 multiplexer and 1×9 demultiplexer using the macro-level gates have been shown. In this paper, a very low-cost (=57) 2×9 ternary reversible decoder with active-2 outputs has been realized. Also the use of the decoder outputs in the 9×1 ternary reversible multiplexer and the 1×9 reversible demultiplexer circuits makes those circuits easier to realize though increasing their costs(=102). [2]

In the paper named "New Reversible/Quantum Ternary Comparator" by Reza Pa[illegible]n Zadeh and Majid Haghparast, the design of an n-qutrit ternary comparator has been demonstrated. In this paper, the use of 1-qutrit permutation gates, 3-qutrit Toffoli gates, M-S gates and lower-quantum-cost full adders makes the comparator circuit much easier to realize than the classical comparator circuit. [3]

In the paper "M[illegible]Valued Logic Gates for Quantum Computation" by Ashok Muthukrishnan and C. R. Stroud, Jr, he authors have developed a new approach for multi-level quantum system by decomposing any arbitrary unitary operations of d-levels(d>2) into logic gates of two systems by which the number of ions required for computation is reduced by a factor $\log_2 d$. In this paper, the authors have efficiently reduced the complexity of the multi valued simulation by a factor of $\log_2 d$. But the use of non-logarithmic scaling brings inefficiency in the construction part. A lot of elementary gates are required which makes the circuit a little complex. [4]

In the paper "Logic Synthesis of Ternary Quantum Circuits with Minimal Qutrits" by Xiaoyu Li, Guowu Yang, Desheng Zheng, a universal approach of synthesizing arbitrary ternary to quantum computation using truth table technology is developed by relating the classical logic circuit and quantum logic circuit. The authors provide an algorithm of Swap Gate, NOT gate and Toffoli gates and showed that the numbers of qutrits used are minimal. In this paper, the authors have developed a universal method for synthesizing ternary logic gates by combining the logic of classical and quantum logic circuits and have used a very good approach for the description of their ideology, a well-defined proof and mathematic relation for every equation. They provide a lot of tables which makes the understanding quite better. At every step they have related the quantum logic with the classical one and have made a smooth transformation from classical world to the quantum world. [5]

In the paper named "[illegible]alisation of Online Ternary Testable Circuit" by Naushin Nower, Ahsan Raja Chowdhury, an idea of testing the ternary network real time is demonstrated using the reversible gates. In this paper, , the authors have developed a new ideology of testing ternary network in real time by implementing a Ternary Testable Block(TB_3) using reversible gates and applying some GF_3 operations on each testable minterm such that if every block is correctly designed then final testable block will produce output 1.[6]

In the paper named "Quantum phases of qutrit" by Andrei B. Klimov , Luis L. S´anchez-Soto, Hubert de Guise and Gunnar Bjork , qutrits are represented geometrically in a space and all the formulas of complex number space diagram are developed for qutrits. In this paper, the authors have represented qutrits as an analogy to complex number vector representing in space diagram. They have developed a representation of qutrits in a Poincare Sphere later developed fundamental properties of unit vector using seven dimensional unit sphere. The [illegible]hors performed all the basic phase operations and Positive Operator Measures for the Qutrit [illegible]ses taking continuous values in 2π interval giving a description of qutrit phases in terms of a proper polar decomposition of its amplitudes .[7]

In the paper named "A Reve[illegible]e Ternary Adder for Quantum Computation" by Takahiko Satoh, Shota Nagayama, Rodney Van Meter, a reversible ternary carry-ripple adder is designed using 3n + 1 qutrits for adding two n-bits trits. In this paper, the authors have developed a method of adding two ternary qutrit developing the idea of addition of binary qubits. The authors have developed a circuit taking A and B as Input and giving A and A+B as output. Authors developed separate circuits for Sum and Carry. The depth and Total complexity of both the circuit is O(n).[8]

III. Proposed Work

Ternary Half Adder

The truth table of the ternary half adder function is shown in Table 4. The realization of the ternary half adder circuit is shown in Fig. 5. The circuit is realized based on cascade of Generalized Ternary Gates by using suitable combinations of ternary shift operations. The cost of this realization is 20 since 4 GTGs are used and the cost of each GTG is 5[11].

Table 4: Truth table of ternary half adder

AB	$C_{out}S$
00	00
01	01
02	02
10	01
11	02
12	10
20	02
21	10
22	11

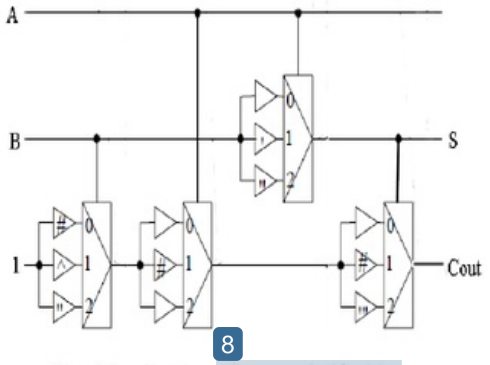

Fig. 5 Realization of ternary half adder

Ternary Full Adder

The truth table of the ternary full adder function is shown in Table 5. The realization of the ternary full adder circuit is shown in Fig. 6. The circuit is realized based on cascade of Generalized Ternary Gates by using suitable combinations of ternary shift operations. The cost of this realization is 50 since 10 GTGs are used and the cost of each GTG is 5[11].

Table 5: Truth table of ternary full adder

ABC_{in}	$C_{out}S$
000	00
001	01
002	02
010	01
011	02
012	10
020	02
021	10
022	11
100	01
101	02
102	10
110	02
111	10
112	11
120	10
121	11
122	12
200	02
201	10
202	11
210	10
211	11
212	12
220	11
221	12
222	20

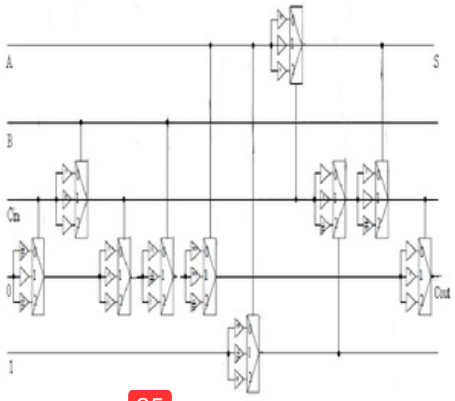

Fig. 6 Realization of ternary full adder

Ternary Half Subtractor

The truth table of the Ternary Half Subtractor function is shown in Table 6. The realization of the Ternary Half Subtractor is shown in Fig. 7. The circuit is realized based on cascade of Generalized Ternary Gates by using suitable combinations of ternary shift operations. The cost of this realization is 20 since 4 GTGs are used and the cost of each GTG is 5[11].

Table 6: Truth Table of ternary half subtractor

A	B	Diff	Bout
0	0	0	0
0	1	1	1
0	2	2	2
1	0	1	0
1	1	0	0
1	2	1	1
2	0	2	0
2	1	1	0
2	2	0	0

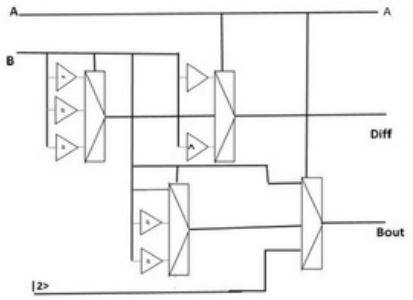

Fig 7: Realization of ternary half Subtractor

D. Ternary Full Subtractor

The truth table of the Ternary Full Subtractor is shown in Table 7. The realization of the Ternary Full Subtractor is shown in Fig. 8. The circuit is realized based on cascade of Generalized Ternary Gates by using suitable

combinations of ternary shift operations. The cost of this realization is 35 since 7 GTGs are used and the cost of each GTG is 5[11].

Table 7: Truth Table of ternary full subtractor

A	B	Bin	D	Bout
0	0	0	0	0
0	0	1	1	1
0	0	2	2	2
0	1	0	1	1
0	1	1	0	1
0	1	2	1	2
0	2	0	2	2
0	2	1	1	2
0	2	2	0	2
1	0	0	1	0
1	0	1	0	0
1	0	2	1	1
1	1	0	0	0
1	1	1	1	1
1	1	2	2	2
1	2	0	1	1
1	2	1	0	1
1	2	2	1	1
2	0	0	2	0
2	0	1	1	0
2	0	2	0	0
2	1	0	1	0
2	1	1	0	0
2	1	2	1	1
2	2	0	0	0
2	2	1	1	1
2	2	2	2	2

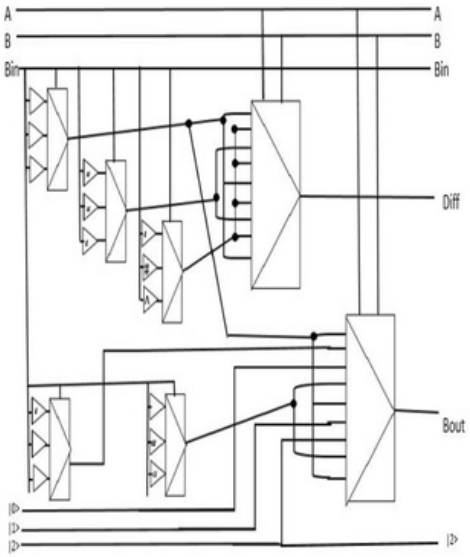

Fig 8: Realization of ternary full Subtractor

E. 9×2 Ternary Reversible Encoder

The truth table of the 9×2 Ternary Reversible Encoder function is shown in Table 8. The realization of the 9×2 Ternary Reversible Encoder circuit is shown in Fig. 9. The circuit is realized using ternary M-S Gates. For any 1 input being active(=2) and all other inputs being inactive(=0) at a particular time, the corresponding output combination is obtained. The cost of this realization is 27, since 27 M-S Gates have been used and the cost of each M-S Gate is unity[2].

Table 8: Truth table of 9×2 ternary reversible encoder

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_0
0	0	0	0	0	0	0	0	2	0	0
0	0	0	0	0	0	0	2	0	0	1
0	0	0	0	0	0	2	0	0	0	2
0	0	0	0	0	2	0	0	0	1	0
0	0	0	0	2	0	0	0	0	1	1
0	0	0	2	0	0	0	0	0	1	2
0	0	2	0	0	0	0	0	0	2	0
0	2	0	0	0	0	0	0	0	2	1
2	0	0	0	0	0	0	0	0	2	2

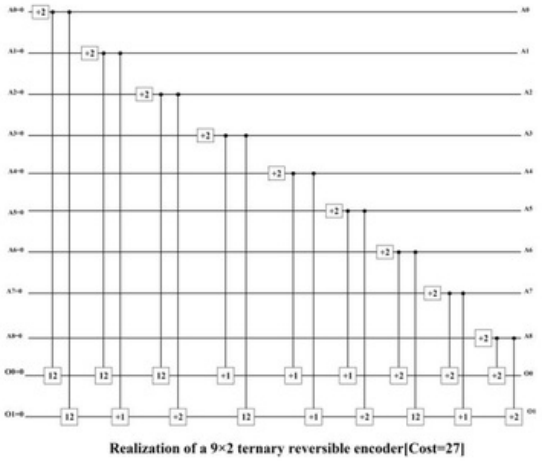

Fig. 9 Realization of 9×2 ternary reversible encoder

F. 9×2 Ternary Reversible Priority Encoder

The truth table of the 9×2 Ternary Reversible Priority Encoder function is shown in Table 9.The realization of the 9×2 Ternary Reversible Priority Encoder circuit is shown in Fig. 10. The circuit is realized by using ternary M-S gates. For any one input being active(=2) and all other inputs being either inactive (=0) or don't care terms at a particular time i.e. the values of the outputs are not affected by the values of the inputs other than the active input, the corresponding output combination is obtained. The cost of this realization is 44, since 44 M-S gates have been used and the cost of each M-S gate is unity[2].

Table 9: Truth table of 9×2 ternary reversible priority encoder

A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	O_1	O_0	V
0	0	0	0	0	0	0	0	0	×	×	0
0	0	0	0	0	0	0	0	2	0	0	2
0	0	0	0	0	0	0	2	×	0	1	2
0	0	0	0	0	0	2	×	×	0	2	2
0	0	0	0	0	2	×	×	×	1	0	2
0	0	0	0	2	×	×	×	×	1	1	2
0	0	0	2	×	×	×	×	×	1	2	2
0	0	2	×	×	×	×	×	×	2	0	2
0	2	×	×	×	×	×	×	×	2	1	2
2	×	×	×	×	×	×	×	×	2	2	2

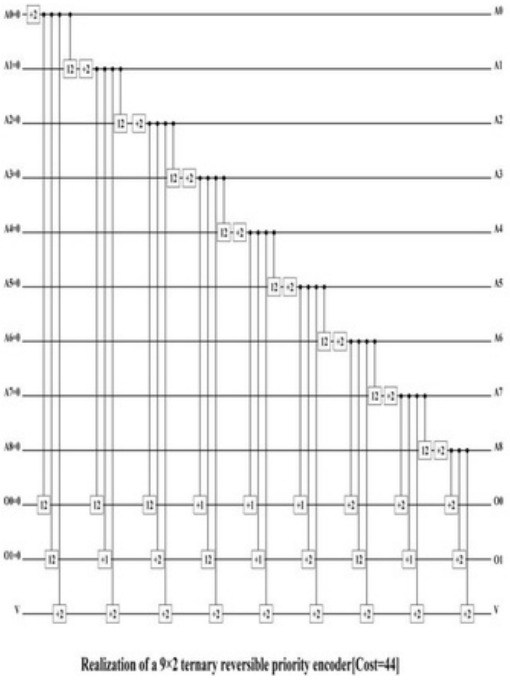

Fig.10 Realization of 9×2 ternary reversible priority encoder

IV. CONCLUSION AND FUTURE WORK

The proposed designs in this paper are based on the concept of ternary reversible logic with the help of quantum mechanics. The quantum reversible circuit has the advantages over the digital one in terms of power dissipation and speed up. In this paper, the basic ternary gates are used to design the circuits of adder/subtractor, encoder and priority encoder by taking care of some quantum parameters like quantum cost. Proposed circuits can be used for the design of complex computational units in future research.

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