Analog IC Design: Course Project

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LOW NOISE, LOW POWER NEURAL AMPLIFIER USING OTA TOPOLOGY

ACKNOWLEDGEMENT

I express my deep gratitude to **Dr. Abhishek Srivastava** for his valuable guidance and suggestions throughout the project work. I am grateful for his constant support and extend my sincere thanks for providing me with his valuable time and for always being approachable, which made the learning easier and helped me complete the project.

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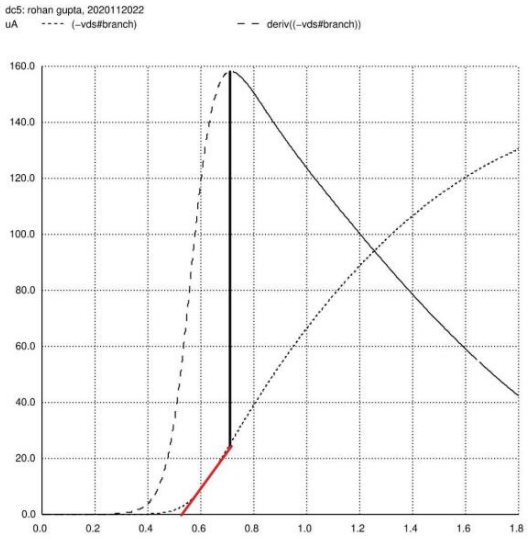
Design specifications Design the low noise low power neural amplifier (Fig. 1 in the paper) using the OTA topology (Fig. 4 in the paper) given in the following research paper: R. R. Harrison and C. Charles, A low-power low-noise CMOS amplifier for neural recording applications, IEEE J. Solid-State Circuits, vol. 38, no. 6, pp. 958965, Jun. 2003. Design for the following specifications:

- DC gain ≥ 60dB.
- -3 dB bandwidth ≥ 10 kHz.
- Input referred noise ≤ 2 μ Vrms.
- CMRR ≥ 100 dB.
- Noise efficiency factor (NEF) ≤ 4
- DC power consumption ≤ 30 μA
- Supply voltage ≤ 1.8 V

We start with acquiring the device parameters of MOsfets:



Vth = 0.54Volts

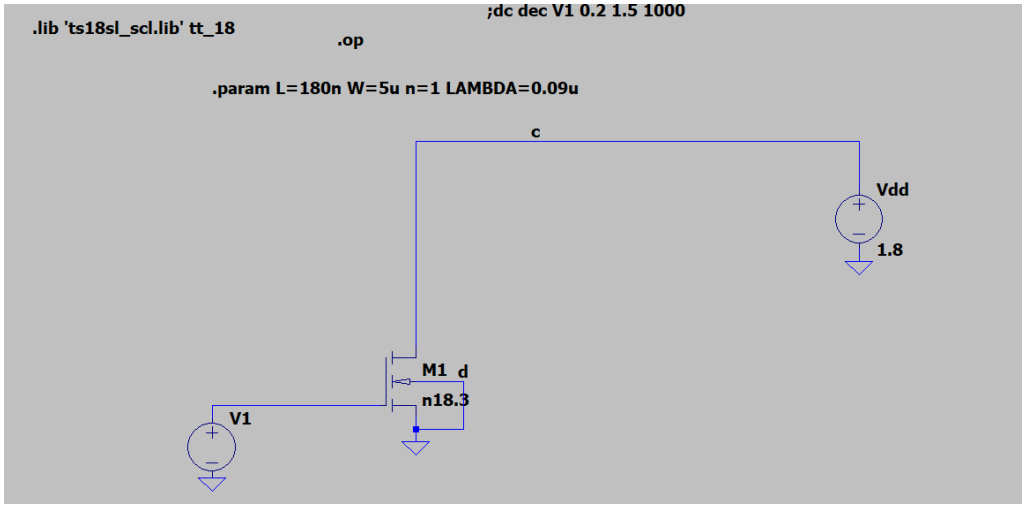


Fig: Circuit For NMOS device Parameter calculation

Device Parameter Calculation: NMOS (n18.4): VTHn=0.54V (in Linear region),

µnCox=280.6 uA/V

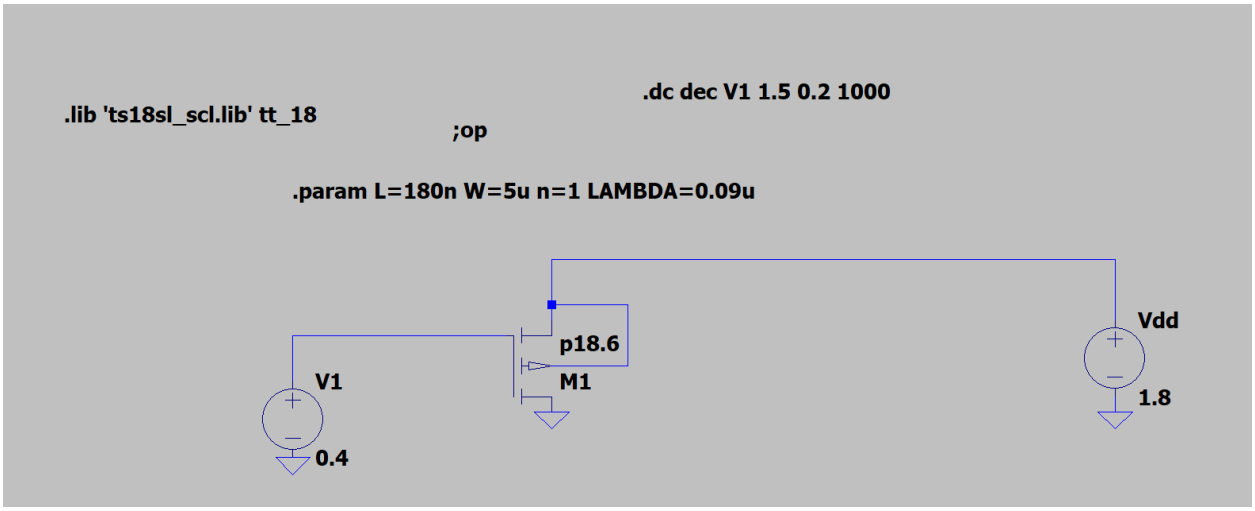


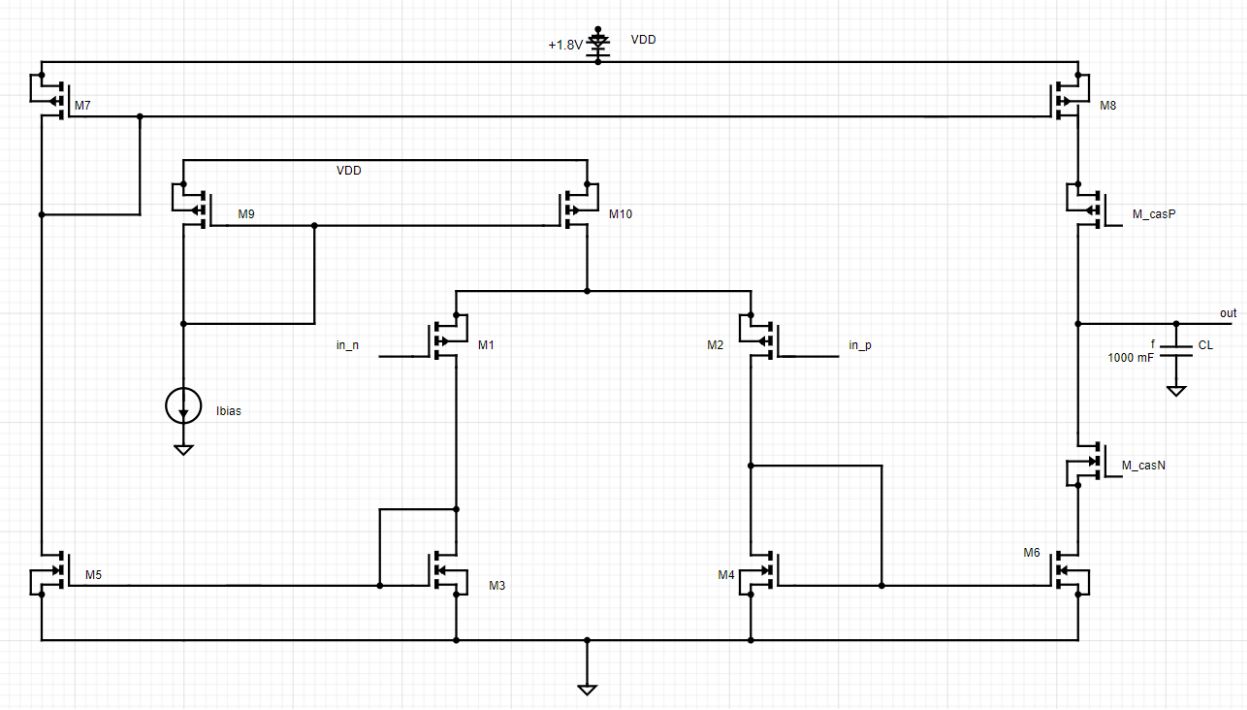
Fig: Circuit For PMOS device Parmaeter Calculation

Similarly we do for other nmos and pmos:

MOSFET	**uCox(uA/v²)**	**V_{th}**
n18.7	280.33	0.54
n18.9	58.55	0.378
p18.2	68.14	0.365
p18.7	56.35	0.471

p18.9	58.55	0.378

Que1.



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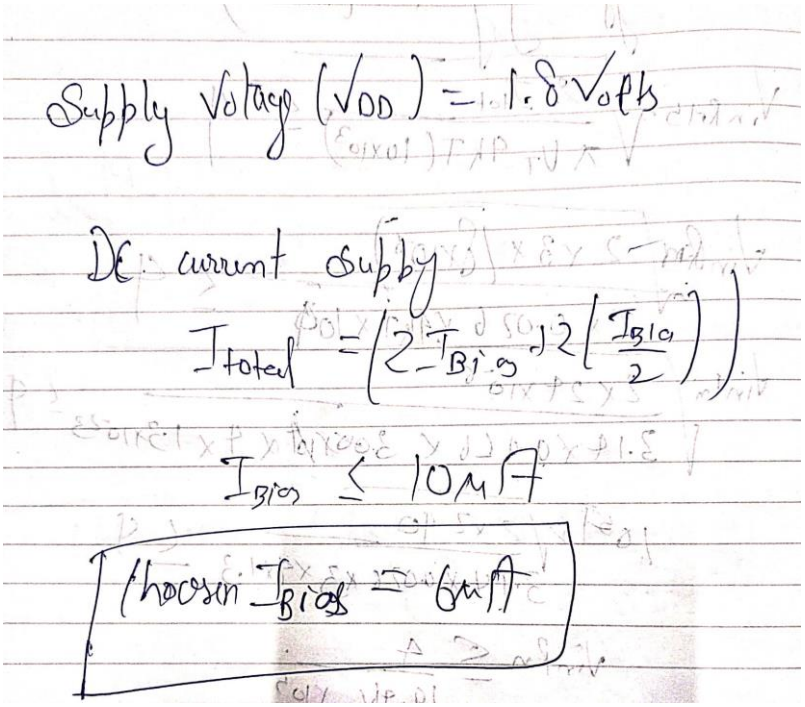

Supply Voltage (V_{DD}) = 1.8 Volts
DC current supply
$I_{total} = \left(2 - I_{Bias} \cdot 2\left(\frac{I_{Bias}}{2}\right)\right)$
$I_{Bias} \leq 10\mu A$
Choosing $I_{Bias} = 6\mu A$

M_1, M_2 – Subthreshold

$I_{1,2} < 0.1 \rightarrow I_{D1,2} = 4\,nA$

$\mu_p C_{ox} = 56.34\,\mu$

$\left(\frac{W}{L}\right)_{1,2} \geq \frac{40 \times 4}{(1.8)^2 \times 2 \times \mu_p C_{ox}} = 376.59$

$\left(\frac{W}{L}\right)_{1,2} > 376.59$

Choose sizing – $L = 0.18$, $W = 70$

$\left(\frac{W}{L}\right)_{1,2} = 9474.49$

M_7, M_8 — (strong inversion)

$I_{D7,8} > 10$

$I_{D7,8} = 9\,nA$ (for)

$\left(\frac{W}{L}\right) < \frac{4 \times 10^{-6} \times 0.7}{2 \times 58.39 \times 10^{-6} \times 0.026^2}$

$\left(\frac{W}{L}\right)_7 < 3.9$

Choose size $\left(\frac{W}{L}\right)_{7,8} = \frac{2}{5} = \frac{10\,\mu}{5\,\mu}$

$\left(\frac{W}{L}\right)_{3,6}$ (Saturation) (strong inversion)

$\frac{g_m}{I_D} < 2.5$

$g_m < 10 \times 10^{-6}$

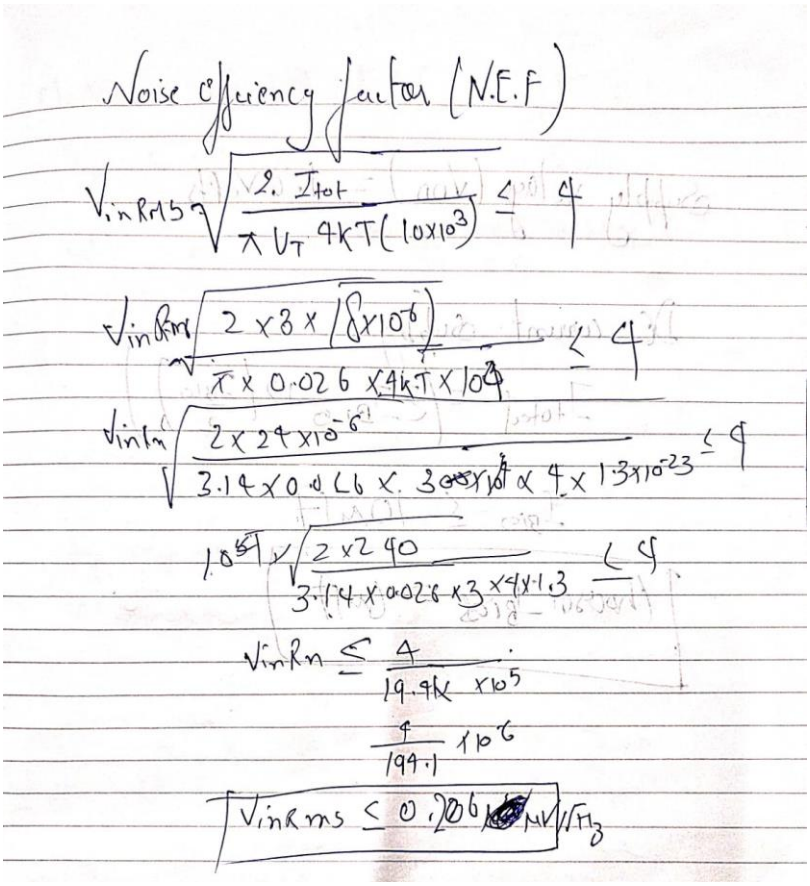
$\sqrt{2 I_D \mu_n C_{ox} \left(\frac{W}{L}\right)_{3,6}} < 10 \times 10^{-6}$

$= \sqrt{2 \times 4 \times 10^{-6} \times 280 \times 10^{-6} \left(\frac{W}{L}\right)_{3,6}} < 10 \times 10^{-6}$

$\left(\frac{W}{L}\right)_{3,6} < \frac{100}{\sqrt{2 \times 280}}$

$\left(\frac{W}{L}\right)_{3,6} < 4.22$

Choose sizing $\left(\frac{W}{3}\right)_{3,6} \leq \frac{10\,\mu}{5\,L} = 20$



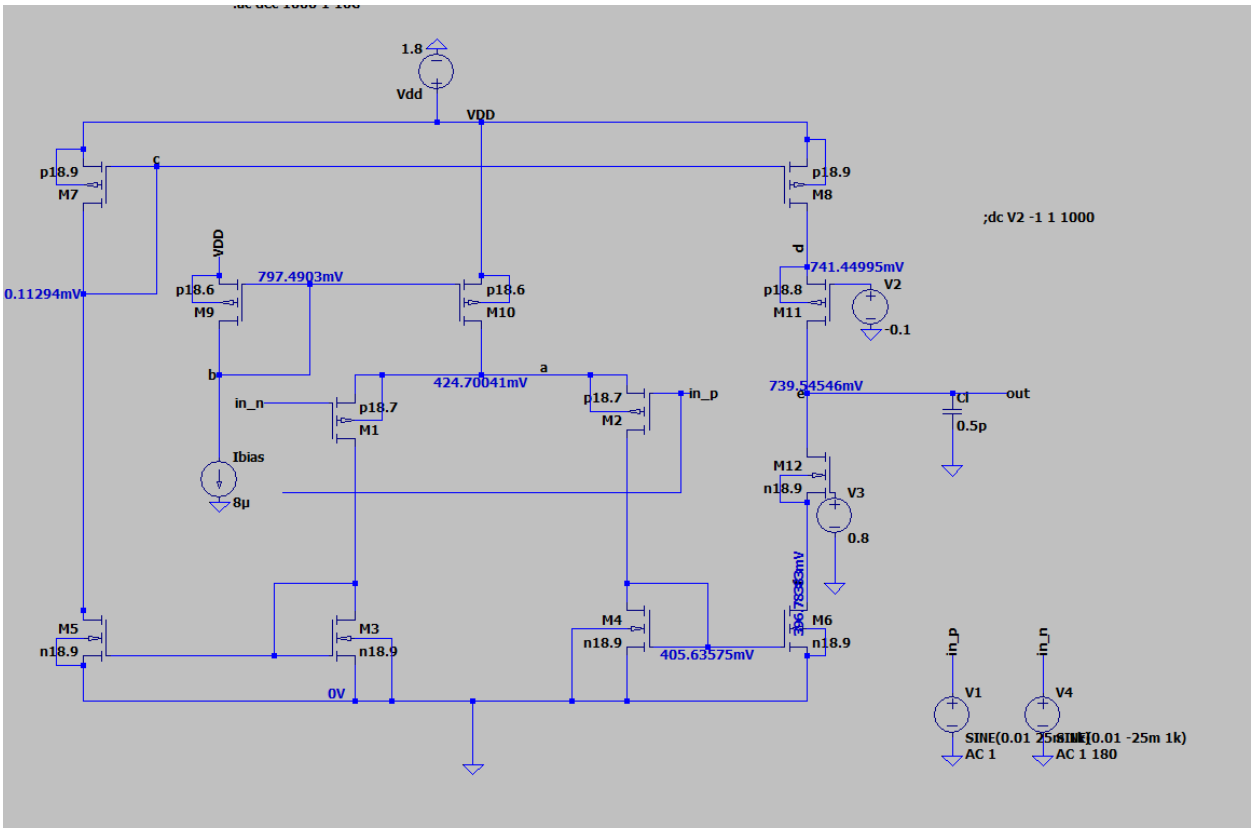
Design Parameters from hand calculations

Devices	Type	W/L
M1,M2	p18.7	80/0.18
M3,M4,M5,M6	n18.9	10/5
M7,M8	p18.9	5/10
M9,M10	p18.6	1.2/1.2
M_cascN	n18.9	12/3.2
M_cascP	p18.8	6.4/3.2

Specifications	Value
Gain	35.726628dB
Unity Gain Badwidth	5.2966344MHz
Phase Margin	55°
Gain Margin	19.871138dB

Que3.

a.)



Devices	Type	W/L	Hand Calculated
M1,M2	p18.7	80/0.18	80/0.18
M3,M4,M5,M6	n18.9	27/3	10/5
M7,M8	p18.9	2/9	5/10
M9,M10	p18.6	1.2/1.2	1.2/1.2
M_cascN	n18.9	40/5	12/3.2
M_cascP	p18.8	90/1	6.4/3.2
CL	0.5pF	1f	80/0.18

Specifications	Value
Gain	62.117163dB
Unity Gain Badwidth	5.4450265MHz
Slew Rate	5.1 MV/s
Phase Margin	42.80548°
Gain Margin	5.588399dB

c.)

OP Points	Values
V(n003)	0.405636V
V(vdd)	1.8Ve
V(a)	0.4247V
V(b)	0.79749V
V(n002)	0.405636V
V(in_n)	0.01V
V(in_p)	0.01V
V(d)	0.74145V
V(c)	0.510113V
V(f)	0.396784V
V(out)	0.739545V
V(n001)	-0.1V
V(p001)	0.8V
I(Cl)	3.69773e-025A
I(Ibias)	8e-006A
I(V4)	0A
I(V3)	0A
I(V2)	0A
I(V1)	0A
I(Vdd)	-2.41474e-005A

Name	m11	m7	m8	m2	m1
Model	p18.8	p18.9	p18.9	p18.7	p18.7
Id	-4.03E-06	-4.04E-06	-4.03E-06	-4.04E-06	-4.04E-06
Vgs	-8.41E-01	-1.29E+00	-1.29E+00	-4.15E-01	-4.15E-01
Vds	-1.90E-03	-1.29E+00	-1.06E+00	-1.91E-02	-1.91E-02
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.14E-01	-3.75E-01	-3.75E-01	-5.19E-01	-5.19E-01
Vdsat	-3.56E-01	-7.21E-01	-7.21E-01	-5.43E-02	-5.43E-02
Gm	8.88E-06	8.14E-06	8.11E-06	7.97E-05	7.97E-05
Gds	2.11E-03	2.81E-08	4.21E-08	1.65E-04	1.65E-04
Gmb	3.25E-06	2.77E-06	2.76E-06	2.48E-05	2.48E-05
Cbd	1.48E-14	4.33E-15	4.50E-15	1.47E-14	1.47E-14
Cbs	1.48E-14	5.90E-15	5.90E-15	1.48E-14	1.48E-14
Cgsov	2.34E-14	5.20E-16	5.20E-16	2.08E-14	2.08E-14
Cgdov	2.34E-14	5.20E-16	5.20E-16	2.08E-14	2.08E-14
Cgbov	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dQgdVgb	7.96E-13	1.18E-13	1.18E-13	9.73E-14	9.73E-14
dQgdVdb	-3.91E-13	-6.30E-16	-8.32E-16	-3.88E-14	-3.88E-14
dQgdVsb	-3.70E-13	-1.06E-13	-1.06E-13	-3.54E-14	-3.54E-14
dQddVgb	-3.95E-13	-4.97E-14	-4.99E-14	-3.89E-14	-3.89E-14
dQddVdb	3.51E-13	4.94E-15	5.27E-15	5.29E-14	5.29E-14
dQddVsb	1.76E-13	6.43E-14	6.43E-14	7.13E-15	7.13E-15
dQbdVgb	-4.84E-15	-1.85E-14	-1.84E-14	-1.94E-14	-1.94E-14
dQbdVdb	-2.74E-13	-4.40E-15	-4.68E-15	-3.14E-14	-3.14E-14
dQbdVsb	-2.04E-14	-2.92E-14	-2.92E-14	-1.44E-14	-1.44E-14

Name	m9	m10	m12	m6	m5
Model	p18.6	p18.6	n18.9	n18.9	n18.9
Id	-8.00E-06	-8.07E-06	4.03E-06	4.03E-06	4.04E-06
Vgs	-1.00E+00	-1.00E+00	4.03E-01	4.06E-01	4.06E-01
Vds	-1.00E+00	-1.38E+00	3.43E-01	3.97E-01	5.10E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.00E-01	-3.99E-01	3.78E-01	3.87E-01	3.87E-01
Vdsat	-4.79E-01	-4.79E-01	6.85E-02	6.62E-02	6.62E-02
Gm	2.41E-05	2.44E-05	8.31E-05	8.45E-05	8.46E-05
Gds	2.34E-07	1.54E-07	7.68E-08	8.42E-08	5.55E-08
Gmb	7.44E-06	7.52E-06	1.96E-05	1.97E-05	1.98E-05
Cbd	4.25E-15	4.00E-15	1.39E-14	1.37E-14	1.33E-14
Cbs	5.52E-15	5.52E-15	1.56E-14	1.56E-14	1.56E-14
Cgsov	3.12E-16	3.12E-16	8.80E-15	5.94E-15	5.94E-15
Cgdov	3.12E-16	3.12E-16	8.80E-15	5.94E-15	5.94E-15
Cgbov	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
dQgdVgb	1.05E-14	1.05E-14	1.02E-12	4.17E-13	4.17E-13
dQgdVdb	-3.19E-16	-3.14E-16	-1.12E-14	-6.48E-15	-6.18E-15
dQgdVsb	-9.23E-15	-9.23E-15	-8.03E-13	-3.26E-13	-3.26E-13
dQddVgb	-4.34E-15	-4.34E-15	-3.96E-13	-1.61E-13	-1.61E-13
dQddVdb	4.56E-15	4.31E-15	2.46E-14	2.01E-14	1.94E-14
dQddVsb	5.24E-15	5.24E-15	4.83E-13	1.93E-13	1.93E-13
dQbdVgb	-1.77E-15	-1.78E-15	-2.25E-13	-9.52E-14	-9.54E-14
dQbdVdb	-4.25E-15	-4.00E-15	-1.52E-14	-1.40E-14	-1.35E-14
dQbdVsb	-7.08E-15	-7.07E-15	-1.88E-13	-8.21E-14	-8.20E-14

d.)

Specifications	Value
Gain	62.117163dB
Unity Gain Badwidth	5.4450265MHz
Slew Rate	5.1V/us
Phase Margin	42.80548°

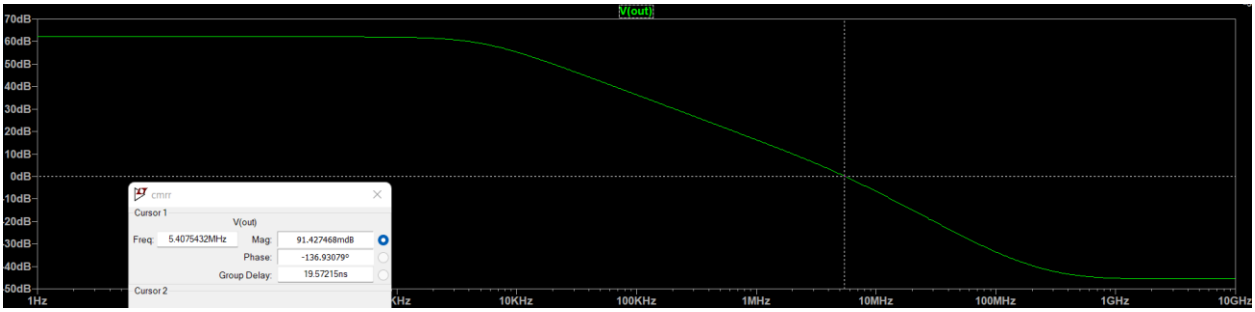


Fig. - Gain Plot

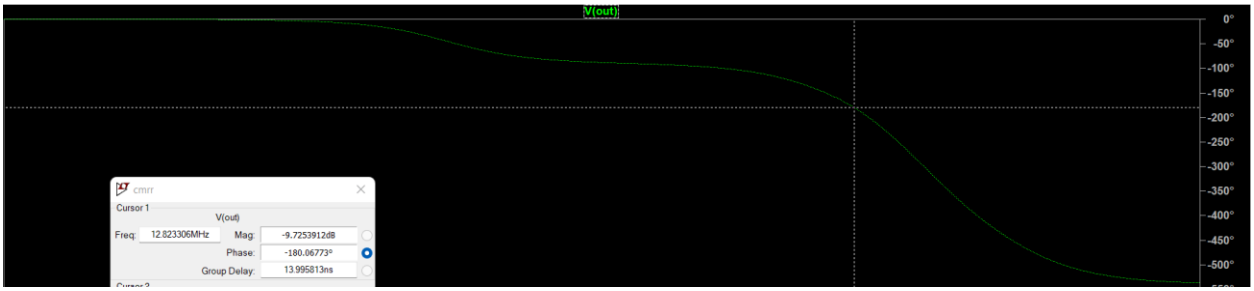


Fig.- Phase Plot

e.)

Maximum value of achieved output - 1.7048613V

90% of Max Value($V_{90\%}$) = 1.534 V - $t_{90\%}$ = 313.85ns

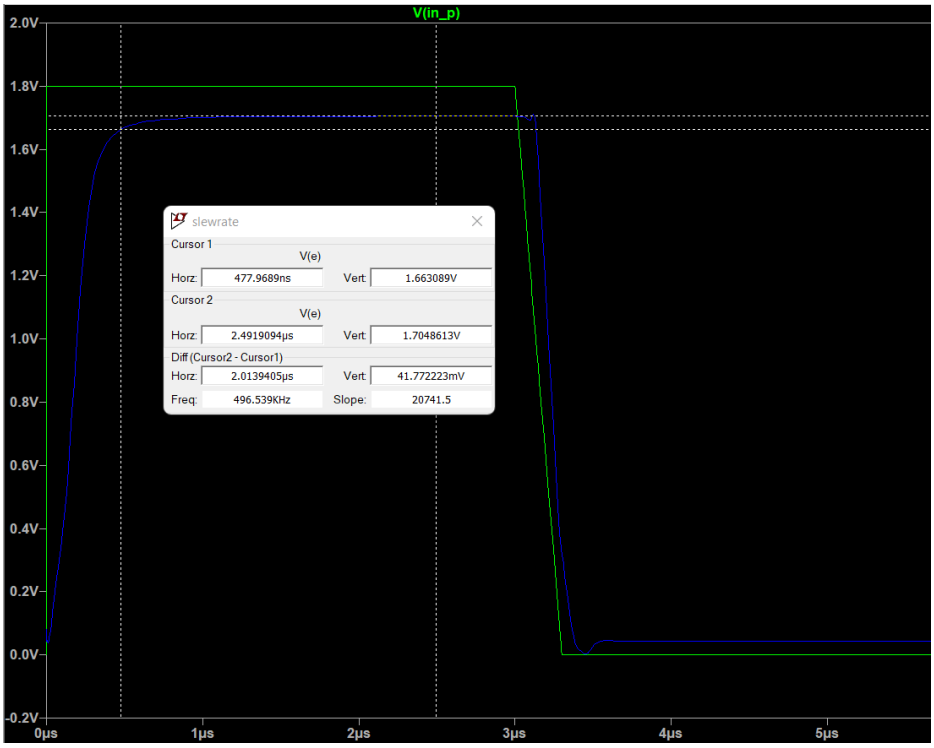
10% of Max Value($V_{10\%}$) = 0.170 V – $t_{10\%}$ = 48.70ns

Slew Rate = ($V_{90\%}$ - $V_{10\%}$)/($t_{90\%}$ - $t_{10\%}$) = 1.364/265.15ns = 5.1V/us = 5.1 MV/s

f.)

SETTLING TIME:
With the OTA in unity gain feedback mode, apply the same step input as above. Measure and report the settling time, ts for 2% accuracy.

Settling time for 98% of Max Value - 477.9689ns



g.)

SYSTEMATIC OFFSET:

With the OTA in unity gain feedback mode, measure and report the systematic offset value using dc analysis. Clearly show the output node voltage on the schematic.

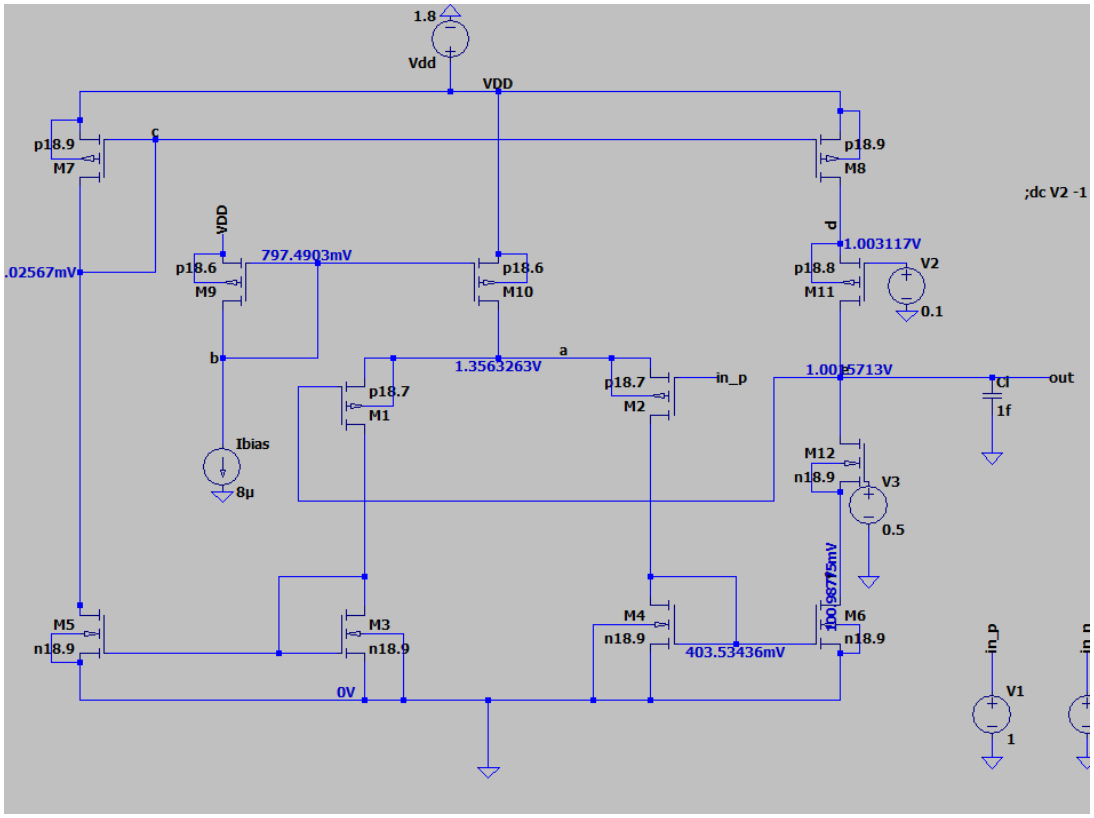
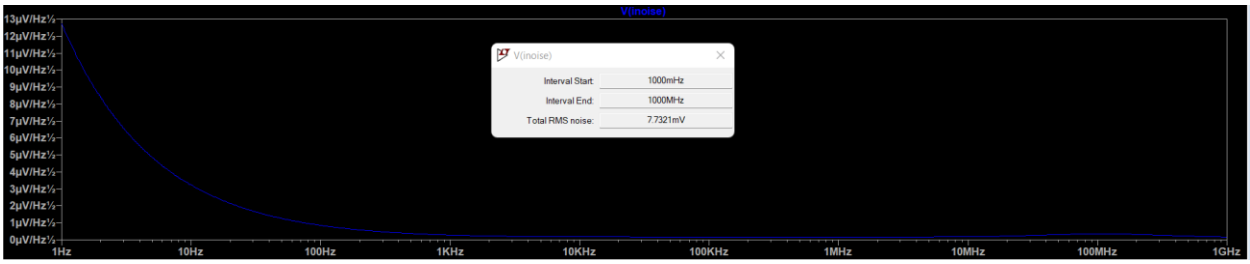


Fig: Systematic Offset

The systematioc offset value when an input of 1V is given comes out to be 1.0015713 V as shown which means that offset preset is **1.57 mV.**

h.)

NOISE:
Show the input referred noise PSD from 1Hz to 1GHz band. Clearly show the RMS thermal noise voltage in the plot (with cursor). Report the integrated noise voltage over the unity gain bandwidth.



Integrated noise voltage over the unity gain bandwidth - 21.058mV

Input Referred integrated noise voltage over the unity gain bandwidth **- 401.77µV**

i.)

CMRR:
Plot the open loop CM gain of the OTA with clear labels. Report the CMRR of the OTA.

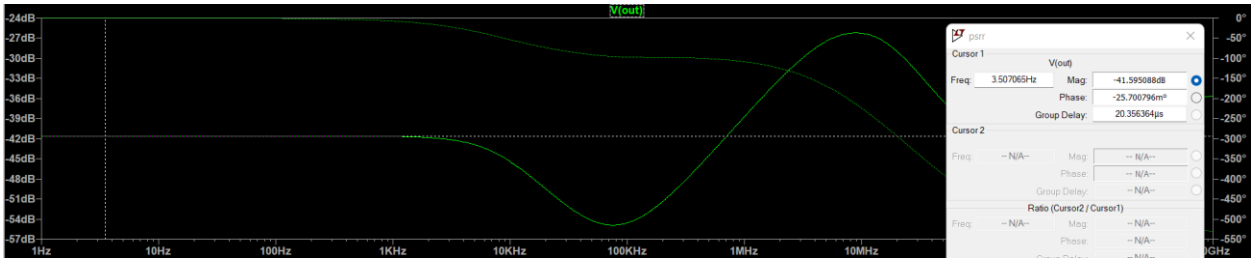


Fig: Open Loop CM Gain

CMRR= 20log(Adm/Acm) = Adm(dB)-Acm(dB) = 62.103965dB +41.595088dB = 103.699053

CMRR = 103.699053dB

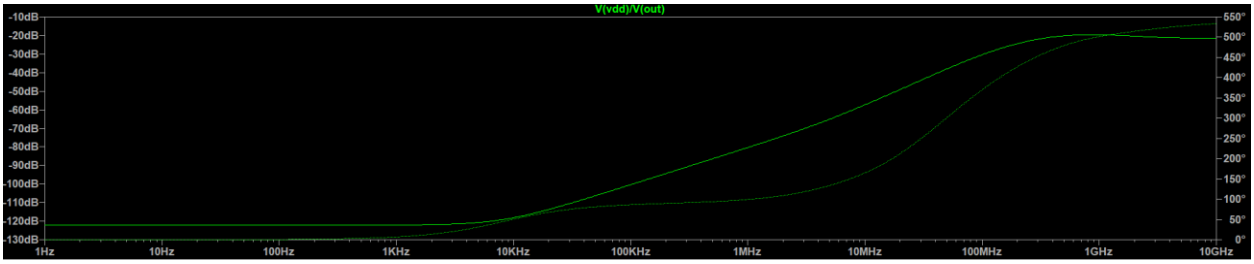
j.)

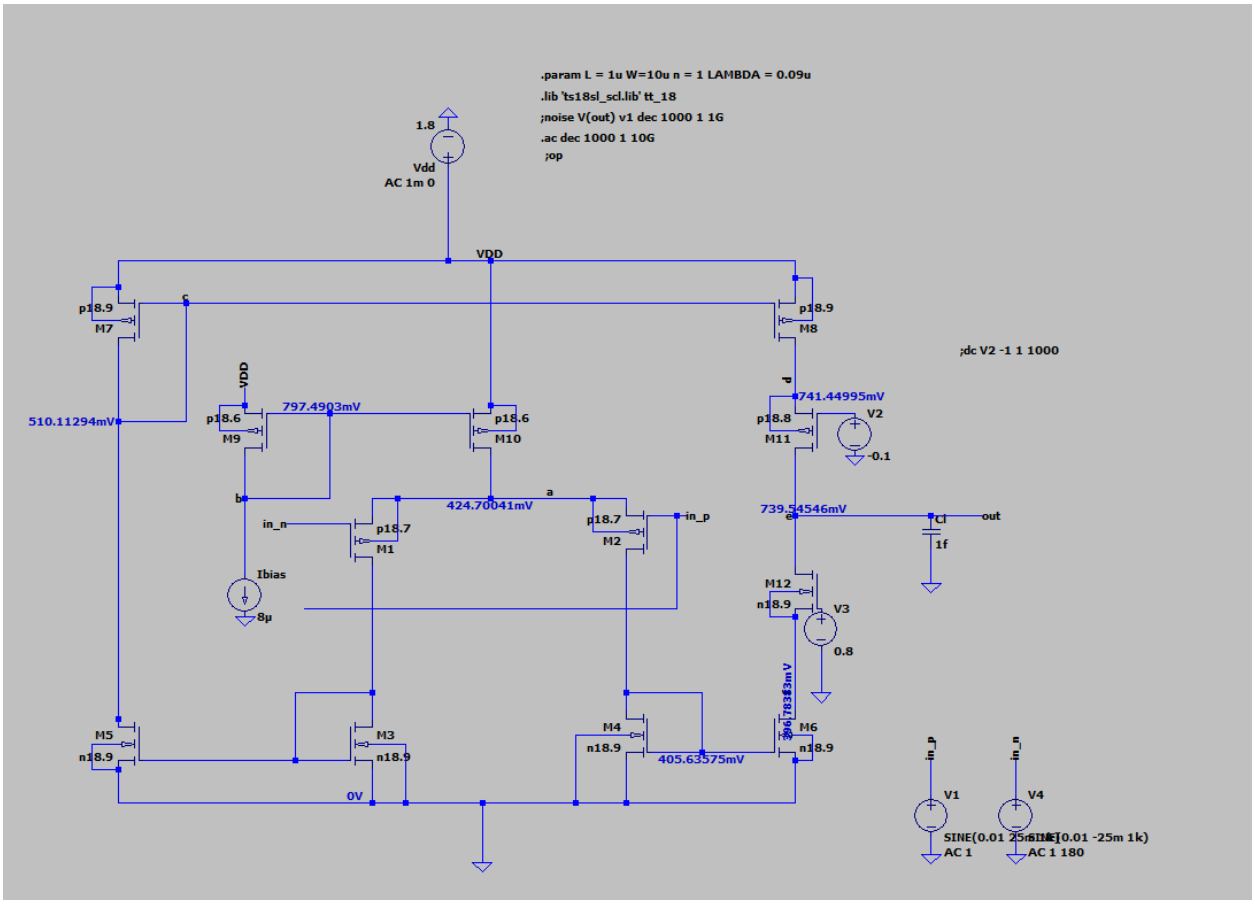
PSRR:

Perform the PSRR simulation by adding a small signal component only on the voltage supply of the OTA. Plot and report the PSRR value with clear labels (Open loop).

$$PSRR_+ = \frac{Differential\ Mode\ gain\ (in\ linear\ scale)}{Gain\ in\ PSRR\ configuration}$$

Reported PSRR = 20log[(61.2 dB)linear scale*(-122.44 dB)linear scale]= -**<u>60.19 dB</u>**

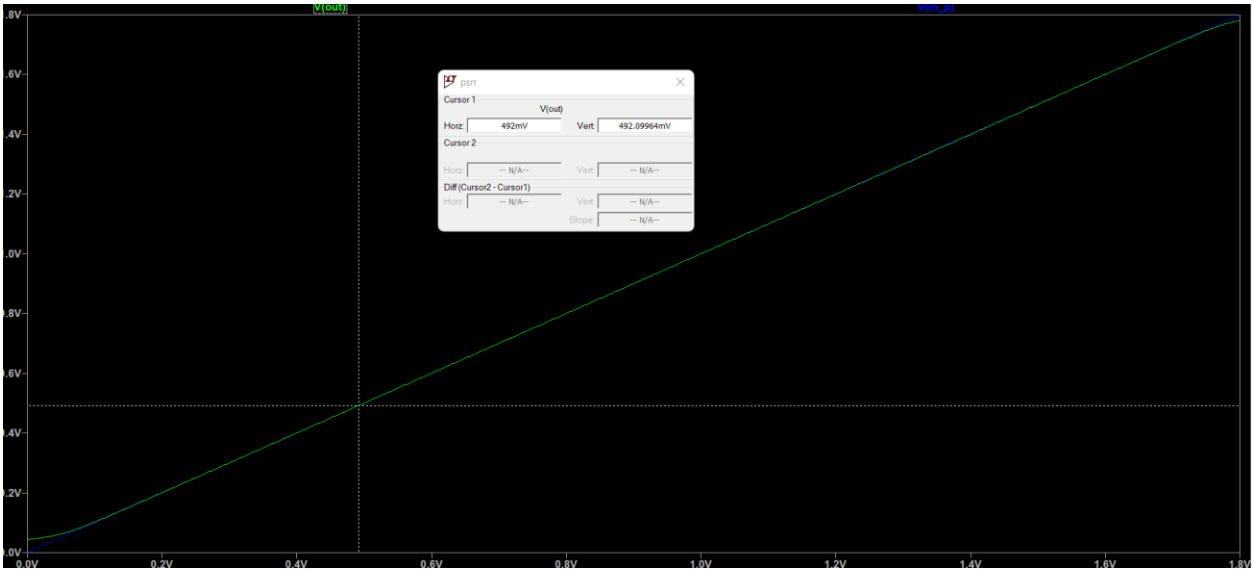


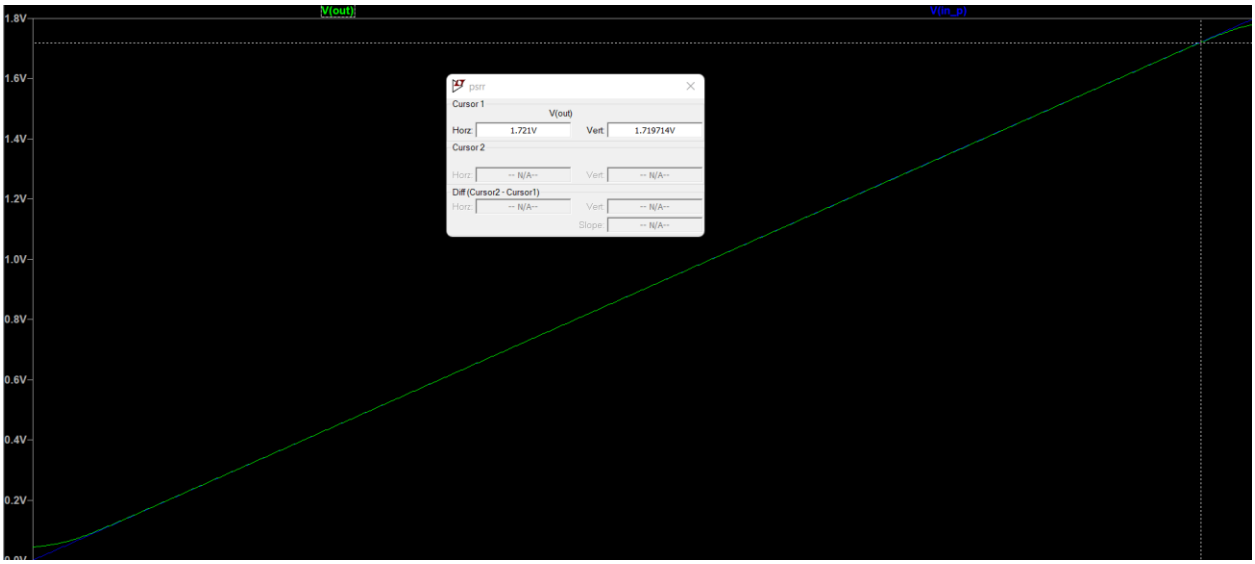


k.)

INPUT COMMON MODE RANGE:

Sweep the input common mode voltage in the unity gain configuration and report the maximum input common mode range of the OTA.

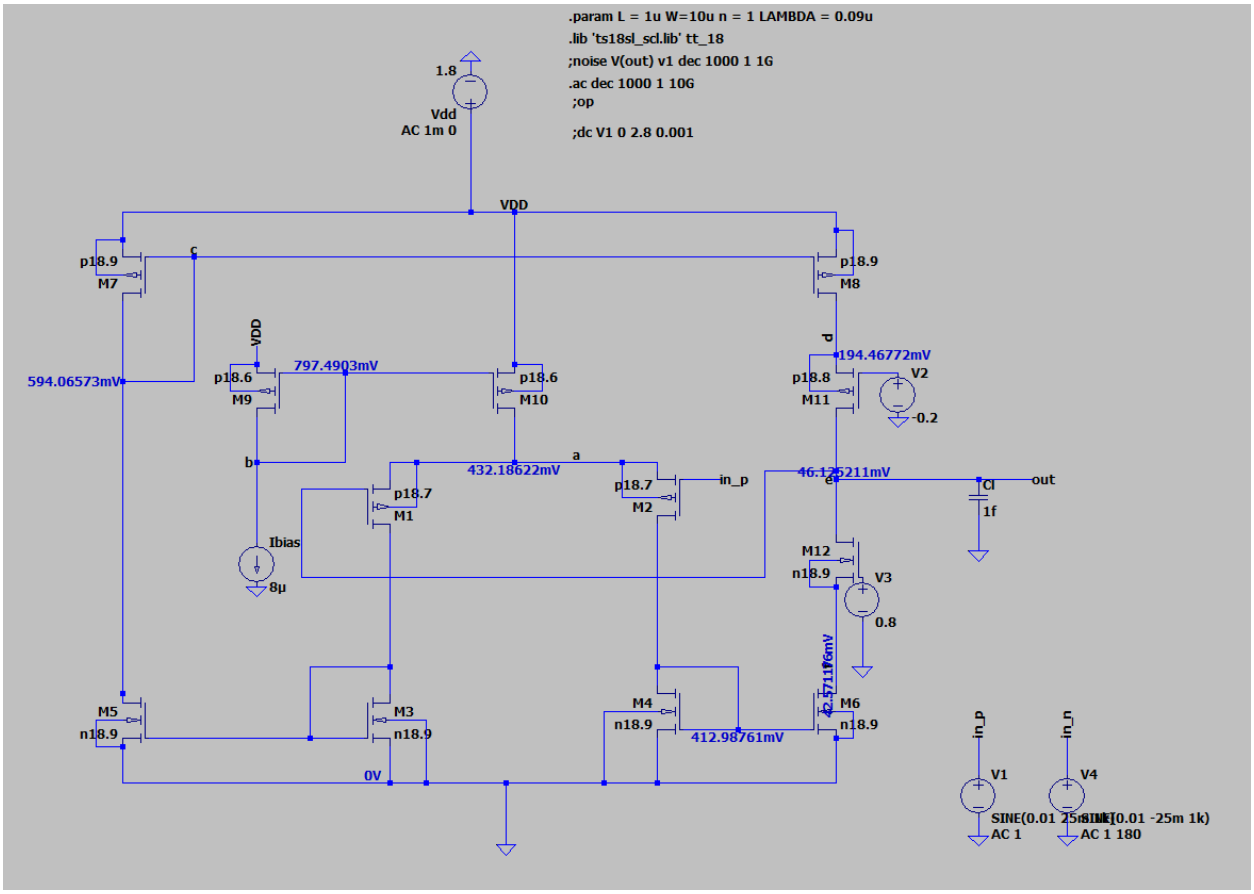


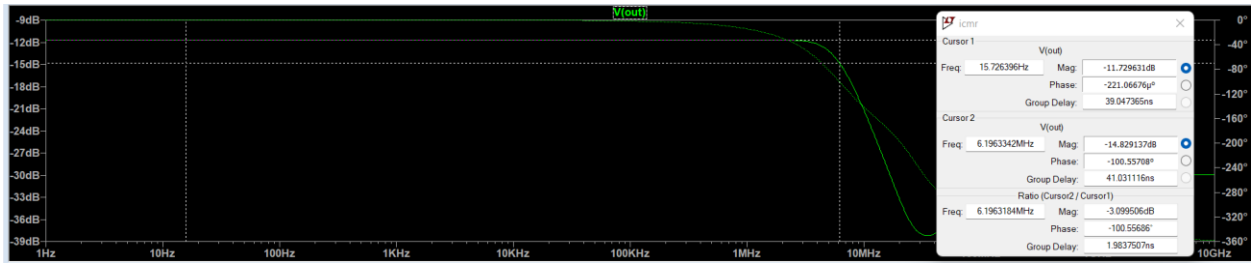


The ICMR of the OTA is shown. The range is from 492mV to 1.721 V which gives the range of **1.22 V.**

l.)

CLOSED LOOP GAIN: With the OTA in unity gain feedback mode, perform ac analysis and report the DC gain and the -3dB frequency.





The closed loop dc gain is around -12dB

-3dB bandwidth = 6.196 MHz

n.)

POWER CONSUMPTION:
Report the total current and power consumption of the OTA.

```
I(Vdd):          -2.41474e-005  device_current
```

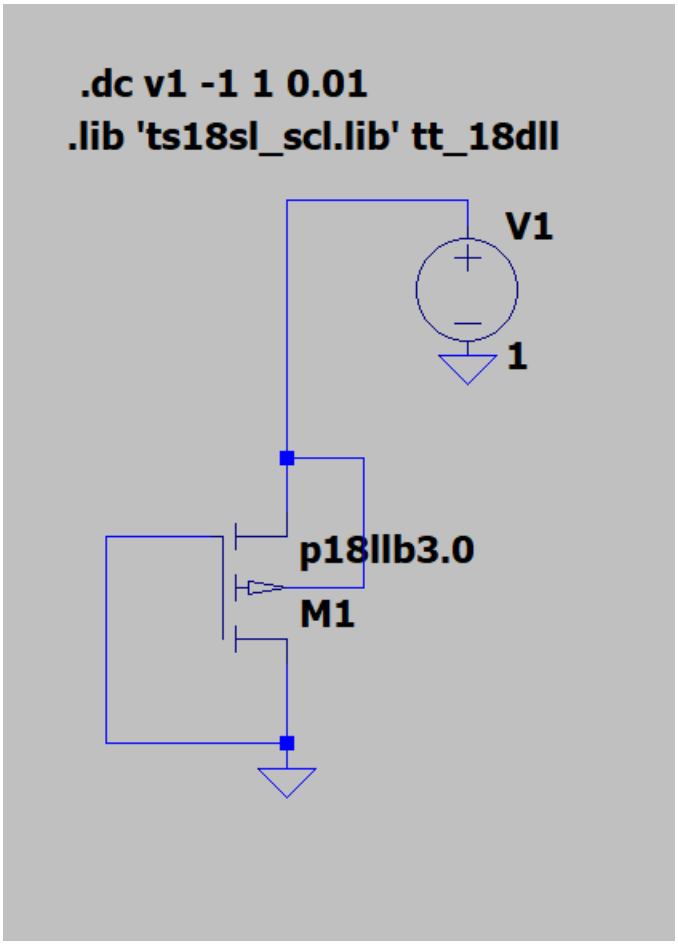
Current Consumption – **24.14uA**

Power Consumption – Vdd*Id = 1.8*24.14uA = **43.452uW**

Que4.

Pseudo resistor design

Design the pseudo PMOS resistor shown in the Fig. 1 in the paper. Simulate and plot its I-V characteristics and incremental resistance vs incremental voltage across it.



Below Fig shows the simulations performed using the pseudo resistor. Fig. (A) shows the variation of resistance w.r.t the voltage across the pseudo resistor. (B) shows the

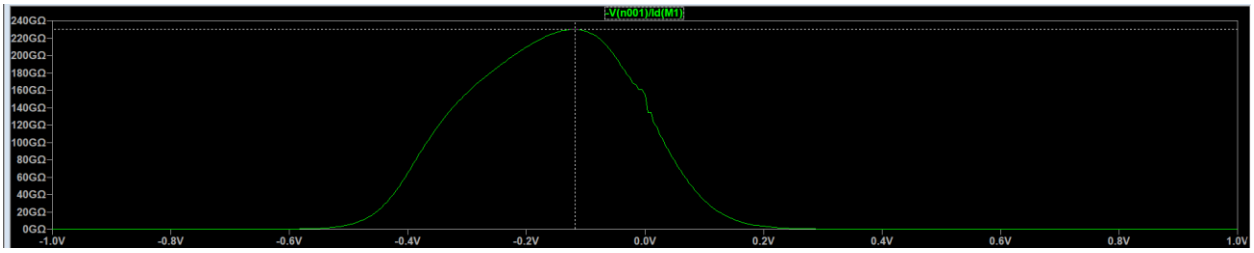
incremental resistance vs incremental voltage graph (dV/dID Ω). Fig. 4(C) shows the I-V characteristics of the pseudo resistor.

• The maximum resistance is around 229.99117GOhm

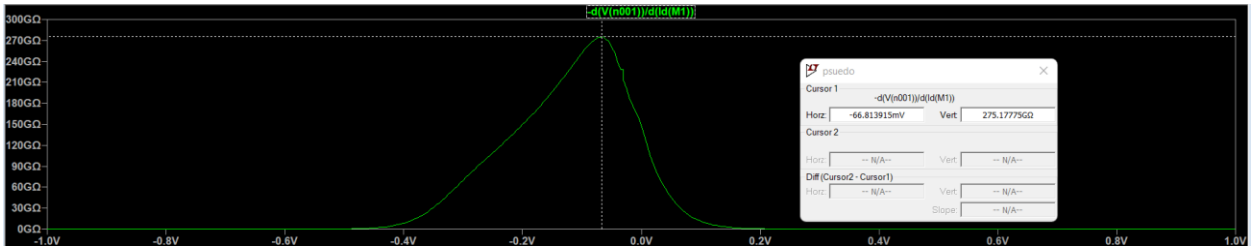
• The maximum incremental resistance is approximately 275.0 GΩ

• The pseudo resistor follows the behaviour of the pseudo resistor mentioned in [1], i.e, it shows a significantly high resistance at minute voltages (|ΔV | < 0.2V)

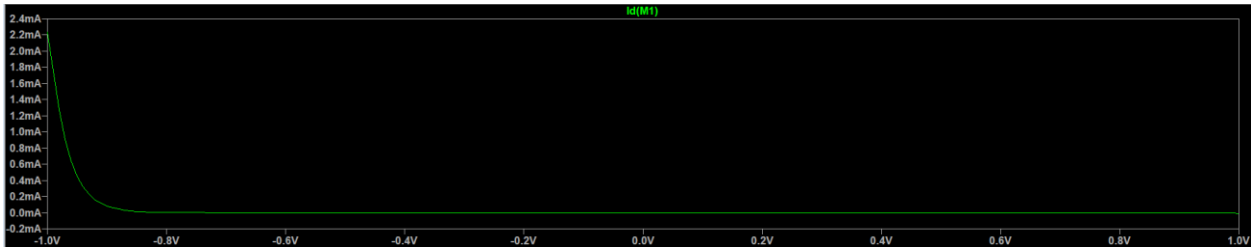
• The pseudo resistor is capable of resisting large DC offsets and provide stability when used in feedback



(A) Resistance vs Voltage -229.99117GOhm



(B). Incremental resistance vs Incremental Voltage



(C) I-V Characteristics.

igure : Pseudoresistor Simulations.

Que5.

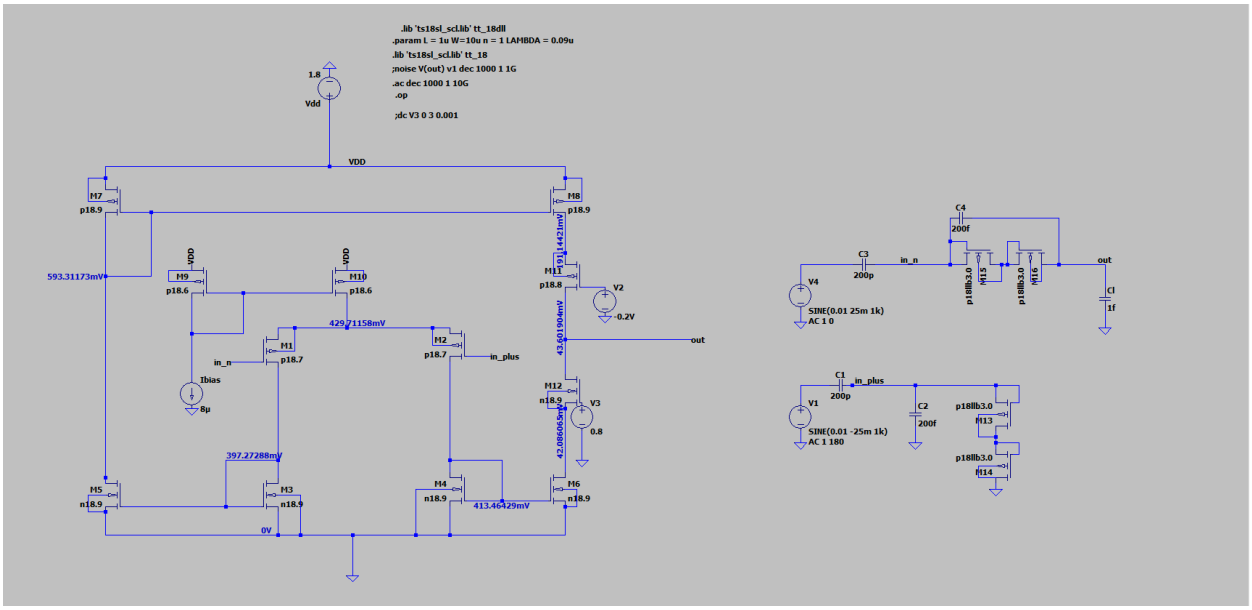


Fig: Neural Amplifier Schematic

Specifications	Value
Gain	1.3262585dB
Unity Gain Badwidth	2.837919MHz

Que6.

Final Results:

Performace	OTA
Gain	62.117163dB
Unity Gain Badwidth	5.4450265MHz
Slew Rate	5.1 MV/s
Phase Margin	42.80548°
Gain Margin	5.588399dB
ICMR	1.22 V
CMRR	103.699053dB
PSRR	60.19 dB
RMS Noise	401.77µV/
Power	43.452uW