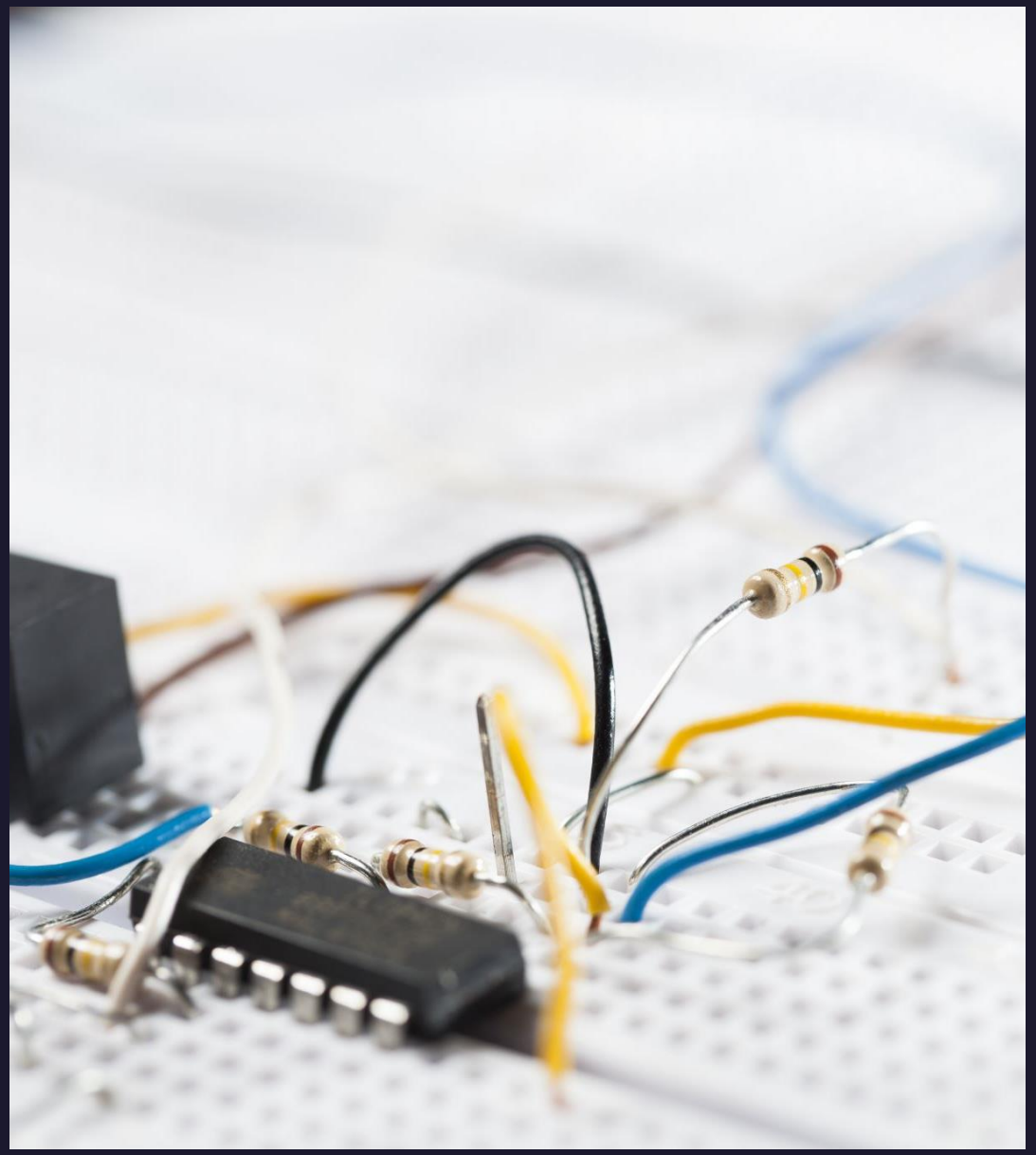

# Analog IC Design

## A Low-Power Low-Noise CMOS Amplifier for Neural Recording Applications

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# Introduction

The goal is to design a low-noise low-power bio signal amplifiers capable of amplifying signals in the millihertz-to-kilohertz range.

Fig. 1 shows the schematic of our bioamplifier design. Given in the paper.

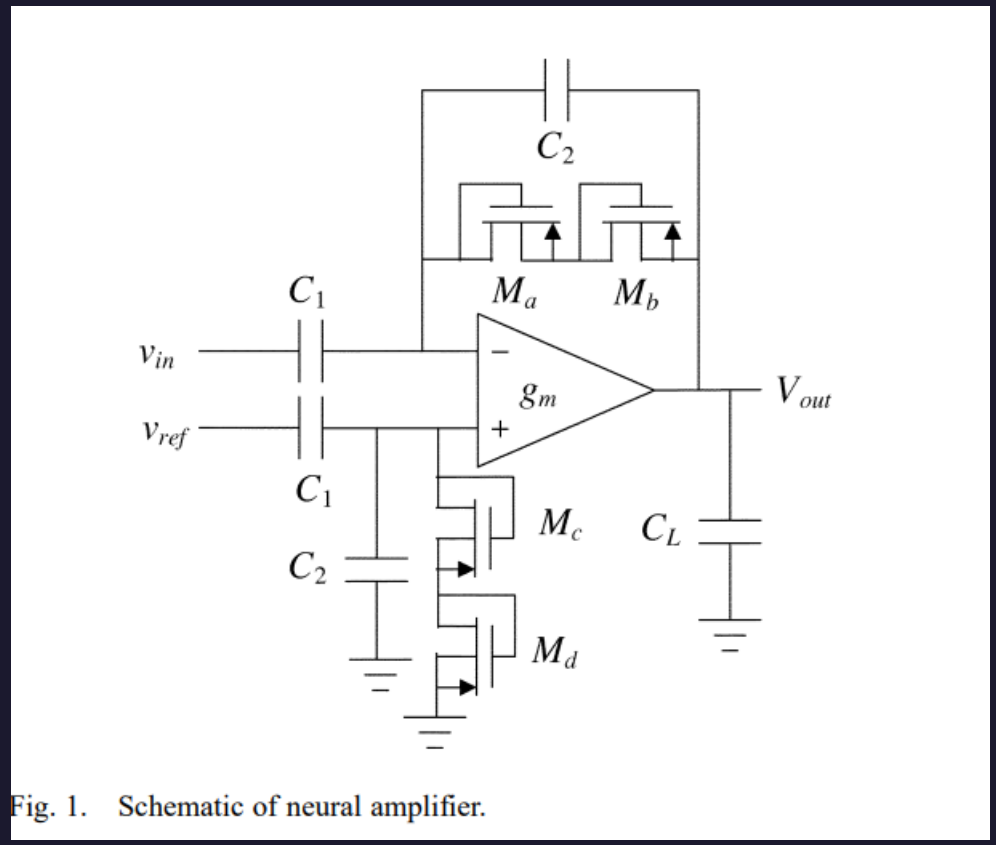



Fig. 1. Schematic of neural amplifier.

Fig 1: Schematic of Neural Amplifier

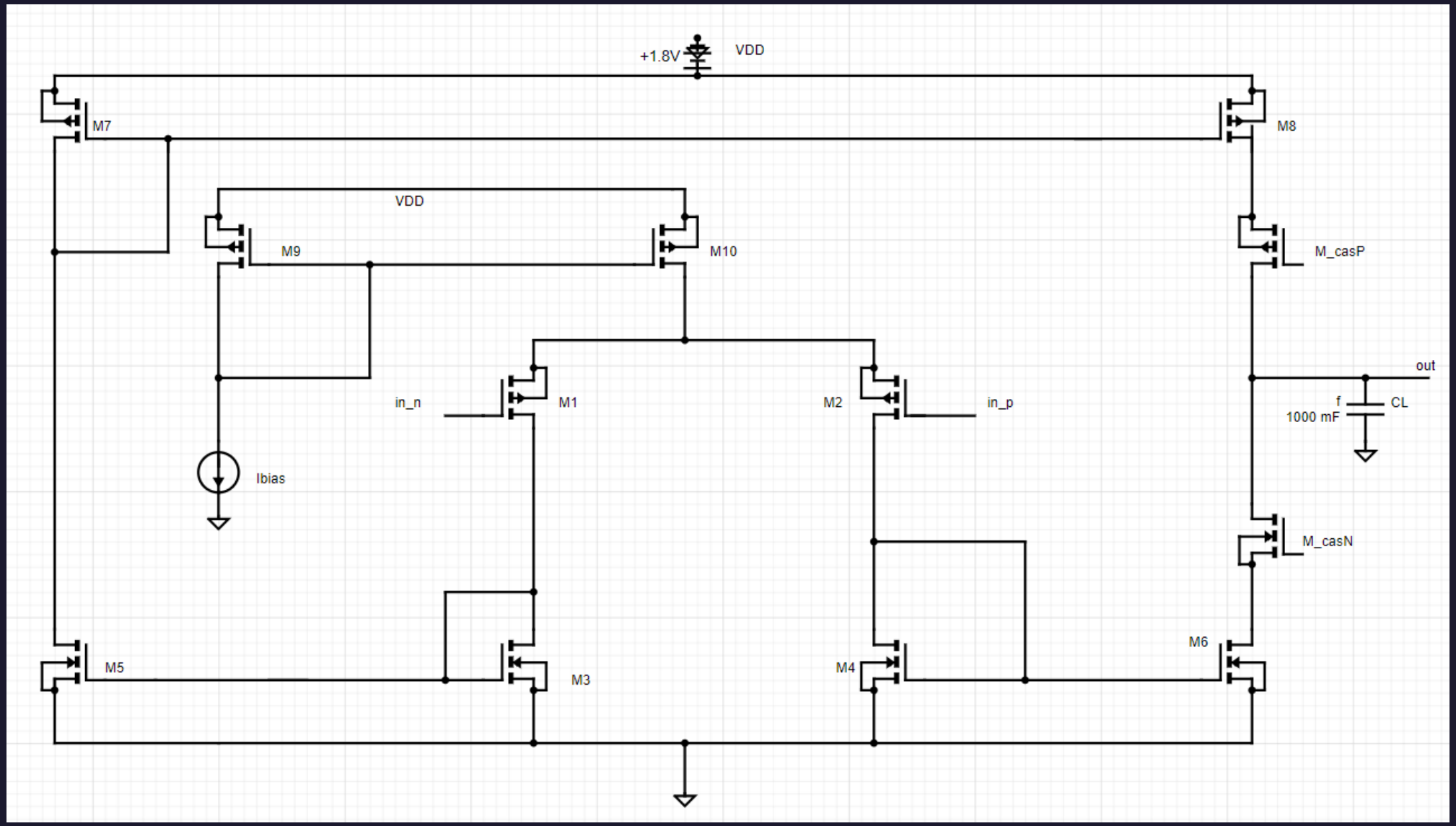



Fig 2: current-mirror OTA used in the bioamplifier.

# Output transconductance Amplifier

- Fig. 4 shows a schematic of the current-mirror OTA used in the bioamplifier. The circuit topology is a standard design suitable for driving capacitive loads, the sizing of the transistors is critical for achieving low noise at low current levels.
- The bias current is set to 8 A, giving devices – drain currents of 4 A. At this current level, each transistor may operate in weak, moderate, or strong inversion depending on its ratio.
- Given Design Specification for the OTA:

- DC gain $\geq$ 60dB.
- -3 dB bandwidth $\geq$ 10 kHz.
- Input referred noise $\leq 2\ \mu\ V_{rms}$.
- CMRR $\geq$ 100 dB.
- Noise efficiency factor (NEF) $\leq 4$
- DC power consumption $\leq 30\ \mu$A
- Supply voltage $\leq$ 1.8 V

| Devices | ID(uA) | Inversion Coeffecient | Region of Operation |
|---|---|---|---|
| M1,M2 | 4 | <1 | Subthreshold(For greater gm1) |
| M3,M4,M5,M6 | 4 | >10 | Strong Inversion |
| M7,M8 | 4 | >10 | Strong Inversion |
| M9,M10 | 8 | >10 | Strong Inversion,Saturation |
| M_cascN | 4 | 1<IC<10 | Moderate Inversion |
| M_cascP | 4 | >10 | Saturarion |

DC gain = $(gm_1 * gm * r_o^2)/2$, $gm_1$ =Transconductance of M1, gm=Transconductance of Cascode Mosfets

From Design Specifications,

1. For M1 ,M2 IC<1,

$$IC = \frac{Id}{Is} \rightarrow \frac{Id}{\frac{2\mu C_{ox} U_T^2}{\kappa} \cdot \frac{W}{L}} < 1$$ From the following we get $(\frac{W}{L})_{1,2} > 444.44$

2. Similarly for $M_{3-6} < 4.222$ $M_{7-8} < 3.4$

4. -3dB Bandwidth ≥ 10 KHZ (Dominant pole exists at -3db frequency)

$$\frac{1}{Rout * C_L} \geq 10 \text{ KHZ}$$

Assumed $C_L = 10$f farad, $\Rightarrow As, Rout = (gm * r_o^2)/2$ and $r_o = 10^7$ ohm

we get, $gm \leq 200\ \mu S$

From gm, we get $(\frac{W}{L})_{CasN} \leq 22.5$ and $(\frac{W}{L})_{CasP} \leq 45$.

- Design Parameters from Hand calculation

| Devices | Type | W/L |
|---|---|---|
| M1,M2 | p18.7 | 80/0.18 |
| M3,M4,M5,M6 | n18.9 | 10/5 |
| M7,M8 | p18.9 | 5/10 |
| M9,M10 | p18.6 | 1.2/1.2 |
| M_cascN | n18.9 | 12/3.2 |
| M_cascP | p18.8 | 6.4/3.2 |

- Specification Achieved After Hand calculations:

| Specifications | Value |
|---|---|
| Gain | 35.726628dB |
| Unity Gain Badwidth | 5.2966344MHz |
| Phase Margin | 55° |
| Gain Margin | 19.871138dB |

- Final Circuit with chosen MOSFET and sizing

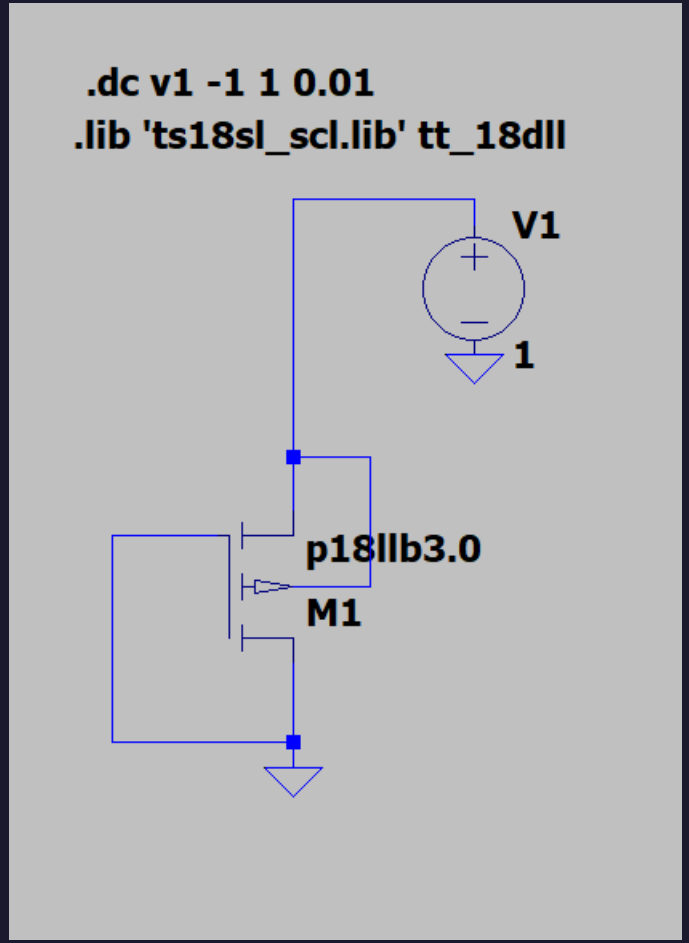
| Devices | Type | W/L | Hand Calculated |
|---|---|---|---|
| M1,M2 | p18.7 | 80/0.18 | 80/0.18 |
| M3,M4,M5,M6 | n18.9 | 27/3 | 10/5 |
| M7,M8 | p18.9 | 2/9 | 5/10 |
| M9,M10 | p18.6 | 1.2/1.2 | 1.2/1.2 |
| M_cascN | n18.9 | 40/5 | 12/3.2 |
| M_cascP | p18.8 | 90/1 | 6.4/3.2 |
| CL | 0.5pF | 1f | |

- Specification Achieved After Final design:

| Specifications | Value |
|---|---|
| Gain | 62.117163dB |
| Unity Gain Badwidth | 5.4450265MHz |
| Slew Rate | 5.1 MV/s |
| Phase Margin | 42.80548° |
| Gain Margin | 5.588399dB |

# Psuedo PMOS Resistor

- The pseudo resistor is capable of resisting large DC offsets and provide stability when used in feedback



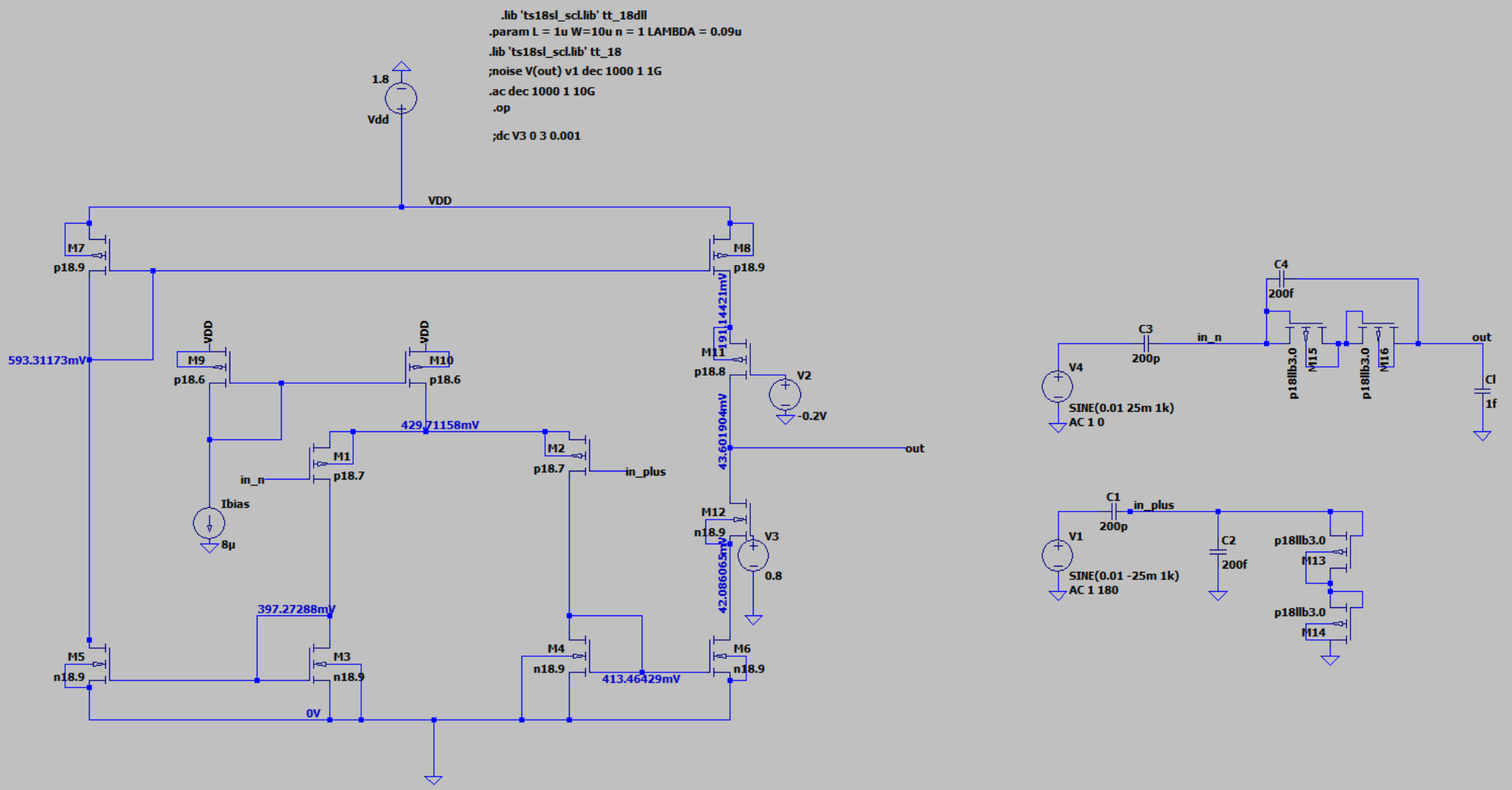
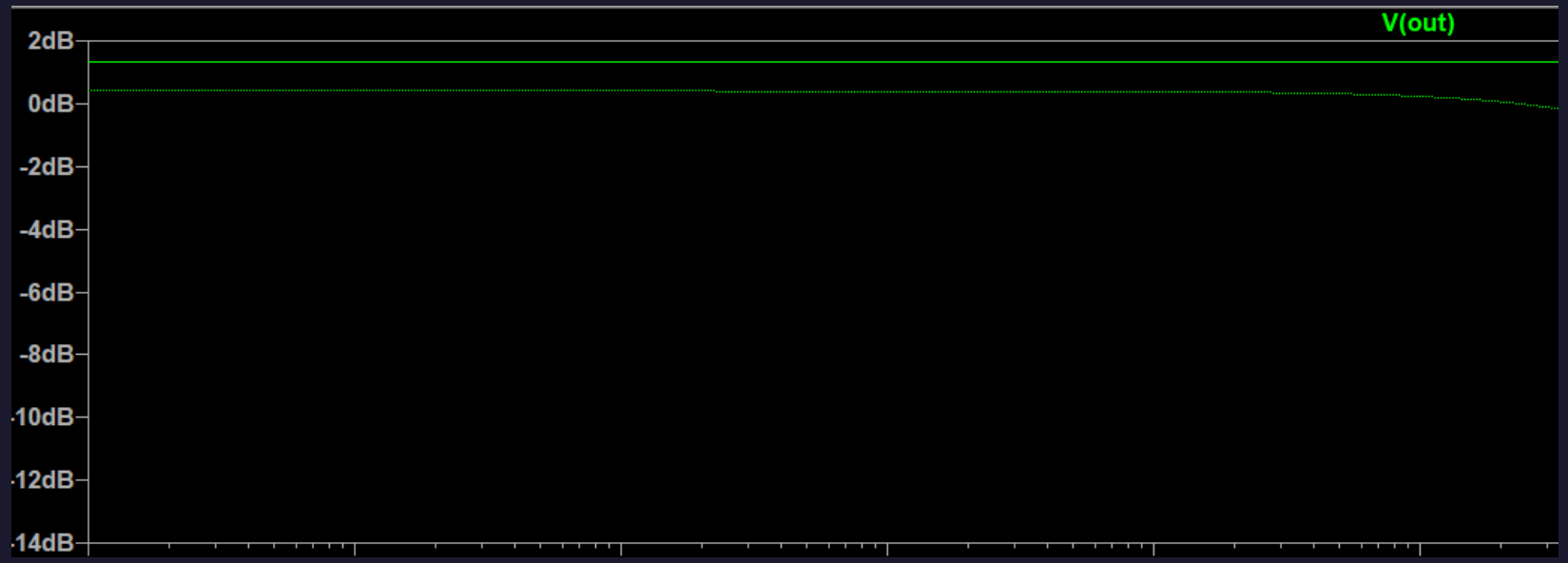



Fig: Neural Amplifier Schematic

# Neural Amplifier

| Specifications | Value |
|---|---|
| Gain | 1.3262585dB |
| Unity Gain Badwidth | 2.837919MHz |



# Final Design and Results:

| **Performace** | **OTA** |
|---|---|
| Gain | 62.117163dB |
| Unity Gain Badwidth | 5.4450265MHz |
| Slew Rate | 5.1 MV/s |
| Phase Margin | 42.80548° |
| Gain Margin | 5.588399dB |
| ICMR | 1.22 V |
| CMRR | 103.699053dB |
| PSRR | 60.19 dB |
| RMS Noise | $401.77\mu V/\sqrt{Hz}$ |
| Power | 43.452uW |