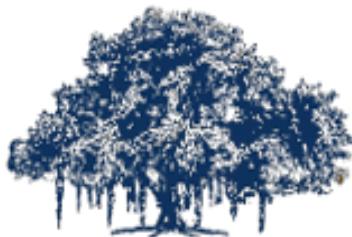


ANALOG IC DESIGN
PROJECT REPORT
MONSOON 2021

Submitted by : **ADITYA GUPTA (2021702002)**
(MS by Research ECE)

Under the guidance of
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INTERNATIONAL INSTITUTE OF
INFORMATION TECHNOLOGY
H Y D E R A B A D

ACKNOWLEDGEMENT

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MS by Research ECE

ABSTRACT

The aim of the project was to learn and implement the concepts behind working and designing of Operational Transconductance Amplifier (OTA).

Through the project an understanding of how to choose an appropriate architecture based on the desired specifications and requirements was built. Furthermore, intricacies involved with the certain tradeoffs, cost requirements and how to counter design related problems were also learnt.

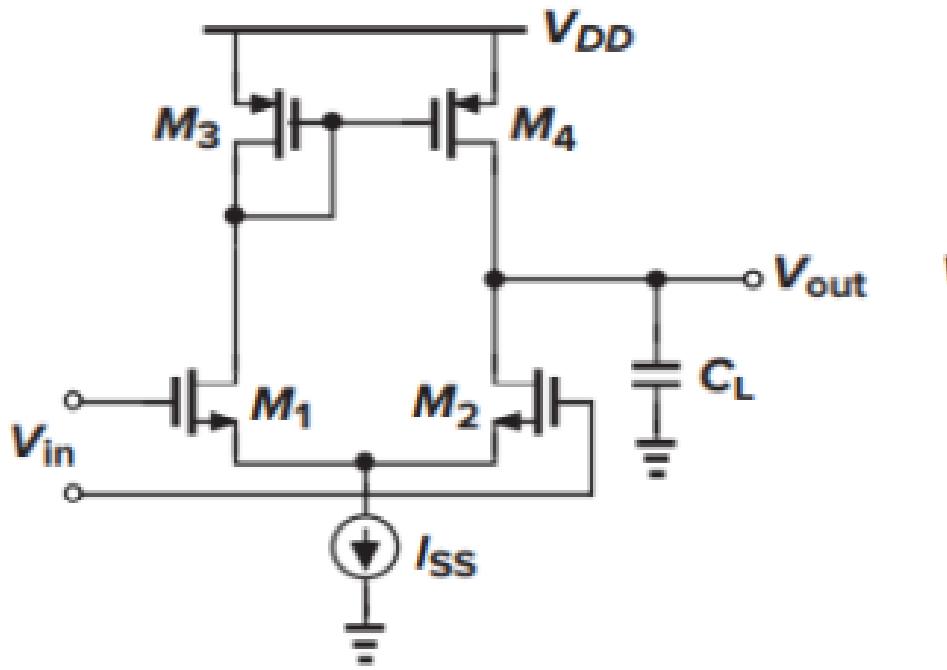
2.a) THEORY

The operational transconductance amplifier (OTA) is an amplifier whose differential input voltage produces an output current. Thus, it is a voltage controlled current source (VCCS).

OTA is similar to a standard operational amplifier in that it has a high impedance differential input stage and that it may be used with negative feedback.

Simple one stage op amp topologies:

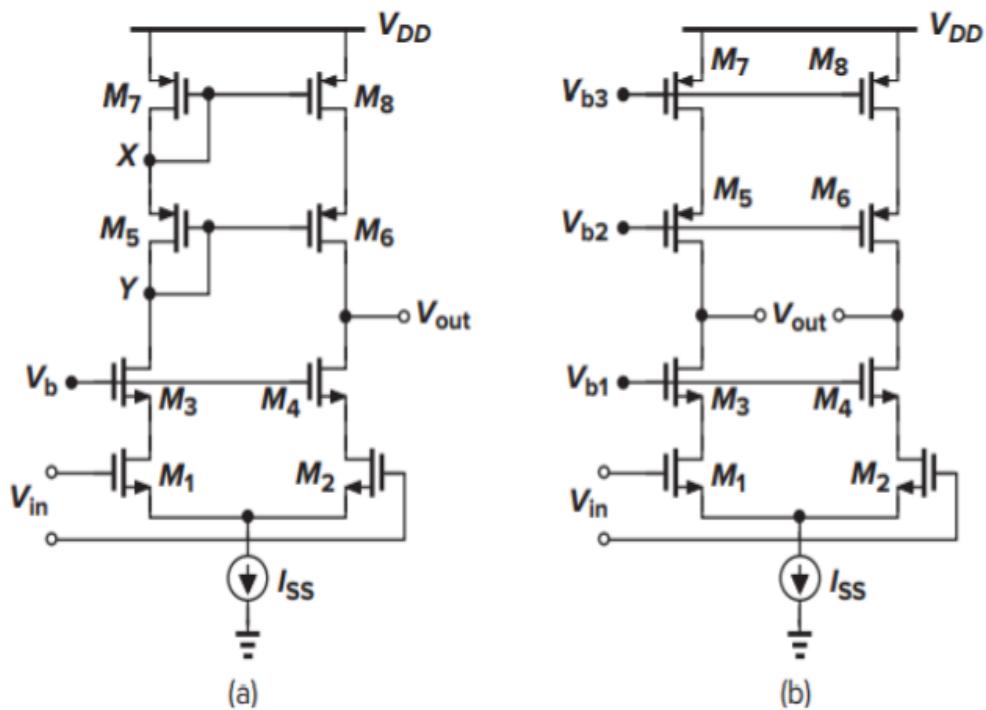
Classical 5T-OTA



The small-signal, low-frequency gain of this circuit is equal to $gm_2(r_{ON}||r_{OP})$.

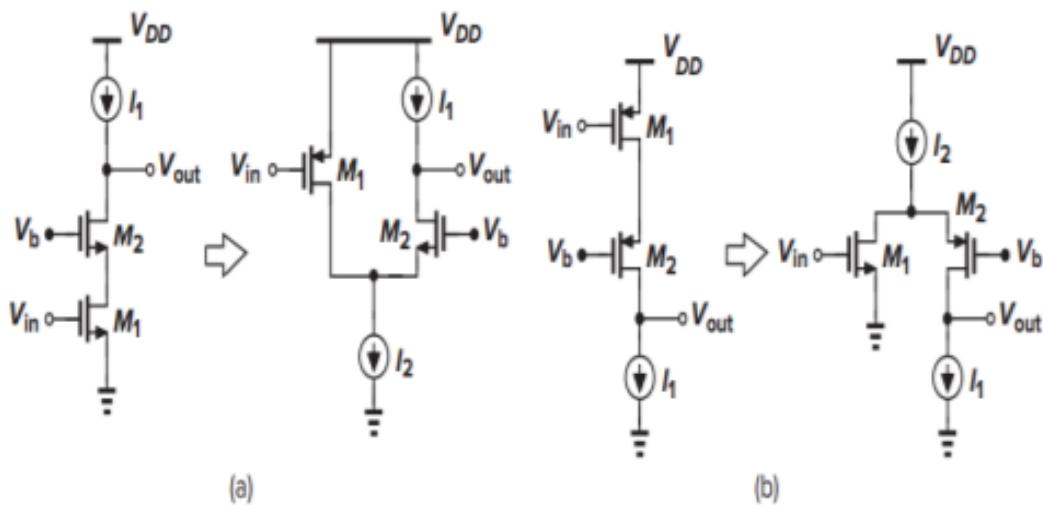
In order to achieve a high gain, the differential cascode topologies are used.

Cacode OTA



Figs. (a) and (b) shows circuit for single-ended and differential output generation, respectively. such circuits display a gain on the order of $gm_2 [(gm_n R_{on}^2)||(g_m p R_{op}^2)]$, but at the cost of output swing and additional poles. These configurations are called telescopic cascode opamp.

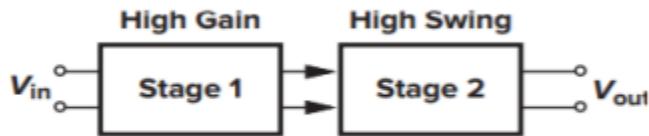
Folded cascode OTA



In order to alleviate the drawbacks of telescopic cascode op amps, namely, limited output swings and difficulty in choosing equal input and output CM levels, a “folded-cascode” op amp can be used.

In an NMOS or PMOS cascode amplifier, the input device is replaced by the opposite type while still converting the input voltage to a current. In the four circuits shown in Fig. 10.10, the small-signal current generated by M1 flows through M2 and subsequently the load, producing an output voltage approximately equal to $gm_1 R_{out} V_{in}$. The primary advantage of the folded structure lies in the choice of the voltage levels because it does not “stack” the cascode transistor on top of the input device.

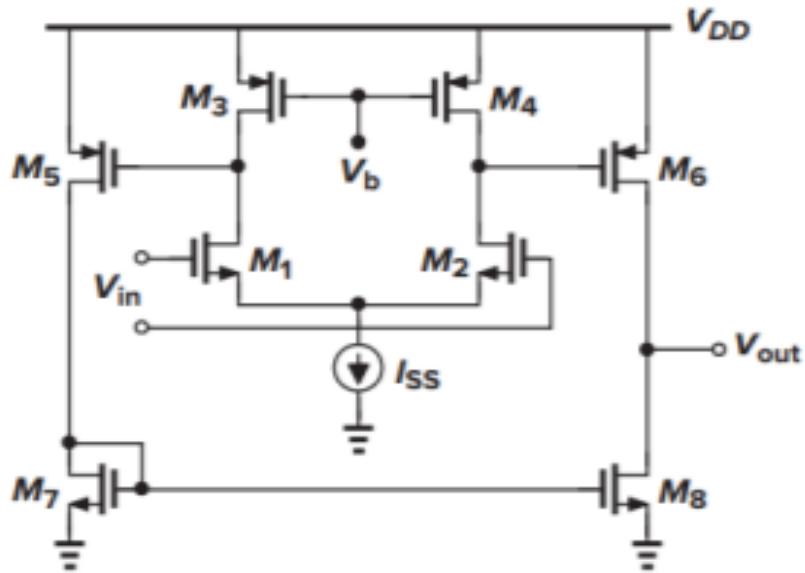
TWO STAGE OPAMP



The opamps seen thus far exhibit a “one-stage” nature in that they allow the small-signal current produced by the input pair to flow directly through the output impedance, i.e., they perform voltage to current conversion only once.

The gain of these topologies is therefore limited to the product of the input pair transconductance and the output impedance. We have also observed that cascoding in such circuits increases the gain while limiting the output swings.

In some applications, the gain and/or the output swings provided by cascode op amps are not adequate. For example, a modern op amp must operate with supply voltages as low as 0.9 V while delivering singleended output swings as large as 0.8 V. In such cases, we resort to “two-stage” op amps, with the first stage providing a high gain and the second, large swings . In contrast to cascode op amps, a two-stage configuration isolates the gain and swing requirements.



Two stage classical topology

The first and second stages exhibit gains equal to $gm_{1,2}(ro_{1,2}||ro_{3,4})$ and $gm_{5,6}(ro_{5,6}||ro_{7,8})$, respectively. The overall gain is comparable to the cascode opamp but the swing at v_{out1} and v_{out2} is equal to $V_{DD} - |V_{O\,D5,6}| - V_{O\,D7,8}$, the highest possible value.

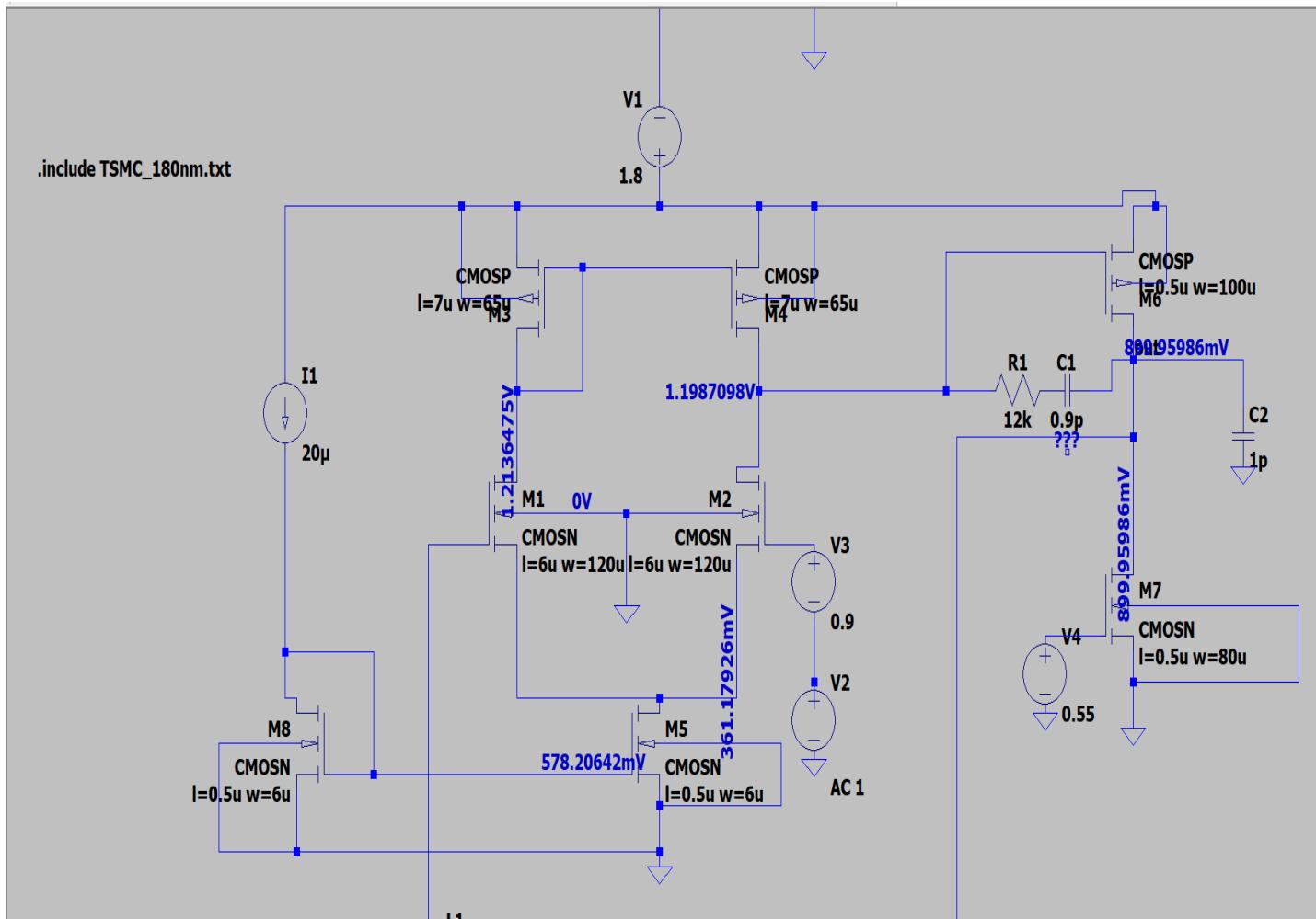
Design specifications

- DC gain $\geq 80\text{dB}$.
- Unity gain frequency $\geq 10 \text{ MHz}$.
- Output voltage swing $\geq 1\text{Vpp}$.
- Slew rate $\geq 100\text{V}/\mu\text{s}$.
- Phase Margin $\geq 65^\circ$.
- Input referred noise (Thermal only) = $10\text{nV}/\sqrt{\text{Hz}}$.
- Input Common mode voltage = 0.9V .
- Output load capacitance = 1pf

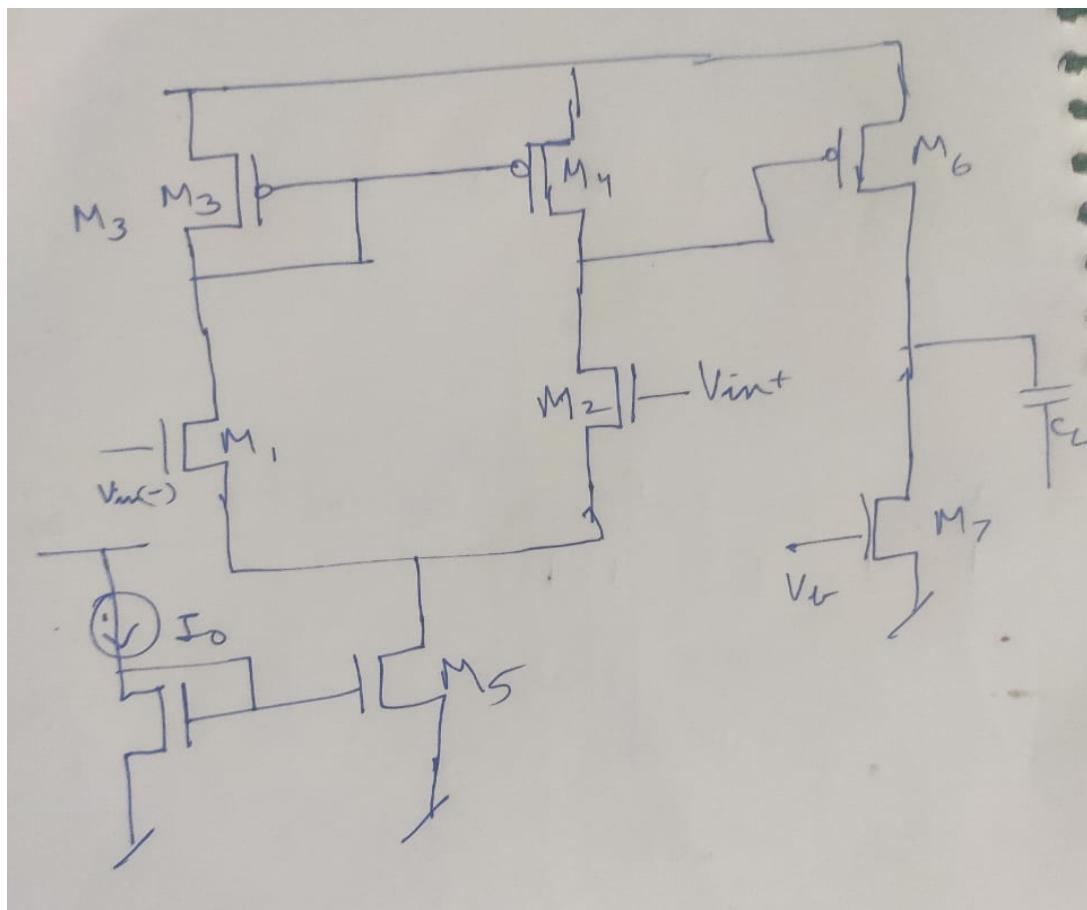
For my project I have used the two stage classical OTA topology , I first tried with single stage OTA but the gain was too low and increasing gain required W and L to be really large , then i tried single stage telescopic cascode OTA , but i could not meet some specs with it , then I used 2 stage classical OTA topology.

2.b) Architecture

This is the architecture of my design with sizes and values mentioned-



2.c) Hand calculations for the design



Using 2nd stage with PMOS
for better biasing

Since, we are using 2 stages for high gain
negative compensation C to get the required
phase margin



$$v_o = \frac{v_{in}}{C_C(1+A)} \cdot \frac{1}{1 + s \left(\frac{1}{P_1} + \frac{1}{P_2} \right) + s^2 \left(\frac{1}{P_1 P_2} \right)}$$

$$\frac{v_o}{v_{in}} = A_{DC} \cdot \frac{\left(1 - \frac{s}{\omega} \right)}{\left(1 + \frac{s}{P_1} \right) \left(1 + \frac{s}{P_2} \right)}$$

$$A_{DC} \cdot \frac{\left(1 - \frac{s}{\omega} \right)}{1 + s \left(\frac{1}{P_1} + \frac{1}{P_2} \right) + s^2 \left(\frac{1}{P_1 P_2} \right)}$$

$$\therefore P_1 \ll P_2 \therefore \frac{1}{P_2} \ll \frac{1}{P_1}$$

$$s \left(\frac{1}{P_1} + \frac{1}{P_2} \right) \approx s \frac{1}{P_1}$$

$$R_1 = \frac{1}{R_2(C_C + C_L)} + R_1(C_C + C_L) + g_m R_2 R_1 C_0$$

$$P_1 \approx \frac{1}{g_m R_2 R_1 g_m}$$

$$P_1 P_2 = \frac{1}{R_1 R_2 (C_1 C_2 + C_1 C_C + C_2 C_C)}$$

$$P_2 \approx \frac{g_m R_1 C_0}{C_2 C_C}$$

$$Z = \frac{g_m}{C_C}, \quad P_1 = \frac{1}{g_m R_1 R_2 C_C}$$

$$P_2 = \frac{g_m}{C_2}$$

$$A_{DC} = g_m R_1 \cdot g_m R_2$$

$$\text{GBW} = \text{DC gain} \times P_1$$

$$= \frac{g_m_1 R_1 g_m_2 R_2 \times 1}{g_m_2 R_1 R_2 C_C}$$

$$\text{GBW} = \frac{g_m_1}{C_C}$$

for slew rate

$$\text{SR.} = \frac{I_o}{C_C}$$

phase margin

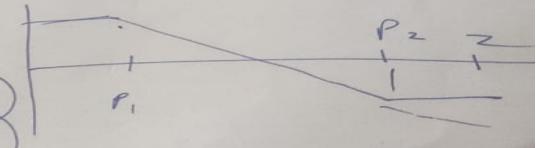
$$\angle \frac{V_o}{V_{in}} = -\tan^{-1}\left(\frac{w}{P_1}\right)$$

$$-\tan^{-1}\left(\frac{w}{P_2}\right)$$

$$-\tan^{-1}\left(\frac{w}{P_3}\right)$$

$$w = \text{GBW} = 10^2$$

$$\angle \frac{V_o}{V_{in}} = \tan^{-1}\left(\frac{1}{10^2}\right) - \tan^{-1}\left(\frac{g_m_1 g_m_2 R_1 R_2 C_C}{C_C g_m_2}\right) - \tan^{-1}\left(\frac{g_m_1}{C_C}\right)$$



$$= -\tan^{-1}\left(\frac{1}{10^2}\right) - \tan^{-1}\left(g_m_1 g_m_2 R_1 R_2\right)$$

$$-\tan^{-1}\left(\frac{g_m_1 C_2}{C_C g_m_2}\right)$$

$$= -\tan^{-1}\left(\frac{1}{10^2}\right) - \tan^{-1}(A_{DC}) - \tan^{-1}\left(\frac{\text{GBW}}{R_2}\right)$$

$$-180 + PM = -5.71 - 90 - \tan^{-1}\left(\frac{\text{GBW}}{R_2}\right)$$

$$PM = 84.29 - \tan^{-1}\left(\frac{\text{GBW}}{R_2}\right)$$

for 65°

$$\frac{\text{GBW}}{R_2} = \tan(20)$$

$$R_2 \geq 2.4 \text{ GBW}$$

$$C_E \geq 0.24 C_L$$

$$C_L = 1 \text{ PF}$$

$$C_E \approx 0.25 \text{ PF}$$

$$C_E \approx 0.5 \text{ PF}$$

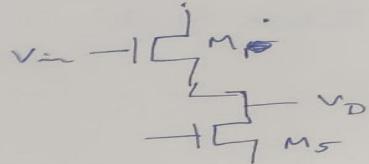
For $g_m =$

$$g_m^2 = 2 I_D \mu n C_{ox} \left(\frac{w}{l}\right)^2$$

$$g_m = 150$$

$$\left(\frac{w}{l}\right)_1 = \cancel{17.34}$$

$$\left(\frac{w}{l}\right)_1 = \left(\frac{w}{l}\right)_2 = 5.18$$



$$V_{DS} > V_s - V_T$$

$$V_{in} \geq V_{gs1} + V_{DSat}$$

$$I_{CMR} \geq V_{gs1} + V_{DSat}$$

$$I_{CMR} \geq \left(\sqrt{\frac{2 I_{D1}}{\beta_1}} + V_{DSat1} \right)_{max} + V_{DSat}$$

For I_{CM} voltage = 0.9

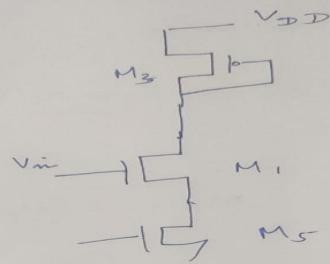
$$V_{DSat} = I_{DS} = \frac{\mu n C_{ox} \left(\frac{w}{l}\right)_S (V_{DSat})}{2}$$

$$\left(\frac{w}{l}\right)_S = \frac{2 I_{DS} - }{\mu n C_{ox} \times (V_{DSat})^2}$$

$$= \frac{2 \times 210}{300 \times (0.1)^2}$$

$$= 12$$

$$\left(\frac{w}{l}\right)_S = 12$$



$$V_{in \ max} = V_{D1} + V_{t1}$$

$$V_{D1} = V_{DD} - V_{sg3}$$

$$V_{D1} = V_{DD} - \left[\sqrt{\frac{2I_2}{P}} + |V_{t2}| \right]$$

$$V_{in \ max} \leq V_{D1} + V_{t1}$$

Putting values we get

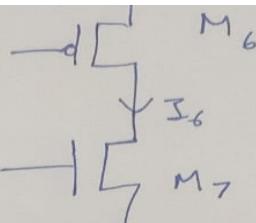
$$\left(\frac{W}{L}\right)_{3,4} = \frac{2 \times 10\mu}{70 [0.2]^2} = 7.14 \approx 7$$

$$\left(\frac{W}{L}\right)_3 \geq \approx 8$$

for 65° PM

$$g_{m6} \geq 10g_{m1} \quad \rightarrow \quad \left(\frac{W}{L}\right)_6 \geq 10 \left(\frac{W}{L}\right)_1$$

$$g_{m6} \geq 1600\mu$$



$$\frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_4} = \frac{g_{m6}}{g_{m4}} \cdot \left(\frac{W}{L}\right)_4$$

$$= 20 \times 7.5 = 150$$

$$\left(\frac{W}{L}\right)_7 = \frac{I_7}{I_5} \left(\frac{W}{L}\right)_5 = 140$$

2.d) Calculated design parameters:

Values	Calculation
(w/l)(1,2)	18
(w/l)(3,4)	7.5
(w/l)(5,8)	12
(w/l)(6)	160
(w/l)(7)	140
C _c	0.5
Nulling resistor	As required

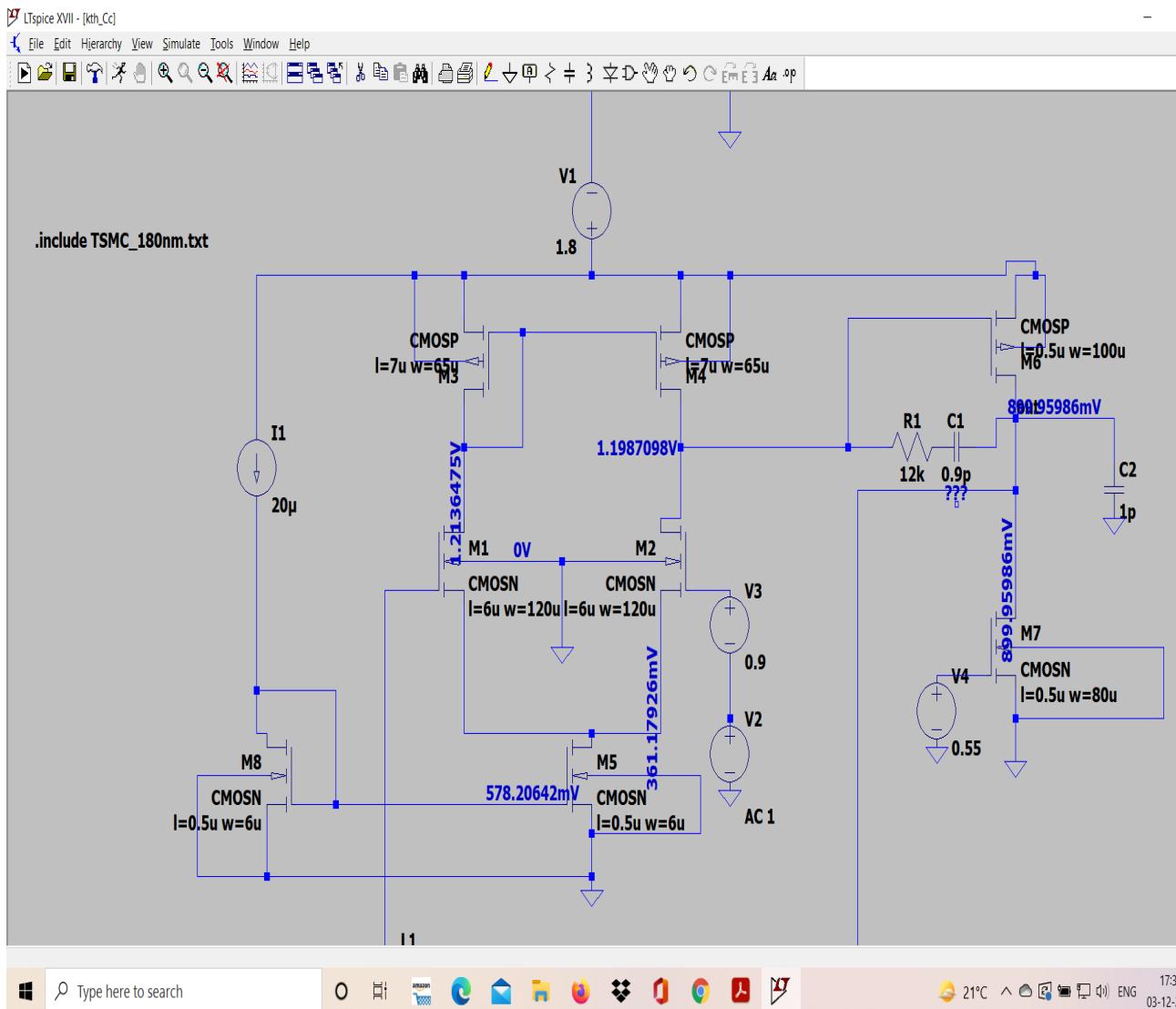
2.e) Calculated specifications:

Values	Calculation
DC gain	83dB
Unity gain frequency	15MHz
Slew rate	100
Phase margin	65

3.a)Netlist extracted from lt spice:

```
M1 N003 N004 N009 0 CMOSN l=6u w=120u
M2 N002 N005 N009 0 CMOSN l=6u w=120u
M5 N009 N007 0 0 CMOSN l=0.5u w=6u
M6 out N002 N001 N001 CMOSP l=0.5u w=100u
M7 out N006 0 0 CMOSN l=0.5u w=80u
V1 N001 0 1.8
I1 N001 N007 20μ
M8 N007 N007 0 0 CMOSN l=0.5u w=6u
V3 N005 N008 0.9
V4 N006 0 0.55
C2 out 0 1p
M3 N003 N003 N001 N001 CMOSP l=7u w=65u
M4 N002 N003 N001 N001 CMOSP l=7u w=65u
L1 out N004 1e17
C1 out P001 0.9p
R1 P001 N002 12k
V2 N008 0 AC 1
.model NMOS NMOS
.model PMOS PMOS
.lib C:\Users\aditya
gupta\Documents\LTspiceXVII\lib\cmp\standard.mos
.include TSMC_180nm.txt
;op dec 10 1 10g
.ac dec 10 1 10g
;tran 0 1m 10u 10u
.backanno
.end
```

Lt spice schematic



3.b) After tuning the amplifier for correct simulations several values were changed to meet the specifications

Values	Hand Calculation	Simulation value
(w/l)(1,2)	18	20
(w/l)(3,4)	7.5	20
(w/l)(5,8)	12	9.3
(w/l)(6)	160	200
(w/l)(7)	140	160
Cc	0.5p	0.9p
Nulling resistor	As required	12k

3.c) operating point

Voltages of every node

```
* C:\Users\aditya gupta\Desktop\analog project\withCc\kth_Cc.asc
--- Operating Point ---
V(n003):      1.21365    voltage
V(n004):      0.89996    voltage
V(n009):      0.361179   voltage
V(n002):      1.19871    voltage
V(n005):      0.9        voltage
V(n007):      0.578206   voltage
V(out):       0.89996    voltage
V(n001):      1.8        voltage
V(n006):      0.55       voltage
V(n008):      0          voltage
V(p001):      1.19871    voltage
Id(M4):       -9.61001e-006 device_current
Ig(M4):       -0          device_current
Ib(M4):       6.1129e-013  device_current
Is(M4):       9.61001e-006 device_current
Id(M3):       -9.60755e-006 device_current
Ig(M3):       -0          device_current
Ib(M3):       5.96353e-013  device_current
Is(M3):       9.60755e-006 device_current
Id(M6):       -0.000176825  device_current
Ig(M6):       -0          device_current
Ib(M6):       9.1004e-013   device_current
Is(M6):       0.000176825  device_current
Id(M8):       2e-005      device_current
Ig(M8):       0          device_current
Ib(M8):       -5.88206e-013 device_current
Is(M8):       -2e-005     device_current
```

All the parameters of every transistor:

SPICE Error Log: C:\Users\aditya gupta\Desktop\analog project\withCc\kth_Cc.log					
Warning: Ps = 0 is less than W. Direct Newton iteration for .op point succeeded. Semiconductor Device Operating Points:					
--- BSIM3 MOSFETS ---					
Name:	m4	m3	m6	m8	m7
Model:	cmosp	cmosp	cmosp	cmosn	cmosn
Id:	-9.61e-06	-9.61e-06	-1.77e-04	2.00e-05	1.77e-04
Vgs:	-5.86e-01	-5.86e-01	-6.01e-01	5.78e-01	5.50e-01
Vds:	-6.01e-01	-5.86e-01	-9.00e-01	5.78e-01	9.00e-01
Vbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Vth:	-3.99e-01	-3.99e-01	-4.53e-01	4.66e-01	4.64e-01
Vdsat:	-1.58e-01	-1.58e-01	-1.37e-01	1.04e-01	8.86e-02
Gm:	9.52e-05	9.52e-05	2.03e-03	3.03e-04	3.02e-03
Gds:	1.64e-07	1.66e-07	2.25e-05	3.41e-06	3.12e-05
Gmb:	3.04e-05	3.04e-05	6.39e-04	8.43e-05	8.45e-04
Cbd:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00	0.00e+00	0.00e+00	0.00e+00
Cgsov:	4.11e-14	4.11e-14	6.32e-14	4.25e-15	5.66e-14
Cgdov:	4.11e-14	4.11e-14	6.32e-14	4.25e-15	5.66e-14
Cgbov:	6.94e-18	6.94e-18	4.39e-19	4.69e-19	4.69e-19
dQgdVgb:	3.11e-12	3.11e-12	4.31e-13	2.76e-14	3.61e-13
dQgdVdb:	-4.27e-14	-4.29e-14	-6.32e-14	-4.15e-15	-5.54e-14
dQgdVsb:	-2.92e-12	-2.92e-12	-3.55e-13	-2.20e-14	-2.82e-13
dQddVgb:	-1.30e-12	-1.30e-12	-1.84e-13	-1.18e-14	-1.52e-13
dQddVdb:	4.24e-14	4.25e-14	6.32e-14	4.19e-15	5.59e-14
dQddVsb:	1.67e-12	1.67e-12	1.60e-13	9.93e-15	1.26e-13
dQbdVgb:	-5.08e-13	-5.07e-13	-6.28e-14	-4.08e-15	-5.57e-14
dQbdVdb:	-1.03e-15	-1.12e-15	-2.06e-17	8.60e-18	1.50e-16
dQbdVsb:	-4.60e-13	-4.60e-13	-2.81e-14	-2.13e-15	-2.74e-14

SPICE Error Log: C:\Users\aditya gupta\Desktop\analog project\withCc\kth_Cc.log		
Name:	m5	m2
Model:	cmosn	cmosn
Id:	1.92e-05	9.61e-06
Vgs:	5.78e-01	5.39e-01
Vds:	3.61e-01	8.38e-01
Vbs:	0.00e+00	-3.61e-01
Vth:	4.68e-01	4.95e-01
Vdsat:	1.03e-01	6.89e-02
Gm:	2.94e-04	1.97e-04
Gds:	3.95e-06	3.64e-07
Gmb:	8.18e-05	4.96e-05
Cbd:	0.00e+00	0.00e+00
Cbs:	0.00e+00	0.00e+00
Cgsov:	4.25e-15	8.50e-14
Cgdov:	4.25e-15	8.50e-14
Cgbov:	4.69e-19	5.97e-18
dQgdVgb:	2.76e-14	4.16e-12
dQgdVdb:	-4.16e-15	-8.31e-14
dQgdVsb:	-2.19e-14	-3.54e-12
dQddVgb:	-1.18e-14	-1.64e-12
dQddVdb:	4.21e-15	8.39e-14
dQddVsb:	9.92e-15	1.98e-12
dQbdVgb:	-4.07e-15	-8.75e-13
dQbdVdb:	-5.08e-18	2.03e-16
dQbdVsb:	-2.14e-15	-5.07e-13

Date: Fri Dec 03 23:56:49 2021

3.d) Stability analysis simulation



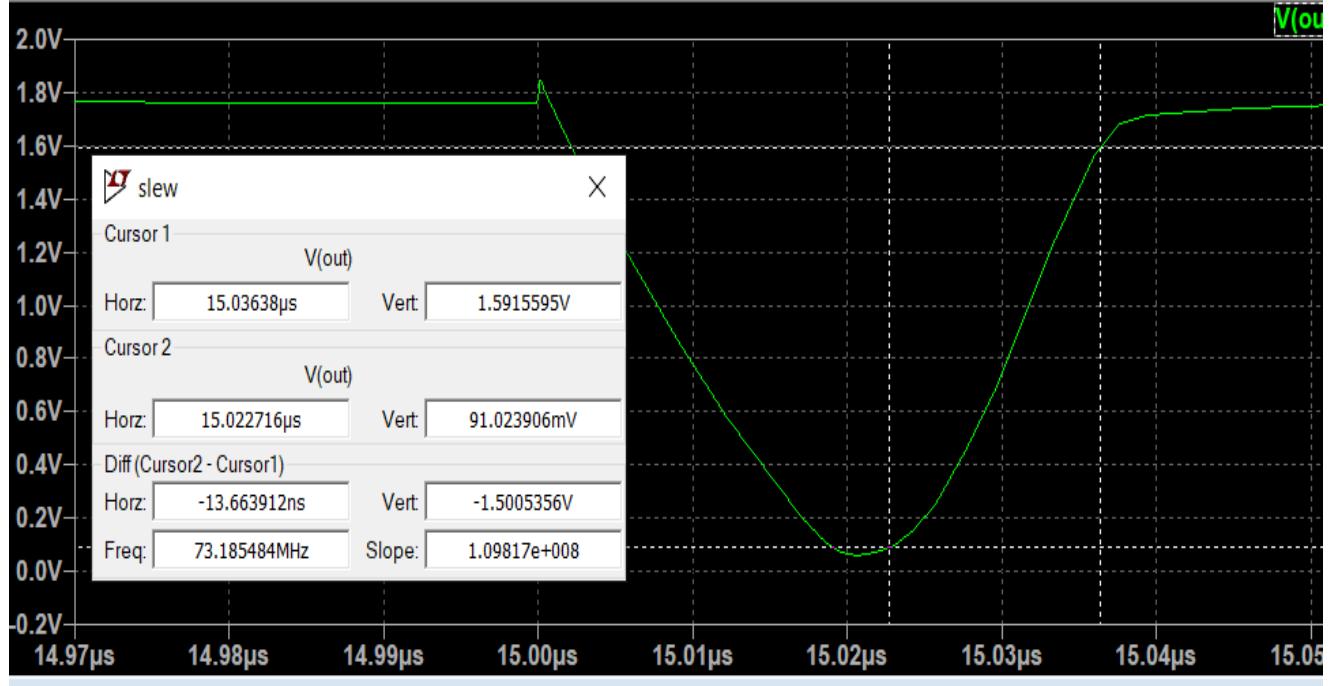
From the simulation we can see,

$$\text{gain} = 80.4 \text{ dB}$$

$$\text{Phase margin} = 67$$

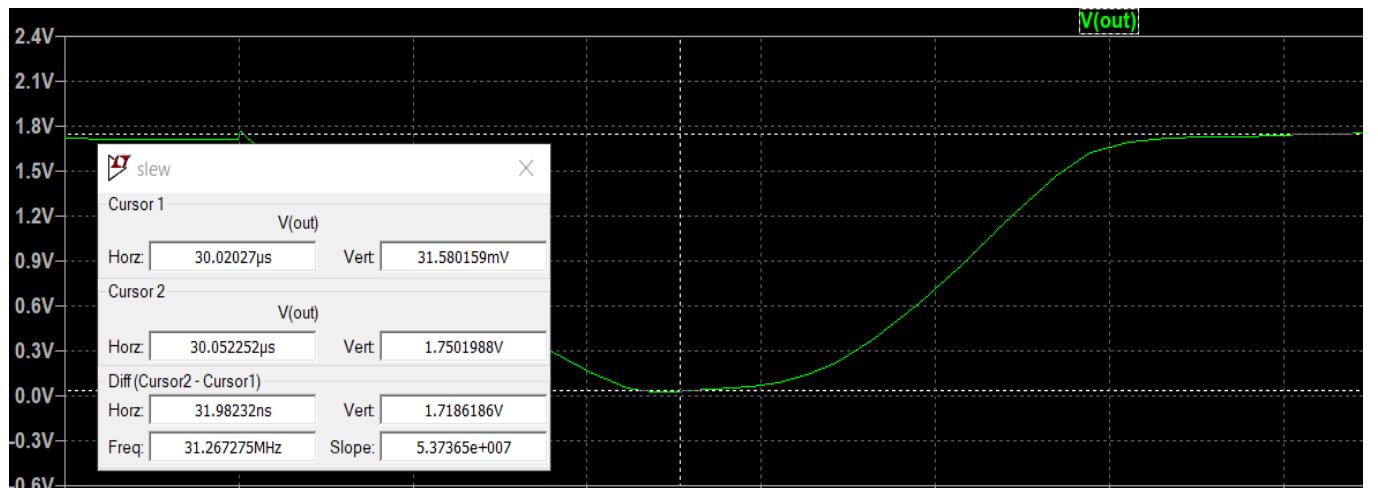
$$\text{unity gain frequency} = 11.25 \text{ MHz}$$

3.e) Slew rate



$$\text{Slew rate} = 110 \text{V/usec}$$

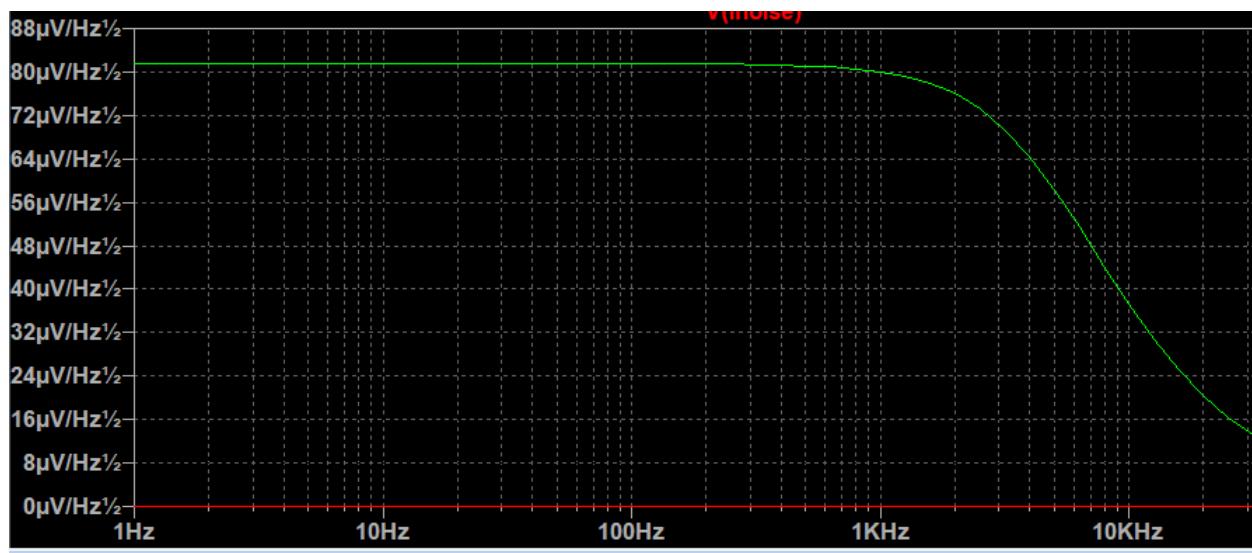
3.f) Settling time



$$\text{Settling time} = 32 \text{ns}$$

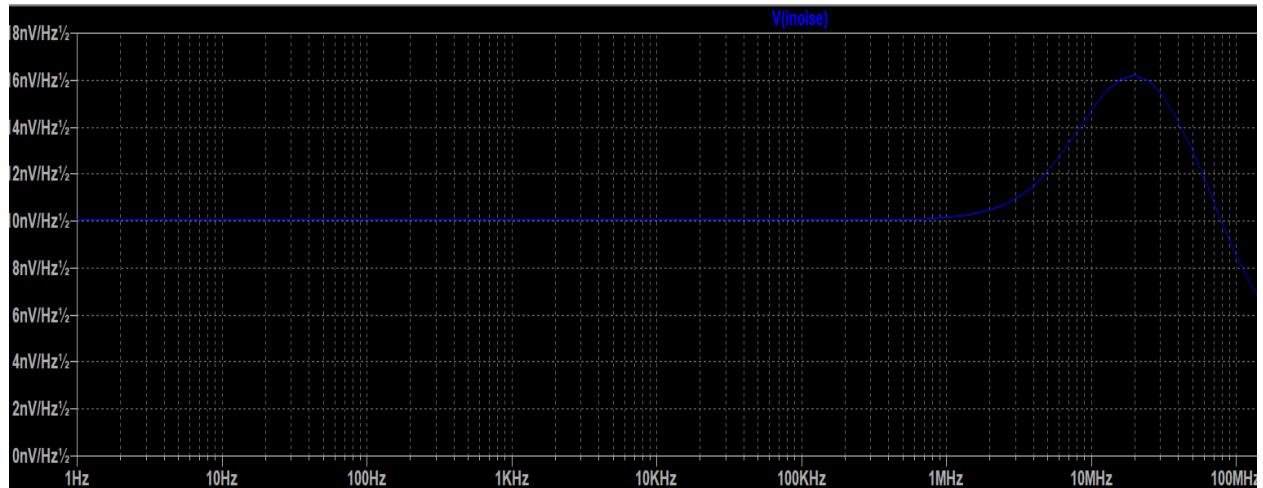
3.g) V_{out} at $V_{in} = 0$ gives offset
Offset value = 3.6mV

3.h) Noise: output noise



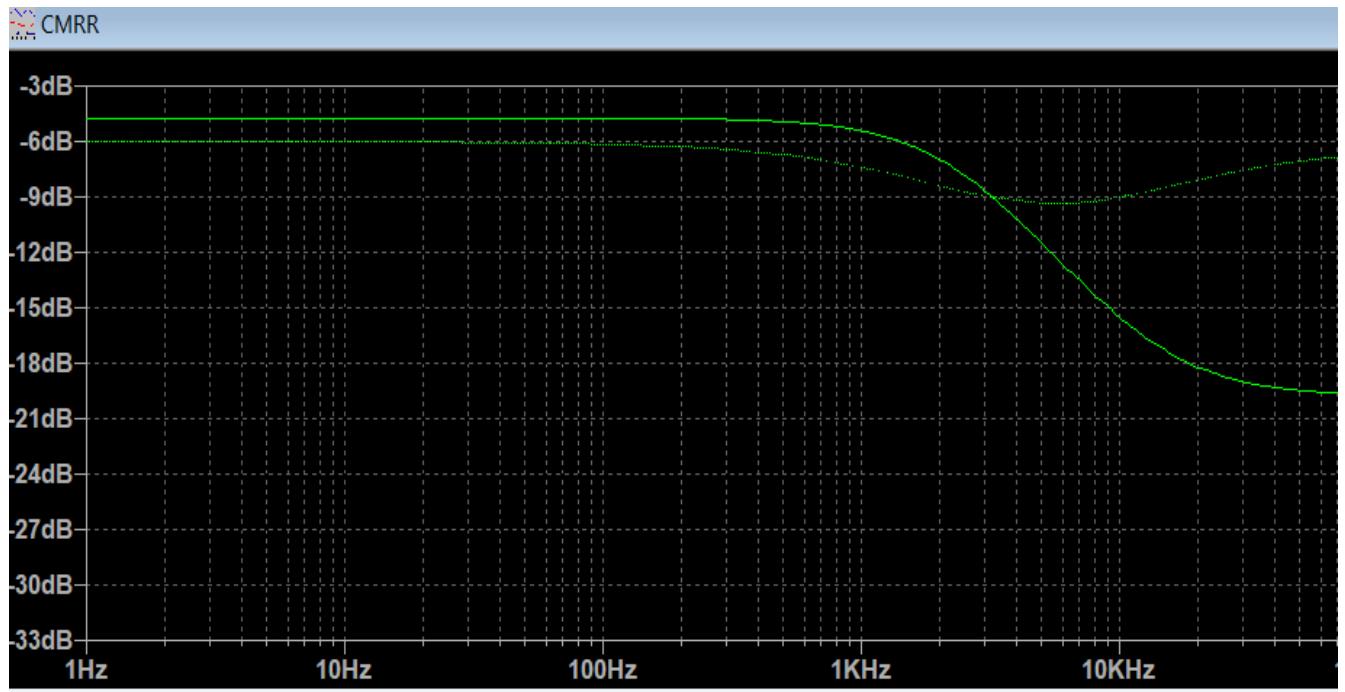
Output noise: $80\mu\text{V}/\sqrt{\text{Hz}}$

Input referred noise



$$\text{Noise} = 9.8 \text{nV}/\sqrt{\text{Hz}}$$

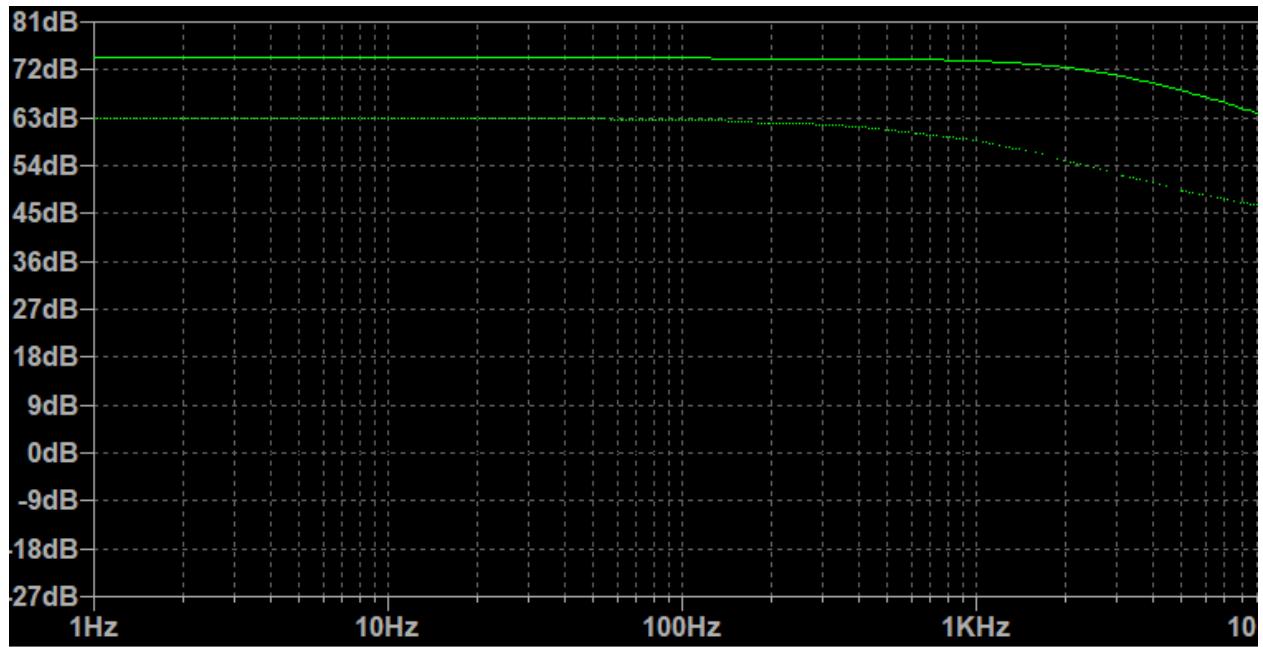
3.i) CMRR



$$\text{CMRR} = \text{Adm}/\text{Acm} = \text{Adm(dB)} - \text{Acm(dB)}$$

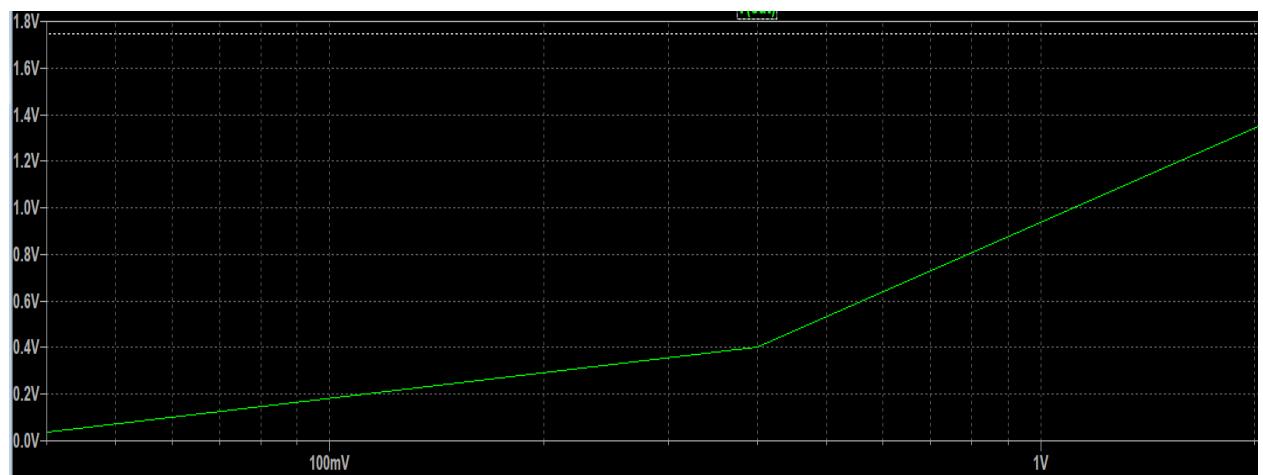
$$80.4 + 4.8 = 85.2 \text{dB}$$

3.j)For PSRR Gain at Vdd=1.2V



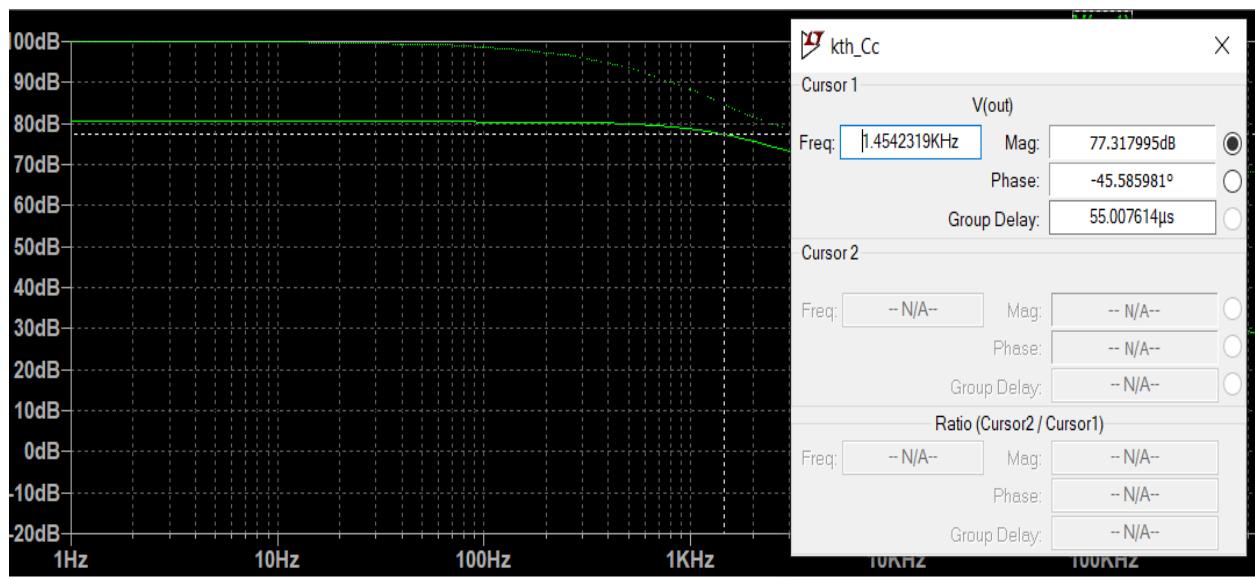
$$Psrr = -20\log(0.6)+(80.4-74)=21.8\text{dB}$$

3.k)ICMR



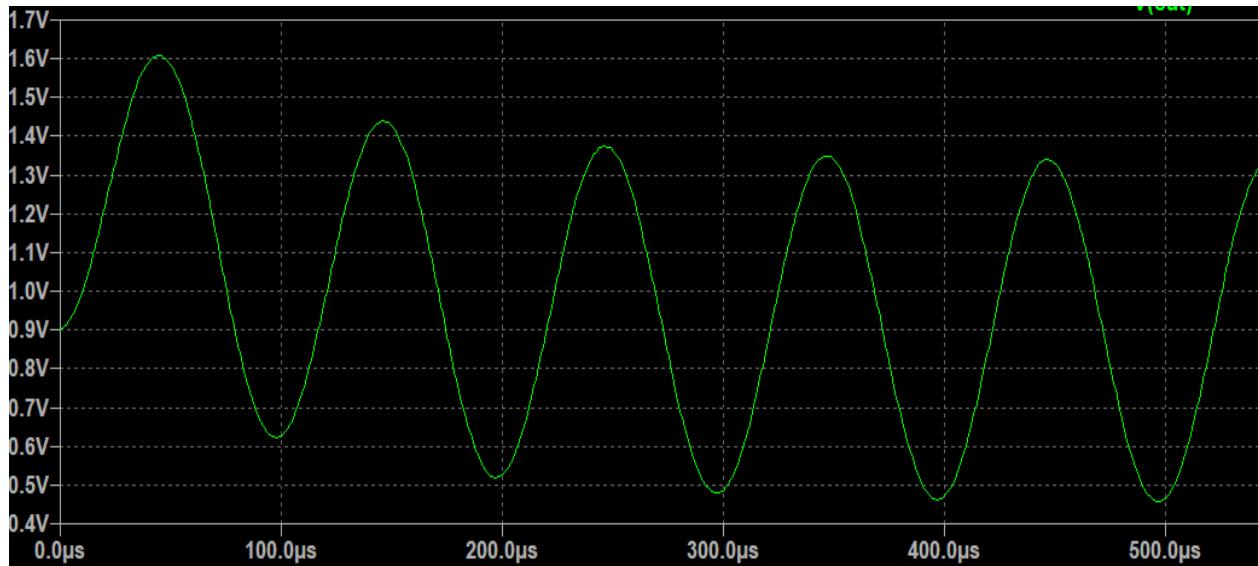
$$ICMR=1.5-.45=1.05\text{V}$$

3.I)3dB frequency



3dB frequency = 1.45KHz

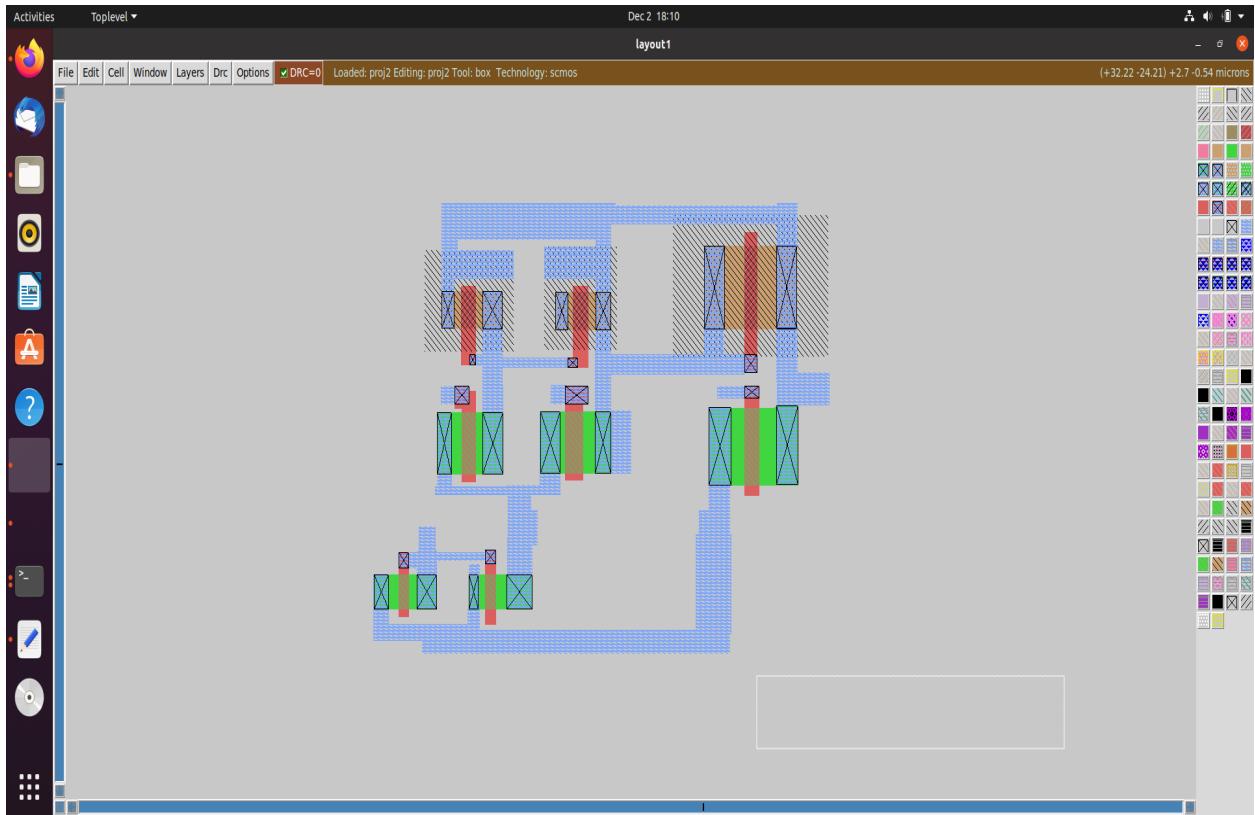
3.m)small signal transient analysis



Applied signal = 0.3 mV , 10KHz at
10.43% distortion

3.n) power taken = $V_{dd} \times$ current
current=216uA $V_{dd}=1.8V$
Power = 0.388mW

4.) Layout in magic tool



Parasitic capacitances extracted

```
proj2a - Notepad
File Edit Format View Help
* SPICE3 file created from proj2.ext - technology: scmos

.option scale=0.09u

M1000 a_n9_71# a_n9_71# a_n31_103# w_n50_83# pfet w=654 l=73
+ ad=982 pd=126 as=8114 ps=696
M1001 a_n31_103# a_110_n29# a_n36_n24# Gnd nfet w=1264 l=61
+ ad=4763 pd=398 as=4157 ps=464
M1002 a_n31_103# a_n9_71# a_99_101# w_86_84# pfet w=654 l=73
+ ad=0 pd=0 as=660 ps=106
M1003 a_n31_103# a_315_n43# a_n108_n141# Gnd nfet w=1264 l=61
+ ad=0 pd=0 as=4135 ps=428
M1004 a_n9_71# a_n16_33# a_n36_n24# Gnd nfet w=67 l=5
+ ad=1643 pd=168 as=0 ps=0
** SOURCE/DRAIN TIED
M1005 a_n31_103# a_n31_103# a_n31_103# w_233_78# pfet w=884 l=5
+ ad=0 pd=0 as=0 ps=0
M1006 a_n36_n24# a_n80_n148# a_n108_n141# Gnd nfet w=764 l=5
+ ad=0 pd=0 as=0 ps=0
M1007 a_n80_n148# a_n80_n148# a_n108_n141# Gnd nfet w=67 l=5
+ ad=928 pd=122 as=0 ps=0
C0 w_86_84# a_n9_71# 5.14fF
C1 a_110_n29# a_n36_n24# 0.6fF
C2 w_86_84# a_99_101# 0.6fF
C3 w_n50_83# a_n31_103# 8.33fF
C4 w_n50_83# a_n9_71# 7.47fF
C5 w_233_78# a_n31_103# 20.03fF
C6 w_86_84# a_n31_103# 9.68fF
C7 a_n80_n148# a_n108_n141# 1.32fF
C8 a_n80_n148# Gnd 10.82fF
C9 a_n108_n141# Gnd 51.52fF
C10 a_n36_n24# Gnd 14.78fF
C11 a_315_n43# Gnd 8.62fF
C12 a_110_n29# Gnd 11.02fF
C13 a_n16_33# Gnd 9.343fF
C14 a_n9_71# Gnd 10.58fF
C15 a_n31_103# Gnd 62.69fF
C16 w_233_78# Gnd 134.87fF
C17 w_86_84# Gnd 73.42fF
C18 w_n50_83# Gnd 87.83fF
```

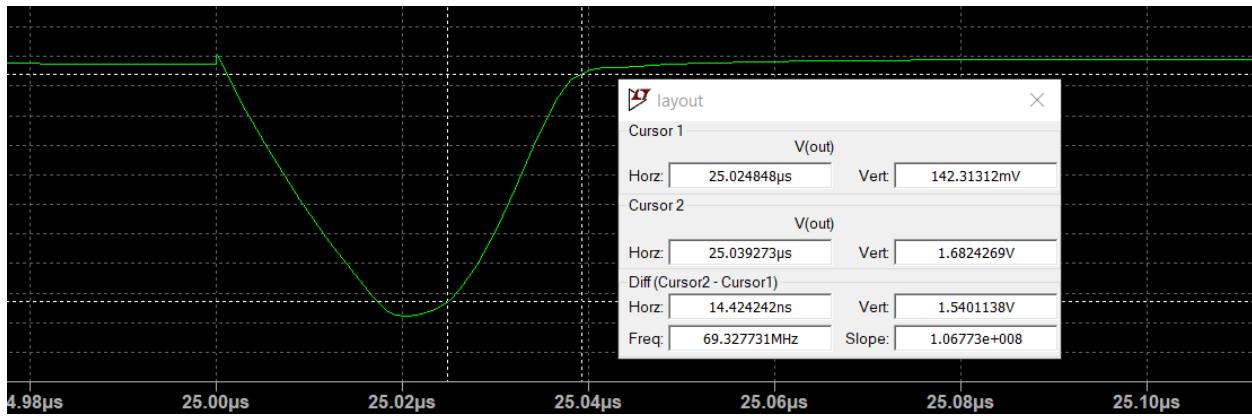
Simulations with parasitics

DC operating point , node voltages

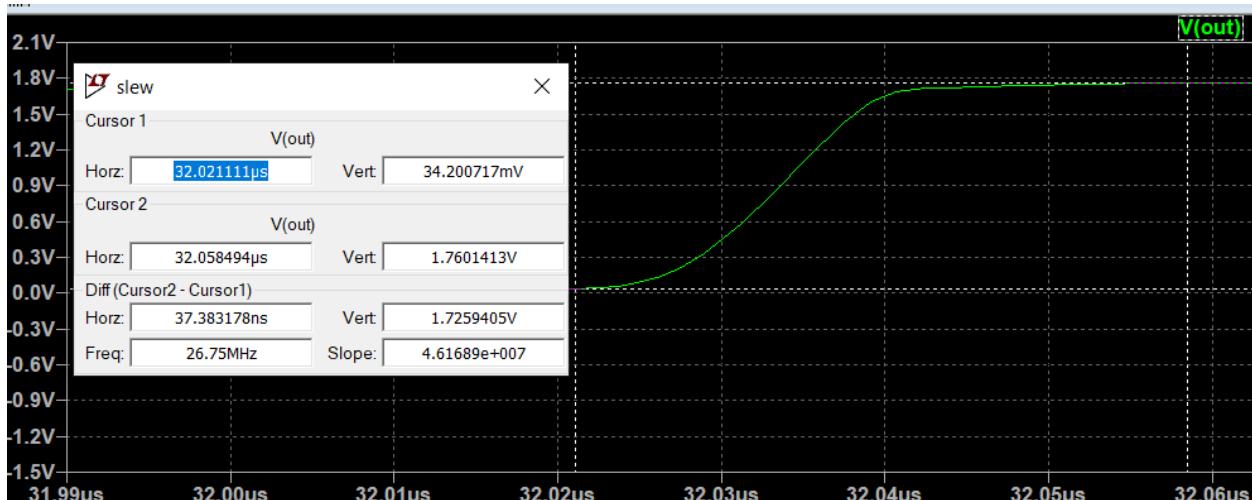
```
V(n003) :      1.21365    voltage
V(n004) :      0.89996    voltage
V(n006) :      0.361179   voltage
V(n002) :      1.19871    voltage
V(n005) :      0.9        voltage
V(n008) :      0.578206   voltage
V(out) :       0.89996    voltage
V(n001) :      1.8        voltage
V(n007) :      0.55       voltage
V(p001) :      1.19871    voltage
Id(M4) :      -9.61001e-006 device_current
Ig(M4) :       -0          device_current
Ib(M4) :       6.1129e-013 device_current
Is(M4) :       9.61001e-006 device_current
Id(M3) :      -9.60755e-006 device_current
Ig(M3) :       -0          device_current
Ib(M3) :       5.96353e-013 device_current
Is(M3) :       9.60755e-006 device_current
Id(M6) :      -0.000176825 device_current
Ig(M6) :       -0          device_current
Ib(M6) :       9.1004e-013 device_current
Is(M6) :       0.000176825 device_current
Id(M8) :       2e-005     device_current
Ig(M8) :       0           device_current
Ib(M8) :      -5.88206e-013 device_current
Is(M8) :      -2e-005     device_current
Id(M7) :       0.000176825 device_current
Ig(M7) :       0           device_current
Ib(M7) :      -9.6006e-013 device_current
```



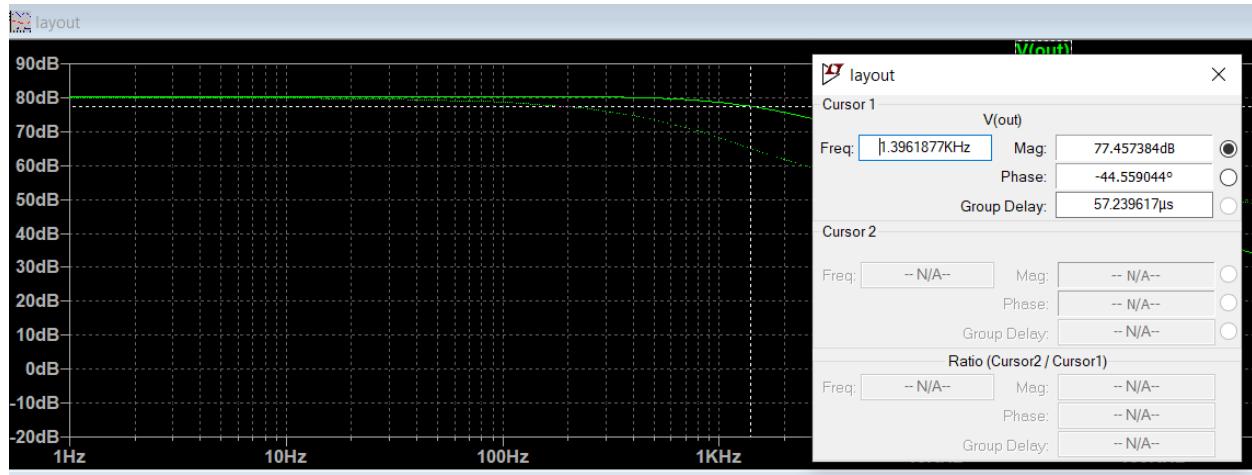
Gain=80.4dB, PM=64.3, UGB=10.79MHz



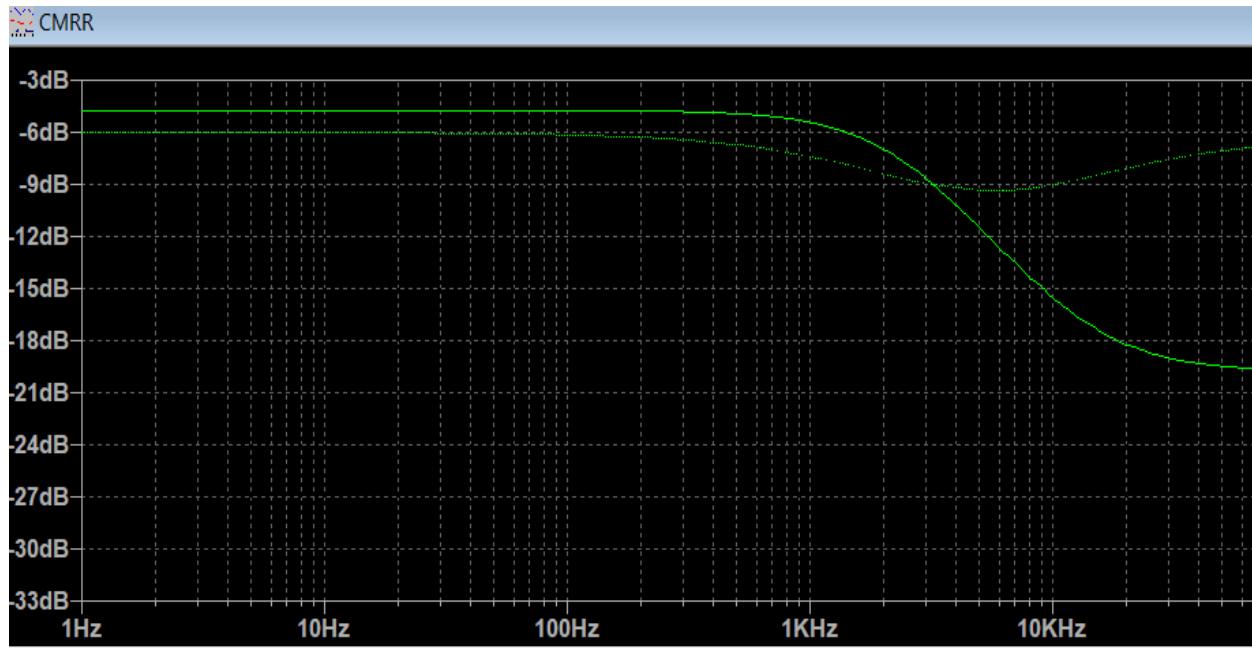
Slew rate = 106V/us



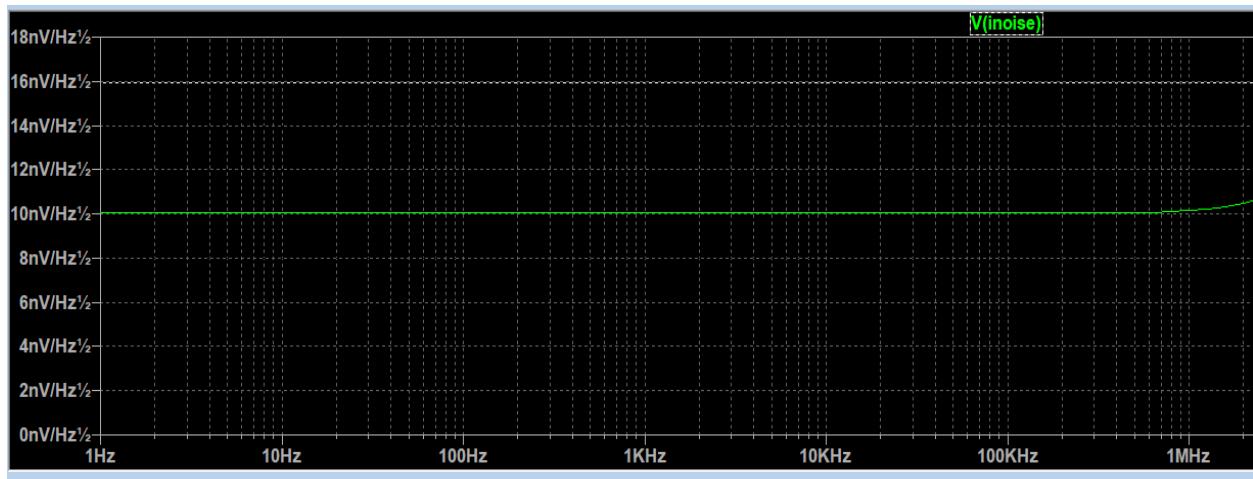
Settling time = 38ns



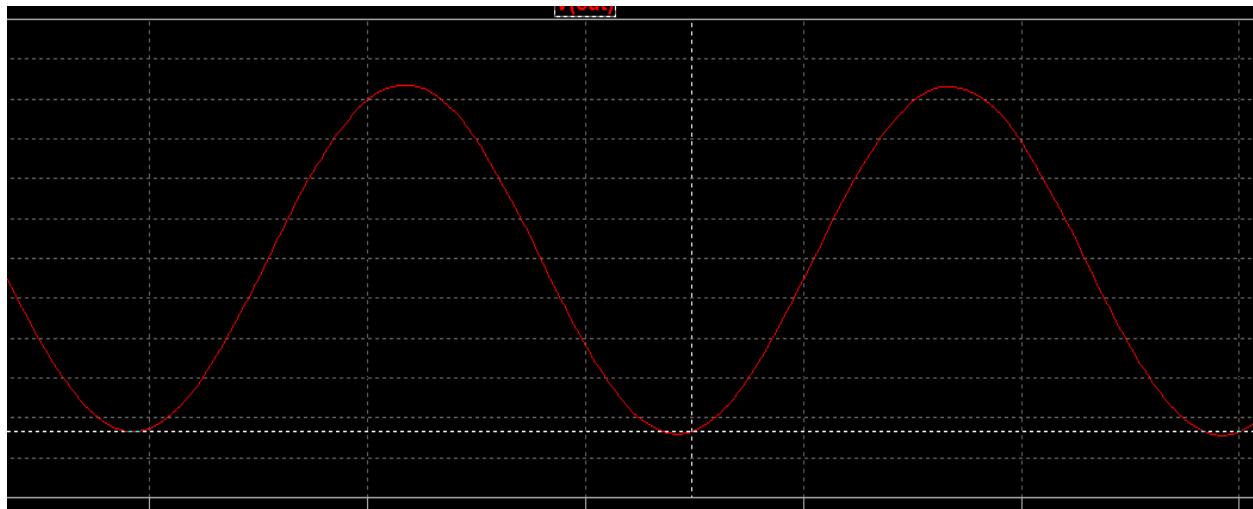
3db frequency=1.39KHz



$$\text{CMRR} = 80.4 + 4.7 = 85.1 \text{dB}$$



Noise = $9.82\text{nV}/\sqrt{\text{Hz}}$

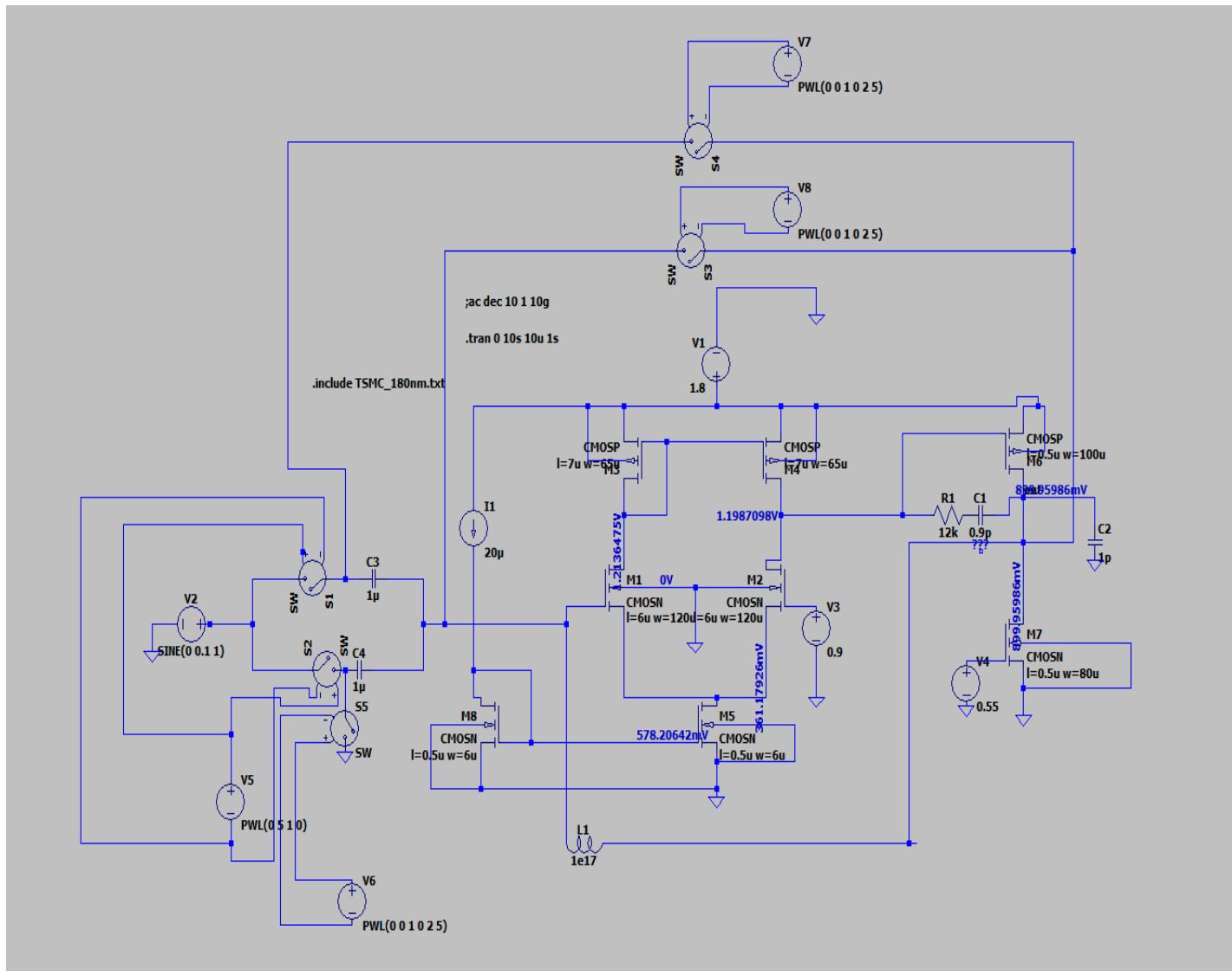


Applied signal = 0.3 mV , 10KHz at
10.97% distortion

Values	specification	Pre layout	Post layout
gain	80dB	80.4	80.4
Phase margin	65	67	64.3
Unity gain frequency	10MHz	11.25MHz	10.79MHz
3dB frequency	-	1.45KHz	1.39KHz
CMRR	-	85.2dB	85.1dB
noise	10nV	9.8nV	9.8nV
Slew rate	100V/usec	110V/usec	106V/usec
Settling time	-	32ns	38ns
Small signal	-	10.43% distortion at 0.3mV	10.97% distortion at 0.3mV
power	-	0.388mW	0.390mW

Since the layout result only involved parasitic capacitances and not resistances etc., there isn't any change observed in noise or gain performance of the amplifier.

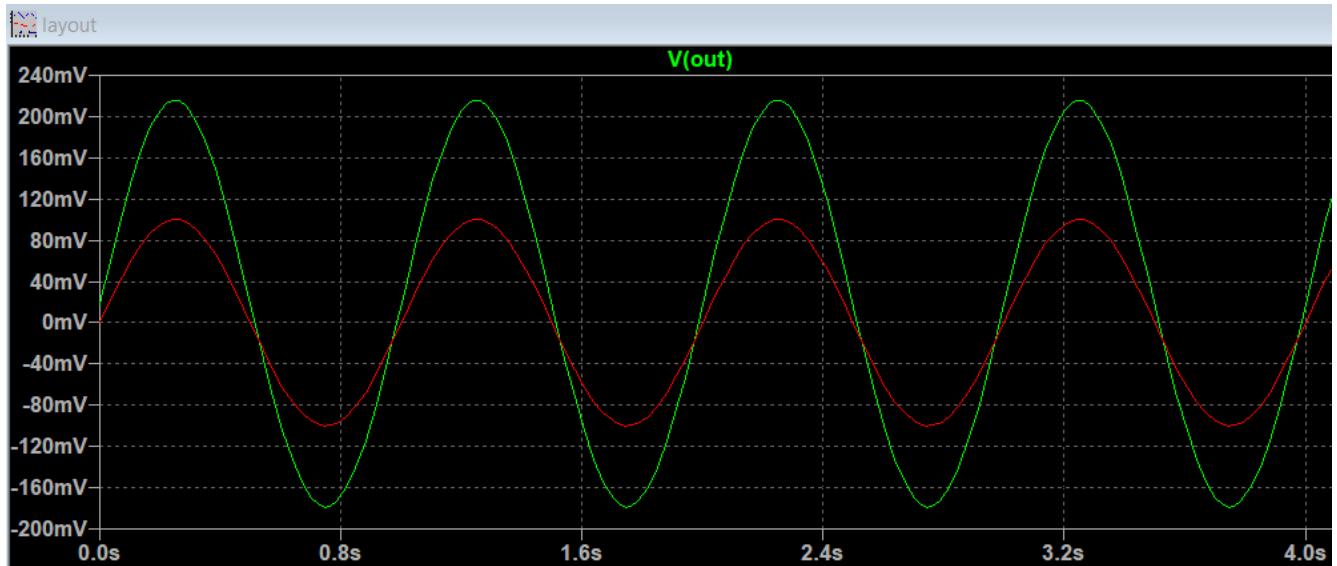
Multiply-by-two circuit



The Switch used in the schematic has the following parameters

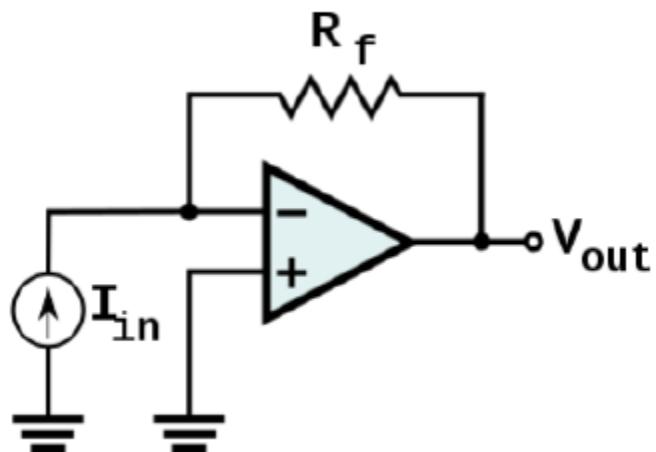
**.model MYSW SW(Ron=1 Roff=1Meg Vt=.5
Vh=-.4)**

Output of the circuit



Thus we can see the output is 1.94 times the input.

Transimpedance Amplifier



From the open loop of the opamp we know $V_o = A_o \cdot V_d$

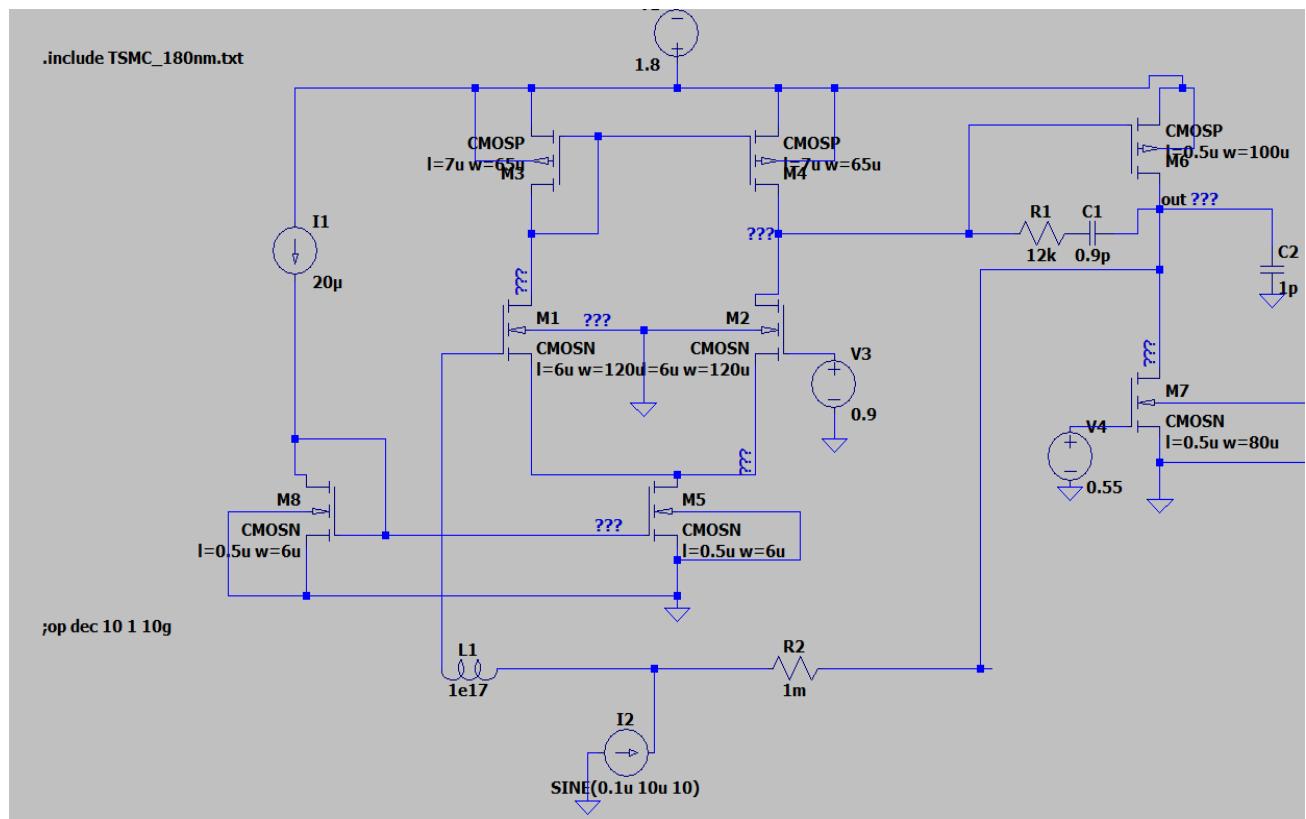
Applying KCL at the negative terminal of opamp,

$$-V_d = V_o - i_1 R_f = V_o / A_0$$

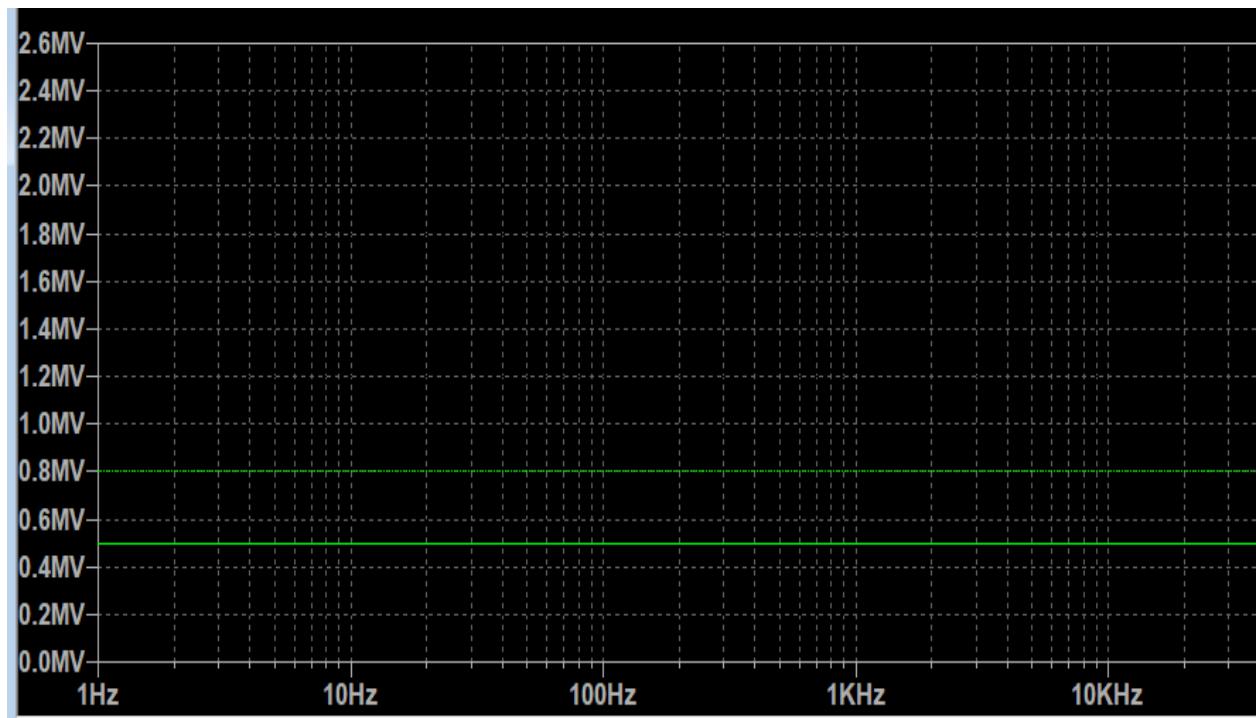
$$V_o / i_1 = R_f / (1 + 1/A_0)$$

Our A_0 is very large compared to 1 so $V_o / i_1 = R_f = 500k$

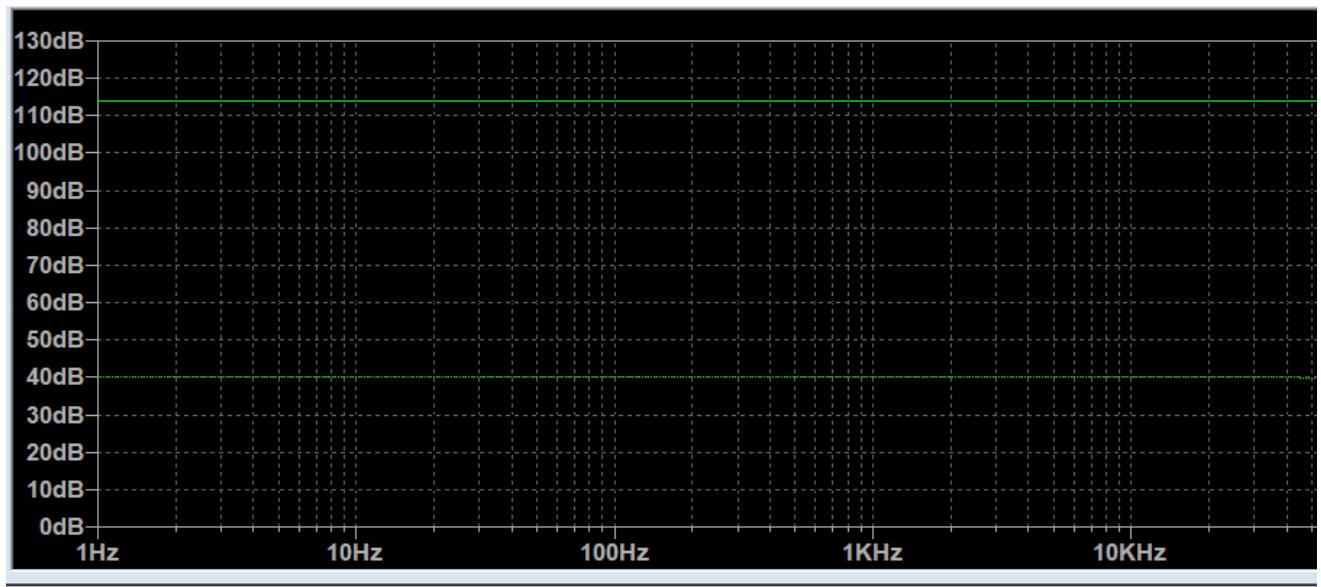
(according to the question)



With input current of $0.4\mu\text{A}$ the output is shown below , the voltage swing is approximately 0.2V , Thus the TIA is providing a gain of 500k ohm .



500k gain on doing AC sweep of the TIA



500K gain in dB