AIC Project

1 Design specifications

Design a differential input, single ended output operational transimpedance amplifier (OTA) with the lowest possible power consumption for the following specifications :

- DC gain \geq 80dB.
- Unity gain frequency ≥ 10 MHz.
- Output voltage swing $\geq 1V_{pp}$.
- Slew rate $> 250 \text{V}/\mu\text{s}$.
- Phase Margin $\geq 65^{\circ}$.
- Input referred noise (Thermal only) = $10\text{nv}/\sqrt{Hz}$.
- Input Common mode voltage = 0.9V.
- Output load capacitance = 1pF.

Topology:

Since we were required a gain of 80 dB and the design also asks for low power consumption so I went to choose the telescopic configuration as the gain is maximum in this also since folded-cascode requires an extra biasing so it consumes more power as compared to telescopic and furthermore the gain is also less than telescopic so I choose the Telescopic configuration.

Notice how my topology (fig1) is slightly different from conventional telescopic as this offers more swing than the traditional telescopic configuration in which the PMOS are connected in diode connected fashion.

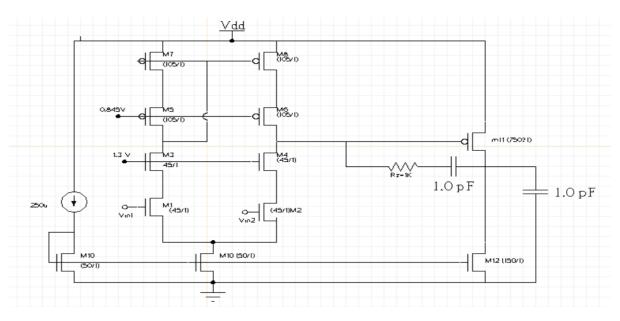


Figure 1

Mosfet	Hand Calculations(W/L)	Actuals Used (W/L)	
M1	41	45	Ln=0.18um
M2	41	45	Ln=0.18um
M3	41	45	Ln=0.18um
M4	41	45	Ln=0.18um
M5	120	105	Lp=0.36um
M6	120	105	Lp=0.36um
M7	120	105	Lp=0.36um
M8	120	105	Lp=0.36um
M9	45	50	Ln=0.18um
M10	45	50	Ln=0.18um
M11	800	750	Lp=0.36um
M12	150	150	Ln=0.18um

Table -1

(The length of P channel I increased as lambda is inversely to length so in order to make both rds of NMOS and PMOS equal to increase the Overall Gain)

Hand Calculations:

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CC = 0.8 pc

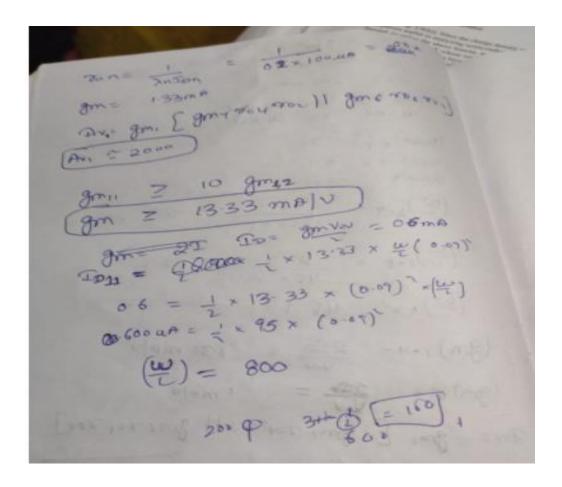
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To = 200 MA

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H-HH and identical

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Hand Calculations Resuts:

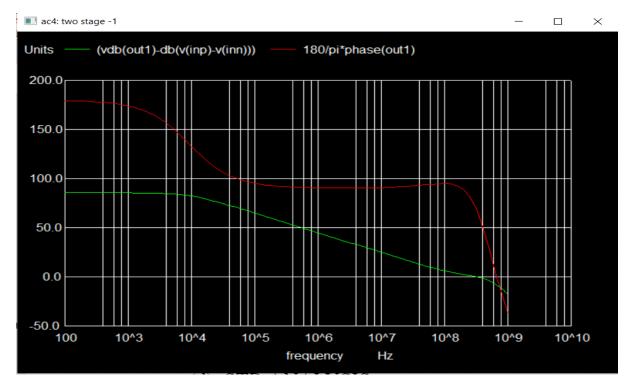
Gain	15000V/V
UGB	1.6Ghz
PM	75
Cc	0.8pF

DC operating Points:

DC operating Points:		
Initial Transient Solution		
Initial Transient Solution Node vdd d1 inp p d2 inn x vb3 out vb5 d7 d8 y h	Voltage 1.8 0.549283 0.900006 0.21492 0.549387 0.9 1.17005 1.3 1.17452 0.845 1.54699 1.54707 0.691377 0.900006	
v3#branch v5#branch vdd#branch	0 0 0 -0.00120986	

3) Simulations:

DC gain and Phase Plot: From AC Analysis

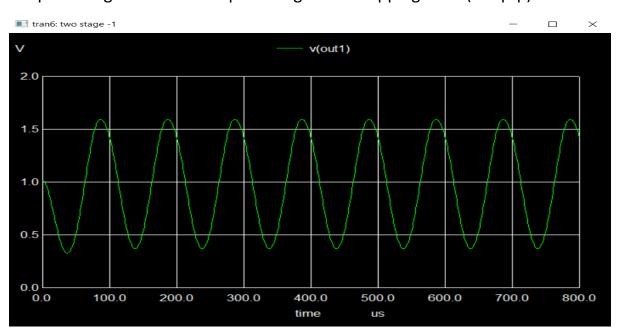


DC gain: 84.2 dB

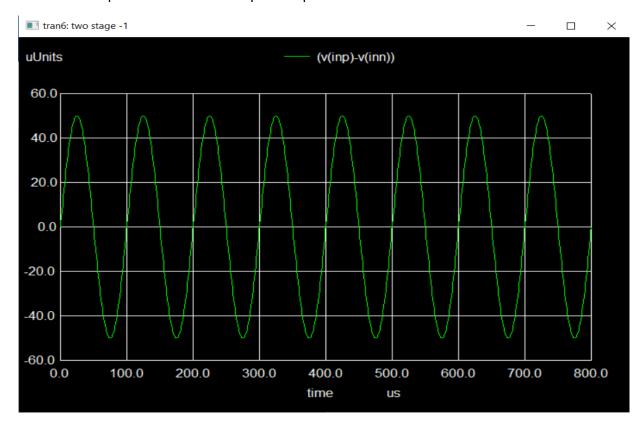
Phase Margin: 71.2 degrees

Unity Gain frequency: 3.01*10^8 Hz

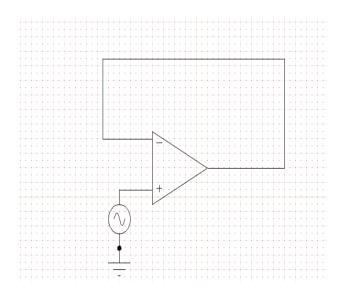
Output Swing: Maximum output swing before clipping 1.23v(>1Vp-p)



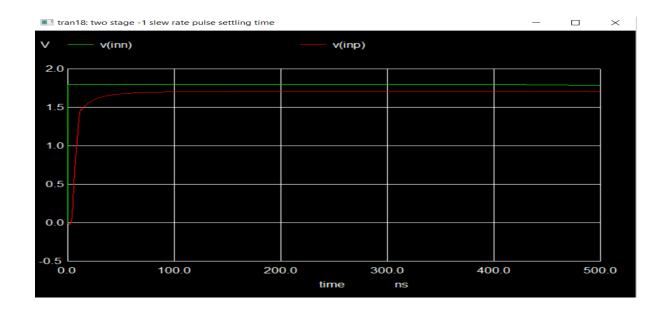
Differential Input of 100micro volts peak to peak.



Slew Rate : We applied a step input of 1.8 V and will check the O/p voltage at other node .

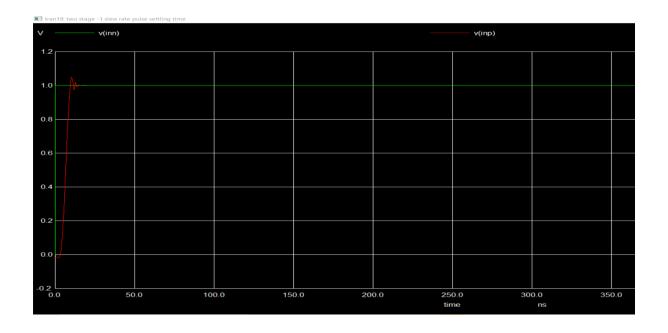


We will now find the maximum Slope by Output voltage for calculation of Slew Rate. SR=230V/us from the below simulations.

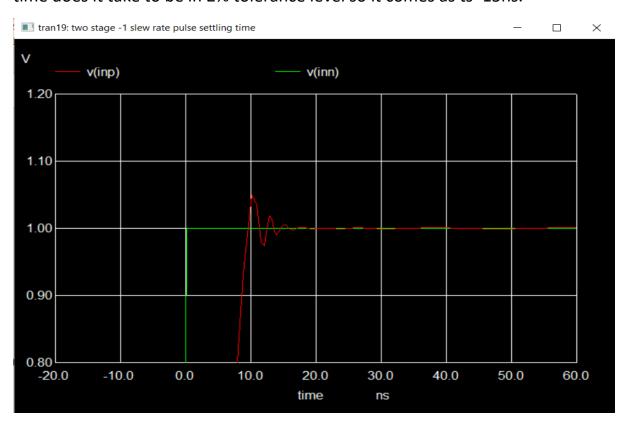


Settling Time: This is due to effect of Phase Margin the more the Phase Margin the less will be the overshoots since my PM is around 71degrees so it has very low peaks.

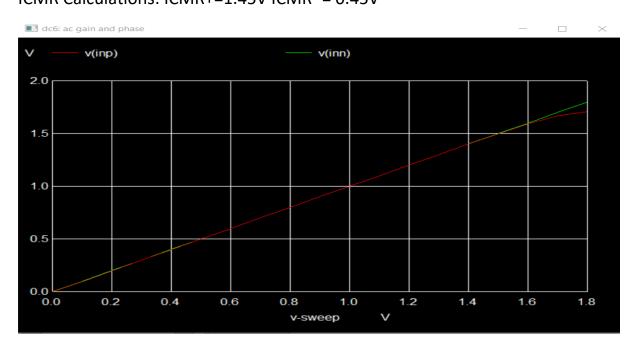
This time instead of applying 1.8V pulse I have applied a 1V peak to see the ringing in my circuit .



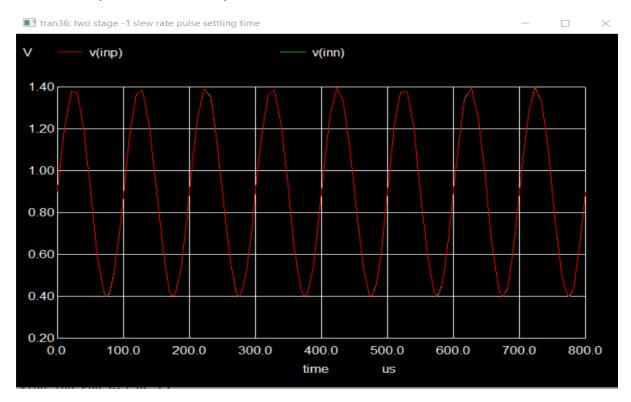
For calculation of settling time we will zoom our previous result to check what time does it take to be in 2% tolerance level so it comes as ts=15ns.



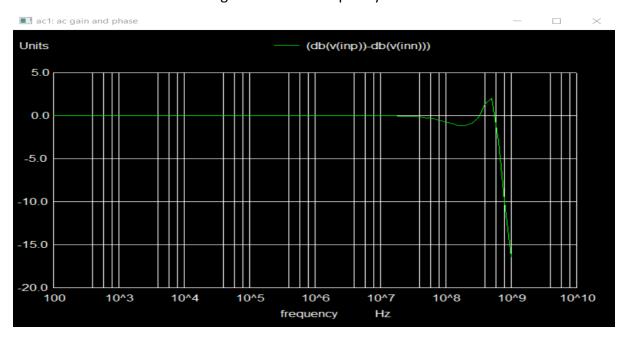
ICMR Calculations: ICMR+=1.45V ICMR- = 0.45V



Closed Loop Transient Analysis:



Closed Loop Gain: We used OTA in negative feedback configuration and performed AC simulation for calculation of DC gain and -3db Frequency.



Av=1 which means 0db which was expected.

F-3db= 0.63Ghz

Power Consumption: Total Current from the Vdd supply including the biasing circuitry is 1.2mA.

P_{total}=Vdd*I(from Vdd)=1.8*1.2=2.16mW.

Conclusions

Requirements	Results from Simulations
DC Gain>80dB	84.2dB
UGB>10Mhz	3*10 ⁸ hz
Output Voltage Swing>1Vp-p	1.23V p-p
Slew Rate>=250V/us	230V/us
Phase Margin>65degree	71.2
Input Referred Noise	-
Output Capacitance=1pf	1pf
ICMR ⁺	1.45V