Department Electronics & Communication Engineering

Analog Electronic Circuits

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AEC Project

Team No. – 10

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Objectives:

To analyse Ring Oscillator circuit and find delay and frequency of Oscillation .

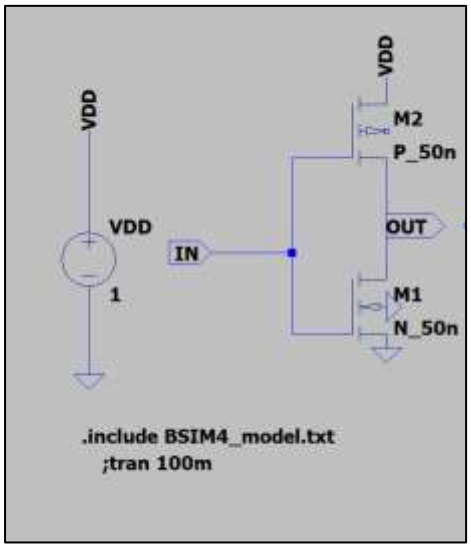
Components Used:

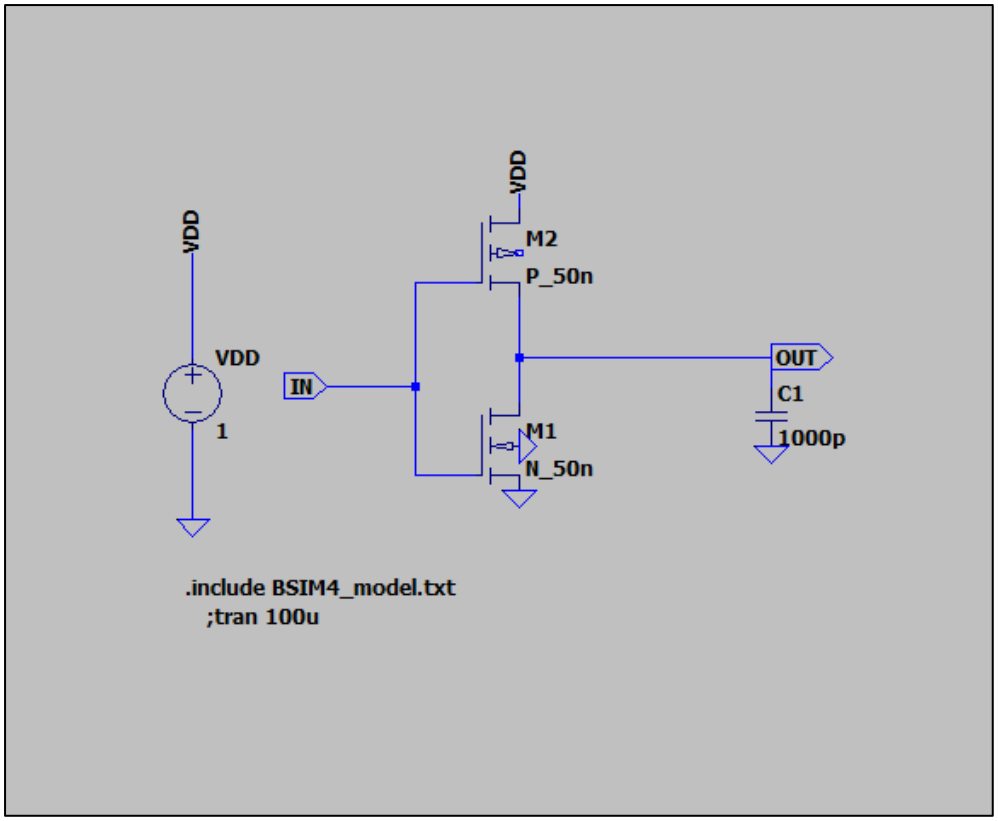
1. Nmos
2. Pmos
3. Capacitor
4. Voltage Source
5. Pulse Generator

Background of the circuit:

1. CMOS Inverter

The circuit required designing a NOT gate circuit as shown below





This circuit consists of a PMOS transistor that connects to the source and an nMOS transistor that connects to the ground.

Let's imagine the input is a 0.

The 0 comes in and goes both up and down the wire to both the pMOS (top) and the nMOS (bottom). When the value 0 reaches the pMOS, it gets inverted to a 1; so, the connection to the source is closed. This will produce a logical value of 1 so long as the connection to the ground (drain) is not also closed. Well, since the transistors are complementary, we know that the nMOS transistor won't invert the value; so, it takes the value 0 as is and will — therefore — create an open circuit to the ground (drain). Thus, a logical value of 1 is produced for the gate.

IN	OUT
0	1

An IN value of 0 produces an OUT value of 1

An IN value of 0 produces an OUT value of 1

What happens if a 1 is the IN value? Well, following the same steps as above, the value 1 gets sent to both the pMOS and the nMOS. When the value is received by the pMOS, the value gets inverted to a 0; thus, the connection to the SOURCE is open. When the value is received by the nMOS, the value does not get inverted; thus, the value remains a 1. When a value of 1 is received by the nMOS, the connection is closed; so, the connection to the ground is closed. This will produce a logical value of 0.

IN	OUT
1	0

An IN value of 1 produces an OUT value of 0.

An IN value of 1 produces an OUT value of 0.

Putting the two sets of input/output together yields:

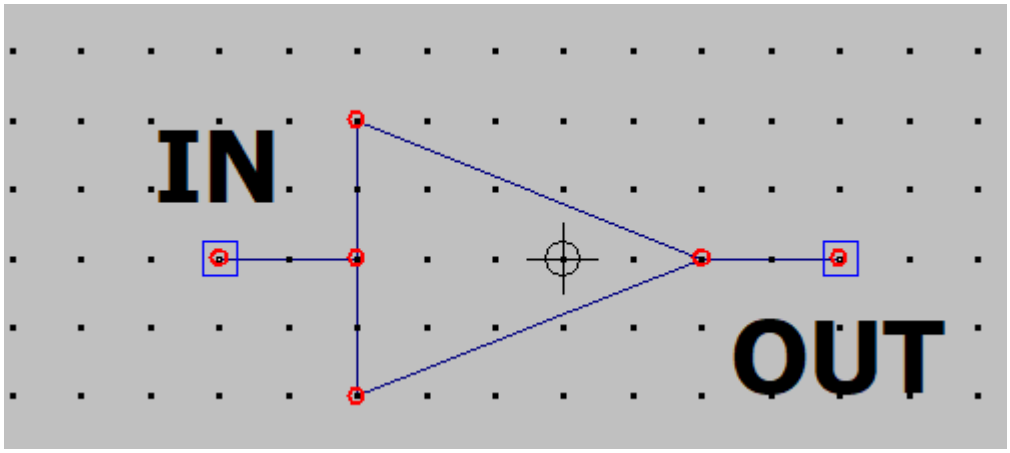
IN	OUT
0	1
1	0

The Truth Table for a NOT gate.

Note - The RC circuit is added in order to factor in delay

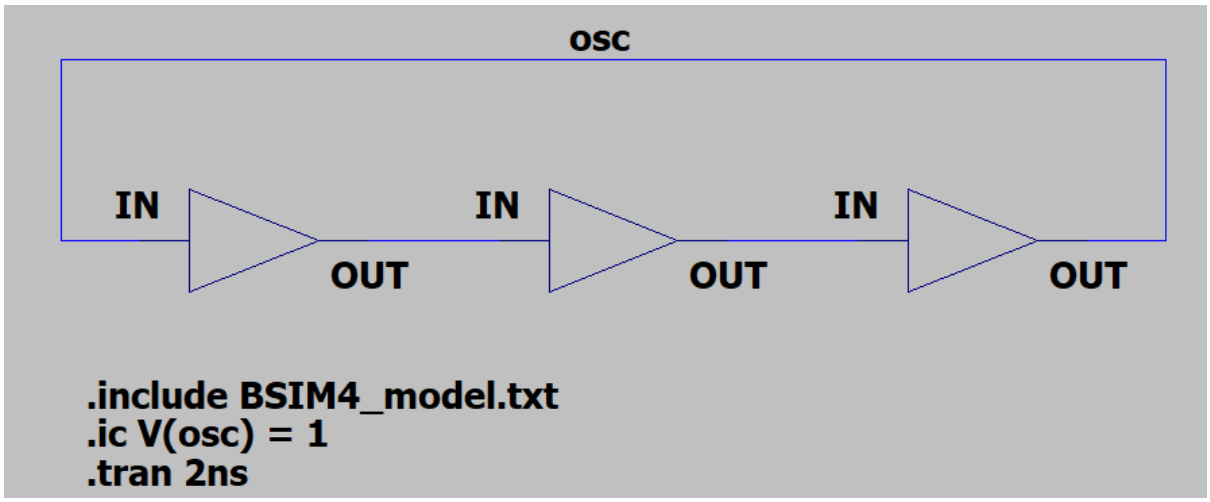
2. NOT Symbol:

To simplify the circuit visually, we stored the NOT gate circuit above as the following symbol:



3. Main Circuit:

Following is the circuit of the ring oscillator:



The input is sent through an odd number of CMOS inverters and the output from the last CMOS inverter is inputted back into the first CMOS inverter. This causes the input to keep oscillating between 1 and 0 as the output from the last CMOS inverter will always be an inversion of the input to the first CMOS inverter.

Calculations:

Parameters from technology file and LT-Spice:

Technology	Drawn	Actual Size	$R_{n,p}$	$C_{ox,n,p}$
NMOS(long-channel)	10/1	10µm by 1µm	1.5k	17.5 fF
PMOS(long-channel)	30/1	30µm by 1µm	1.5k	52.5 fF
NMOS(short-channel)	10/1	0.5µm by 50 nm	3.4k	625 aF
PMOS(short-channel)	20/1	1µm by 50 nm	3.4k	1.25 fF

$C_{oxn} = 0.625 \text{ X } 10^{-15} \text{ F/m}^2$

$C_{oxp} = 1.25 \text{ X } 10^{-15} \text{ F/m}^2$

$W_N = 0.5\mu m$

$W_P = 1\mu m$

$L_N = 50nm$

$L_P = 50nm$

$R_{IN} = 3.4k\Omega$

$Cinv = (5/2)(C_{oxn} + C_{oxp}) = 4.7fF$

$Cout = 1nF$

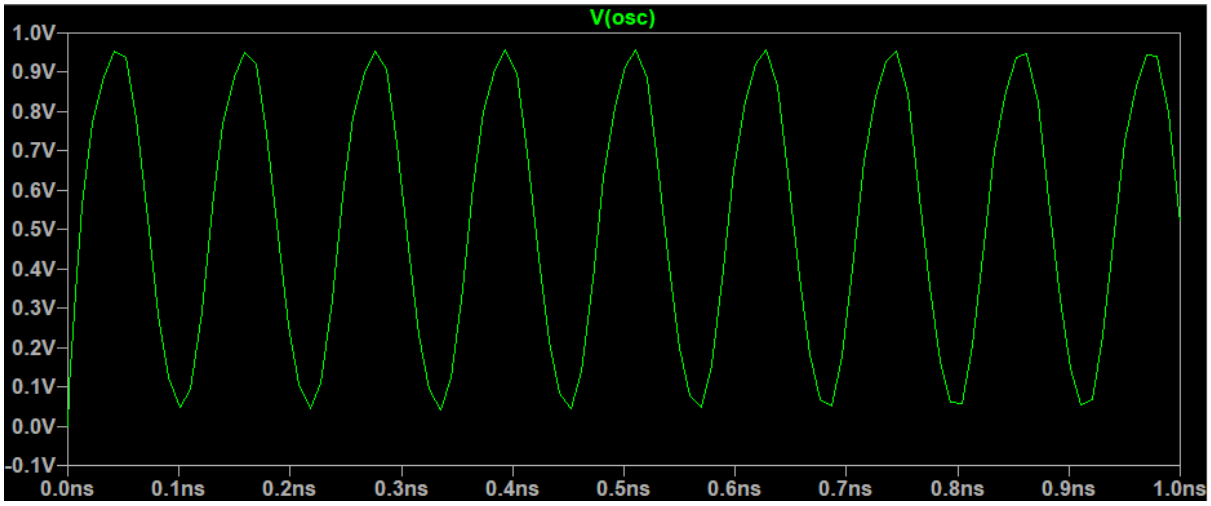
$\tau_{pHL} = \tau_{pLH} = 0.7 \text{ x (Rin) Cout}$

$\tau_{inv} = \tau_{pHL} + \tau_{pLH} = 0.7 \text{ x } (3.4k + 3.4k)(4.7) = 22ps$

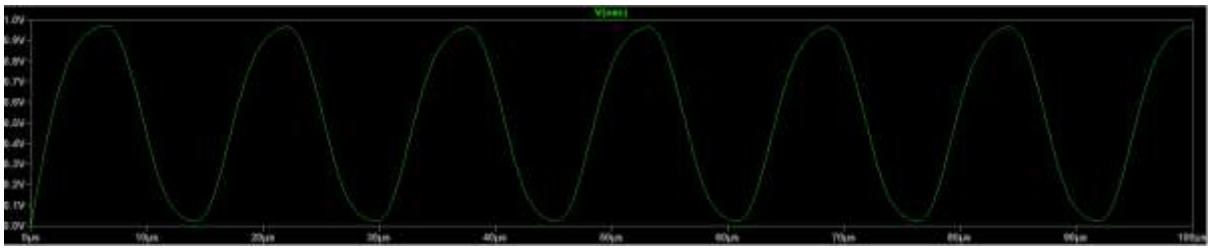
$\tau_{Delay} = \tau_{inv} \text{ x } \frac{Cout}{Cinv} = 22ps \text{ x } (1nF/4.7fF) = 4.68\mu s$

Plots:

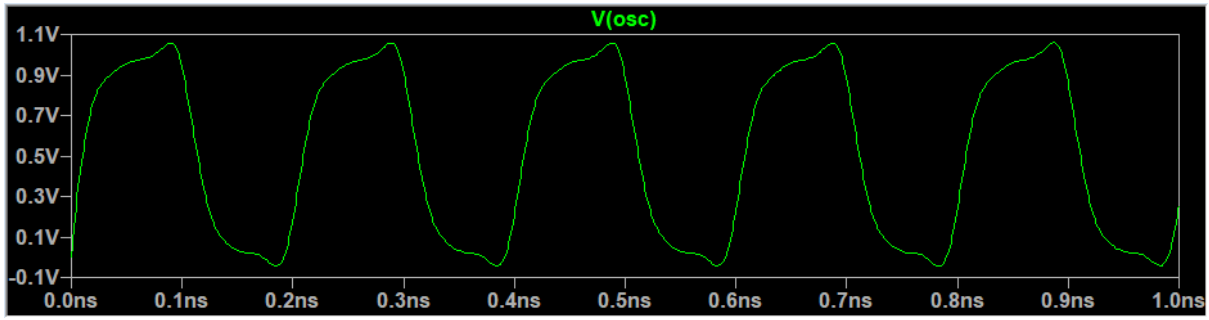
3 Not Gates:

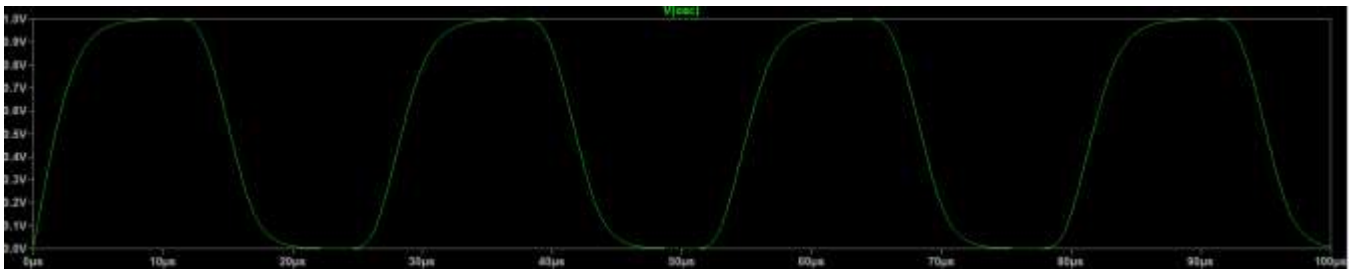


With Capacitance to increase Delay



5 Not Gates:





Comparison between Simulation and Theory:

3 Not Gate	Without C_L	With C_L
Simulation	102.69078ps	13.799875µs

Theory	66ps	14.042μs

5 Not Gate	Without C_L	With C_L
Simulation	178.81562ps	22.686594μs
Theory	110ps	23.404μs

Applications:

1. Oscillatory behaviour is ubiquitous in all physical systems, especially in electronic and optical. In radio frequency and light wave communication systems, oscillators are used for frequency translation of information signals and channel selection
2. Oscillators are also present in all digital electronic systems, which require a time reference, i.e., a clock signal, to synchronise operations.
3. The voltage-controlled oscillator in most phase-locked loops is built from a ring oscillator. The wide voltage tuning range of ring oscillators makes it attractive for Phase-locked-loop based frequency synthesis
4. The temperature of a chip can be measured using the dependence of the delay property of a ring oscillator on temperature. Oscillation frequency also exhibits a linear dependence on junction temperature.
5. A hardware random number generator (HRNG) or true random number generator (TRNG) is a device that generates random numbers from a physical process, rather than by means of an algorithm. The jitters from a ring oscillator can be used as the physical component to generate random numbers.

6. For data recovery purposes in serial data communications, these oscillators are useful.
7. During wafer testing, ring oscillators are used. For example - wafer-lvel TSV connectivity test