Vikhyath Lukka

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SUMMARY

- Detail-oriented and results-driven Electrical Engineer graduate with a Master's degree from San Jose State University.
- Specialized in Digital Design and Verification, with a robust foundation in ASIC and FPGA Design and Verification.
- Adept at implementing complex projects in FPGA and ASIC, showcasing a keen understanding of computer architecture, digital design, and verification concepts.

EDUCATION

Master of Science in Electrical Engineering May 2024

San Jose State University, San Jose, CA

- Related course work: Digital System Design and Synthesis, Advanced Computer Architecture, ASIC CMOS Design, Embedded SoC Design, SoC Design and Verification with System Verilog, Digital Design for AI and DSP.

Bachelor of Technology in Electronics and Communication Engineering Jul 2021

Sreenidhi Institute of Science and Technology, Hyderabad, India

- Related course work: C Programming, Programmable logic devices, Structured digital system design, VLSI technology and design, FPGA architecture and applications, Digital design through Verilog.

TECHNICAL SKILLS

- HDL: Verilog, System Verilog, UVM.
- Programming Languages: C, Python, MATLAB.
- Protocols: APB, AHB, UART, SPI, I2C, AXI, PCI, PCIe.
- Logic Simulation Tools: Synopsys VCS, Design Vision, Synopsys Primetime, Vivado, Vivado HLS, ModelSim, Keil.
- Digital Design Concepts: FSM Design, RTL Design, Logic Synthesis, Static timing analysis (STA), Pipelining.
- Operating System and Tools: Windows, Linux, Microsoft Office, and Adobe Suite.

PROJECT EXPERIENCE

Inference Engine Based on Logarithmic-Based Arithmetic, Digital Design for AI and DSP Oct 2023 - Dec 2023

- Developed a Logarithmic-Based Inference Accelerator for NN with a unique (1,4,3) logarithmic representation.
- Executed functions for conversion between floating-point and logarithmic representations, arithmetic operations, and integrated NN layers with ReLU activation function.
- Proposed Logarithmic representation decreased hardware requirements by 40% compared to int8 representation, leading to a significant boost in clock speed.

Programmable I/O Controller for RP2040 Microcontroller, SoC Design and Verification with SV Aug 2023 - Oct 2023

- Devised a PIO controller in System Verilog, it has 9 instructions controlled by a state machine has 4 states.
- Constructed PIO controller efficiently manages control, status, and data handling through FIFOs, shift registers, clock dividers, and specialized registers. The project demonstrates proficiency in digital design and System Verilog programming.

SoC Design with Cortex-M0 Microprocessor for Snake Game, Embedded SoC Design May 2023 - Jul 2023

- Devised and applied a versatile System-on-Chip platform on Xilinx Artix-7 100T FPGA for Snake game.
- Featured a Cortex-M0 microprocessor and utilized AMBA-AHB Lite protocol for communication.
- Created peripherals (VGA display, 7-segment display, UART communication, GPIO) in Verilog using Vivado.
- Employed Keil software for assembly and C coding to generate hex file for use in Vivado to create a bitstream.
- Integrated AHB-Lite Bus protocol, AHB VGA, and AHB UART for efficient development of versatile embedded applications.

FIR Filter, ASIC CMOS Design Mar 2023 - May 2023

- Built a 29-tap FIR filter with a clock frequency of 300MHz, limited to 5 complex multipliers, and a filter operation performed in no more than 3 clock cycles.
- Displayed expertise in design optimization, pipelining, logic synthesis and RTL Design.

FP MAC with SRAM and Synchronous FIFO, Digital System Design and Synthesis Nov 2022 - Dec 2022

- Built a floating point multiply accumulator with synchronous FIFO employing Verilog on Nexys A7 100T FPGA board.

Cache Simulator, Advanced Computer Architecture Oct 2022 - Nov 2022

5 Stage Pipelined MIPS Architecture with forward chaining, Advanced Computer Architecture Aug 2022 - Sept 2022

CAREER PROGRESSION

RTL Design and Verification Trainee, LUCID VLSI, India Dec 2021 - Apr 2022

- Constructed SystemVerilog Verification Environments for Router 1x1 DUT, Synchronous Memory model.
- Designed and implemented 3 key components: Transaction classes, Generators, Drivers, and Monitors.
- Established In-Order scoreboards and Functional Coverage components for accurate and comprehensive verification.
- Formulated and executed Test Plans, applying factory concepts for flexible transaction overrides.