



## Tutorial #2

### Hilary Term Weeks 4 and 5

### LDM, STM, Stacks and Subroutines

Work in groups of 6 students using one of the whiteboards.  
Complete the exercises in your own time if necessary.  
Revise the exercises to prepare for the next lab.

## 1 Stacks

### 1.1 Stack Operations with LDR/STR

- (a) Provide an ARM Assembly Language program that will push the contents of R4, R5 and R6 on to the system stack. You may not use the LDM or STM instructions.
- (b) Illustrate the state of the stack after each push operation above.
- (c) Provide an ARM Assembly Language program that will pop the three topmost words off the top of the stack, restoring their values into the registers from which they were originally stored in part (a) above. You may not use the LDM or STM instructions.
- (d) Illustrate the state of the stack after each push operation above.

### 1.2 Stack Operations with LDM/STM

- (a) Provide an ARM Assembly Language program that will push the contents of R4, R5 and R6 on to the system stack. You must use the LDM and STM instructions.
- (b) Provide an ARM Assembly Language program that will pop the three topmost words off the top of the stack, restoring their values into the registers from which they were originally stored in part (a) above. You must use the LDM or STM instructions.

## 2 Understanding LDM and STM

Provide diagrams to illustrate the state of the stack (stack pointer and contents) after executing each of the following instructions and list the contents of any registers modified by the operation. Begin by assuming some initial values stored in each register.

1	STMFD	SP!, {R4, R6, R8–R11}	
2	LDMFD	SP, {R10, R11}	; Note – no ! in this instruction
3	LDMFD	SP!, {R8, R10, R11, R4, R6}	



### 3 Other uses of LDM/STM

Write an ARM Assembly Language program to copy 512 bytes of memory from the address in R0 to the address in R1. Take advantage of the LDM and STM instructions to load and store multiple words using a single instruction.

Calculate the number of memory accesses required by your program and compare it with the number of memory accesses required if using only LDR and STR instructions.

### 4 Subroutines

#### 4.1 Subroutine Interfaces

- (a) For each of the following Java/C-like method declarations, design an appropriate ARM Assembly Language interface for a corresponding assembly language subroutine. The interface must include a specification of how each parameter is passed into the subroutine and how any return values are passed back to the calling program.

(i) `void zeroMemory(unsigned int startAddress, unsigned int length)`  
(*zero a range of addresses in memory*)

(ii) `int factorial(unsigned int x)`

(iii) `int power(int x, unsigned int y)`

(iv) `int quadratic(int a, int b, int c, int x)`  
(*evaluate a quadratic function*)

- (b) For each of the subroutines listed above, show how you would invoke (call) the subroutine, assuming the variables to be passed as parameters are initially stored in registers other than R0–R3.

#### 4.2 Subroutine Implementations

Implement each of the subroutines listed in Section 4.1, taking care to hide any unintended side-effects from a calling program using LDM and STM instructions to save and restore registers on the system stack. Your subroutines should adhere to the interfaces that you defined above. Try to use registers R0–R3 to pass parameters and R4–R12 to store variables that are local to the subroutine.

**Complete the exercises in your own time if necessary!**



## CS1022 Tutorial #2 SOLUTION

### Hilary Term Weeks 4 and 5

### LDM, STM, Stacks and Subroutines

## 1 Stacks

### 1.1 Stack Operations with LDR and STR

(a)

1	STR	R4, [SP, #-4]!
2	STR	R5, [SP, #-4]!
3	STR	R6, [SP, #-4]!

(b) Diagram of memory showing stack state after above operations

(c) (Note the order – reverse of above)

1	LDR	R6, [SP], #4
2	LDR	R5, [SP], #4
3	LDR	R4, [SP], #4

(d) Diagram of memory showing stack state after above operations

### 1.2 Stack Operations with LDM and STM

(a)

1	STMFD SP!, {R4–R6}
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(b) Note, the LDM instruction takes care of the order of registers for us. The rule is the lowest numbered register is always loaded/stored from/to the lowest address. So, the order of registers in the list doesn't matter in either LDM or STM!

1	LDMFD SP!, {R4–R6}
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### 1.3 Understanding LDM and STM

1 STMFD SP!, R4, R6, R8–R11

Diagram of memory showing stack state after above operation

2 LDMFD SP, R10, R11

Note – no !

Diagram of memory showing stack state after above operation



3 LDMFD SP!, R8, R10, R11, R4, R6

Note – order doesn't matter, we will still reverse the PUSH performed by the first instruction!!

Diagram of memory showing stack state after above operation

## 1.4 Other uses of LDM/STM

We will copy memory in 64 blocks of 8 words, using 8 registers to load and then store each block, thereby reducing the number of instruction executions required. We will assume that the memory regions are non-overlapping.

```

1 Nbytes EQU 512 ; number of elements
2
3 AREA globals, DATA, READWRITE
4
5 ; N word-size values
6 dest SPACE Nbytes ; copy destination
7
8
9 AREA RESET, CODE, READONLY
10 ENTRY
11
12 LDR R1, =src ;
13 LDR R2, =dest ;
14
15 MOV R0, #0 ; count = 0
16 wh1 CMP R0, #Nbytes >> 3 ; while (count < Nbytes / 8 registers) {
17 BHS eWh1 ;
18
19 ; we can increment the src and destination address registers
20 ; explicitly using ADD instructions ...
21
22 ; LDMIA R1, {R5-R12} ; load 8 words into R5-R12
23 ; STMIA R2, {R5-R12} ; store 8 words from R5-R12
24 ; ADD R1, R1, #8*4 ; advance src by 8 words
25 ; ADD R2, R2, #8*4 ; advance dst by 8 words
26
27 ; ... or implicitly using ! to advance (increment) the pointer
28
29 LDMIA R1!, {R5-R12} ; load 8 words into R5-R12
30 STMIA R2!, {R5-R12} ; store 8 words from R5-R12
31
32 ADD R0, R0, #1 ; count++
33
34 B wh1 ; }
35 eWh1
36
37 STOP B STOP
38
39 src DCD 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
40 DCD 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
41
42 ; ... 512 bytes in total ...
43
44 DCD 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
45 DCD 1,2,3,4,5,6,7,8,9,10,11,12,13,14,15
46
47 END

```



## 2 Subroutines

### 2.1 Subroutine Interfaces

#### (a) (i) zeroMemory

```
1 ; zeroMemory — zero a range of addresses in memory
2 ; Parameters:
3 ;   R0: start address of range to zero
4 ;   R1: length number of bytes to zero (unsigned word)
```

#### (ii) factorial

```
1 ; factorial — compute x!
2 ; Parameters:
3 ;   R0: x (unsigned word)
4 ; Return value:
5 ;   R0: x!
```

#### (iii) power

```
1 ; power — compute x^y
2 ; Parameters:
3 ;   R0: x (signed word)
4 ;   R1: y (unsigned word)
5 ; Return value:
6 ;   R0: x^y
```

#### (iv) quadratic

```
1 ; quadratic — evaluate a quadratic function of the form  $f(x) = ax^2 + bx + c$ 
2 ; Parameters:
3 ;   R0: a (signed word)
4 ;   R1: b (signed word)
5 ;   R2: c (signed word)
6 ;   R3: x (signed word)
7 ; return value:
8 ;   R0: f(x) (signed word)
```

#### (b) (i) zeroMemory (e.g. zero 1024 bytes starting at the address in R4)

```
1 ; assume some initial values in registers other than R0–R3
2 LDR    R4, =tbz
3
4 ; call zeroMemory using interface
5 MOV    R0, R4
6 LDR    R1, =1024
7 BL     zeroMemory
```

#### (ii) factorial (e.g. compute 6!)

```
1 ; assume some initial values in registers other than R0–R3
2 LDR    R4, =6
3
4 ; call factorial using interface
5 MOV    R0, R4
```



```
6      BL      factorial
7      MOV     R7, R0
```

(iii) power (assume R4, R7, R9 have some meaning in a wider context)

```
1      ; assume some initial values in registers other than R0-R3
2      LDR     R4, =4
3      LDR     R7, =3
4
5      ; call power using interface
6      MOV     R0, R4
7      MOV     R1, R7
8      BL      power
9      MOV     R9, R0
```

(iv) quadratic (assume R4, R5, R7, R9, R11 have some meaning in a wider context)

```
1      ; assume some initial values in registers other than R0-R3
2      LDR     R4, =2
3      LDR     R7, =3
4      LDR     R9, =4
5      LDR     R11, =5
6
7      ; call quadratic using interface
8      MOV     R0, R4
9      MOV     R1, R7
10     MOV     R2, R9
11     MOV     R3, R11
12     BL      quadratic
13     MOV     R5, R0
```

## 2.2 Subroutine Implementations

(i) zeroMemory

```
1 ; zeroMemory - zero a range of addresses in memory
2 ; Parameters:
3 ;   R0: start address of range to zero
4 ;   R1: length number of bytes to zero (unsigned word)
5 zeroMemory
6     STMFD    SP!, {R4-R6, LR}
7
8     ; take a local copy of each parameter
9     MOV     R4, R0
10    MOV     R5, R1
11    MOV     R6, #0
12
13    ; fill memory with zeros
14 wh1     CMP     R5, #0
15         BHS     eWh1
16         STRB    R6, [R4], #1
17         SUB     R5, R5, #1
18         B       wh1
19 eWh1
20         LDMFD    SP!, {R4-R6, PC}
21
22         ; we could have optimised this by filling words until we were left
23         ; with < 4 bytes, at which point we finish off with bytes
```

(ii) factorial



```
1 ; factorial – compute x!
2 ; Parameters:
3 ;   R0: x (unsigned word)
4 ; Return value:
5 ;   R0: x!
6 factorial
7     STMFD    SP!, {R4, LR}
8
9     ; take a local copy of each parameter
10    MOV      R4, R0
11
12    ; compute factorial
13    MOV      R0, #1
14 wh2
15    CMP      R4, #0
16    BEQ      eWh2
17    MUL      R0, R4, R0
18    SUB      R4, R4, #1
19    B        wh2
20 eWh2
21    LDMFD    SP!, {R4, PC}
```

(iii) power

```
1 ; power – compute x^y
2 ; Parameters:
3 ;   R0: x (signed word)
4 ;   R1: y (unsigned word)
5 ; Return value:
6 ;   R0: x^y
7 power
8     STMFD    SP!, {R4–R5, LR}
9
10    ; take a local copy of each parameter
11    MOV      R4, R0
12    MOV      R5, R1
13
14    ; compute x^y
15    MOV      R0, #1
16 wh3
17    CMP      R5, #0
18    BEQ      eWh3
19    MUL      R0, R4, R0
20    SUB      R5, R5, #1
21    B        wh3
22 eWh3
23    LDMFD    SP!, {R4–R5, PC}
```

(iv) quadratic

```
1 ; quadratic – evaluate a quadratic function of the form  $f(x) = ax^2 + bx + c$ 
2 ; Parameters:
3 ;   R0: a (signed word)
4 ;   R1: b (signed word)
5 ;   R2: c (signed word)
6 ;   R3: x (signed word)
7 ; return value:
8 ;   R0: f(x) (signed word)
9 quadratic
10    STMFD    SP!, {R4–R7, LR}
11
12    ; take a local copy of each parameter
13    MOV      R4, R0
14    MOV      R5, R1
```



```
15      MOV      R6, R2
16      MOV      R7, R3
17
18      ; compute quadratic
19      MUL      R0, R3, R3
20      MUL      R0, R4, R0
21
22      MUL      R5, R7, R5
23      ADD      R0, R0, R5
24
25      ADD      R0, R0, R6
26
27      LDMFD    SP!, {R4-R7, PC}
```