Company :	**GLOBALFOUNDRIES**
Company Name :	**GLOBALFOUNDRIES**
Nature Of Business :	**Service Semiconductor Foundry**
Designation :	**Senior/ Principal Engineer Design Enablement/ Device Modeling:**
Tentative Job Location :	Bangalore

Description :

Job Purpose:

To develop FET compact models in Silicon Photonics (SiPh) Semiconductor Technologies for state-of-the-art applications in the growing High Performance, Hyperscale Computing & Wired industries (CWI)

Roles and Responsibilities:

- **GLOBALFOUNDRIES is seeking a motivated, self-driven engineer to develop FET compact models which are actively used by clients to design critical CMOS circuits suchs High-Speed IOs and Transimpedance Amplifiers (TIAs) for state-of-the-art monolithic solutions. Familiarity with SOI FET transistor engineering, processing and modeling methodologies, including BSIM and PSP (bulk & SOI), are required to obtain accurate device characteristics suitable for high-frequency applications**
- **This includes an understanding of how the various model parameters affect the simulation results and how one might extract these parameters from measured data. The role requires a demonstrated background in semiconductor device physics and high-speed circuit design while utilizing automation software for data analysis, parameter extraction & simulation of the device/circuit characteristics.**
- **Comprehensive knowledge is required of Direct Current (DC), Scattering-parameter, high-frequency measurements for linear and Non-linear characterization, including de-embedding techniques. Experience working with EDA tools, hardware description languages, Electro-Magnetic and integrated circuit simulators are desirable.**
- **Applicants will be a member of an established technical team, driven by collaborative innovation and creative problem solving. Demonstrated effective communication (written & verbal), analytical thinking, desire to innovate, and people skills are also required**

Requirements:

- **Master's Degree in Electrical & Electronics, Microelectronics Engineering or Physics; PhD is preferred**
- **At least 1 years experience in Device/Circuit Design and Compact Modeling; 1+ years is preferred**
- **English: Proficient.**

Eligibilty :

Program	AE	BSBE	CE	CHE	CSE	EE	ES	ME	MSE	PHY	CHM	MTH	ECO	DES	IME	CGS	HSS	EEM	MSP	NET	PSE	Stats
BT	No	No	No	No	No	No	--	No	No	--	--	--	--	--	--	--	--	--	--	--	--	--
BS	--	--	--	--	--	--	No	--	--	No	No	No	No	--	--	--	--	--	--	--	--	--
MT	No	No	No	No	No	Yes	No	No	Yes	--	--	--	--	--	No	--	--	No	No	No	Yes	--
DoubleMajor	No	No	No	No	No	Yes	--	No	No	No	No	No	No	--	--	--	--	--	--	--	--	--
dual	No	No	No	No	No	Yes	No	No	Yes	Yes	No	No	No	--	--	--	--	--	--	--	--	--
dualB	No	No	No	No	No	Yes	--	No	Yes	Yes	No	No	No	--	No	--	--	No	--	No	Yes	--
dualC	No	No	No	No	No	Yes	No	No	Yes	Yes	No	No	No	No	No	--	--	--	--	--	--	--
Mdes	--	--	--	--	--	--	--	--	--	--	--	--	--	No	--	--	--	--	--	--	--	--
MBA	--	--	--	--	--	--	--	--	--	--	--	--	--	--	No	--	--	--	--	--	--	--
Phd	No	No	No	No	No	Yes	No	No	Yes	Yes	No	No	No	No	No	No	No	No	No	No	Yes	No
MSc	--	--	--	--	--	--	--	--	--	Yes	No	No	--	--	--	--	--	--	--	--	--	No
MSR	No	No	No	No	No	Yes	--	No	Yes	--	--	--	--	--	--	No	--	--	--	--	Yes	--

Cost to Company :	**For PhDs- CTC: 2167480 INR** **For Master's- CTC: 1288772 INR**
Package Details :	**Following is the break up for PhDs:** **Base Pay- 1850000, AIP- 185000, Gratuity- 37908, PF- 94572** **Following is the break up for Master's:** **Base Pay- 1100000, AIP- 110000, Gratuity- 22540, PF- 56232**
Bond :	**False**
CPI CutOff :	**0.0**
Medical Requirments :	**Medical Insurance is provided by the company**
Resume Shortlist :	**True**
Resume Shortlist Criteria:	**N/A**
Aptitude Test:	**False**
Group Discussion:	**False**

Technical Test:	**False**
Technical Interview:	**True**
Technical Interview Duration:	**N/A**
Number of Techincal Interview Rounds:	**3**
HR Interview:	**True**
HR Interview Duration:	**N/A**
Additional Information:	