**Tejas Networks** Company: **Company Tejas Networks** Name: **Nature Of Business:** Designation **Hardware Engineer** : Tentative Job Bangalore Location: **FPGA Design** You will be a key member of the design/development team of FPGA systems mainly working on VHDL/Verilog for telecom applications **Proficiency: Description:** You need to have a thorough understanding of hardware concepts and be very comfortable with electronic circuits and how they operate You need to be familiar with digital/analogue design concepts Exposure to FPGA design is an advantage You are a self-starter and have ability to think deeply Program AE BSBE CE CHE CSE EE ES ME MSE PHY CHM MTH ECO DES IME CGS HSS EEM MSP NET PSE Stats BT No No No No No No -- No No BS -- No -- --No No No No MT No No Yes Yes No DoubleMajor No No No No No No -- No No Nο Nο Nο Nο No No dual No No Yes Yes No No No Nο Nο Nο Nο No **Eligibilty:** dualB No No No No Yes Yes-- No No No No No No No No dualC No No No No Yes Yes No No No No No No No No No Mdes No MBA --No Phd No MSc -- ---- ------ -- -- --No MSR No No No No Yes Yes -- No No No No **Particulars B.Tech** M.Tech 8.91 Fixed Component 9.33 0.54 Variable Pay Cost to Company: TOTAL 8.91 9.87 0.26 0.26 Welfare Benefit Retrials (PF + Gratuity) 0.83 0.87 **Cost to Company 10 LPA 11 LPA Particulars B.Tech** M.Tech 8.91 9.33 Fixed Component Variable Pay 0.54 **Package Details:** 9.87 TOTAL 8.91 0.26 0.26 Welfare Benefit Retrials (PF + Gratuity) 0.83 0.87 **Cost to Company 10 LPA 11 LPA False** Bond: **CPI CutOff:** 0.0Medical Requirments : Resume True **Shortlist:** Resume 7 **Shortlist** Criteria: **Aptitude** 

True

**Test:** 

Aptitude Test **45 Duration:** Group False **Discussion:** Technical True **Test: Technical 45** Test **Duration: Technical** True Interview: **Technical** Interview 60 **Duration:** Number of **Techincal** 2 Interview **Rounds:** HR True Interview:  $\mathbf{H}\mathbf{R}$ Interview **30 Duration:** 

Additional Information: