

Company :	Marvell Semiconductors
Company Name :	Marvell Semiconductors
Nature Of Business :	R & D
Designation :	Design Engineer
Tentative Job Location :	Bangalore

Hardware JD:

Responsibilities:

As member of the Marvell team,

- You will be involved in the area of Logic Design/Integration, Functional Verification, Design for Test (DFT), Analog design & Layout, Physical Implementation, Low Power & Signoff for processor systems, ASICs or IPs.
- Opportunity to work for complete SoC design cycle, starting from Architecture definition and logic design, feasibility planning/benchmarking for Power/Performance/Area/Yield to end-to-end Design/Implementation/Signoff
- Opportunity to work on challenging design architecture across Networking, Processor, Computing, Automotive, Switching, Connectivity and Security, in the technology nodes across 5nm/7nm/12nm/14nm and more.
- You will work closely with different functional teams in Marvell and enable successful products for the next generation technology.
- Opportunity to work in multi core ARM sub-system architecture, high speed interface designs using Serdes, PCI-e, DDR4, low power design architecture and design/manufacturing for high quality/reliability.

Requirements:

- BE/BTech or ME/MTech in EE/EC/VLSI/Instrumentation with 0-1 years of experience.
- Exposure on Design, Verification, Test, Physical implementation, Layout and Semiconductor device/process through previous work/intern experience or course work.
- Experience in one or more of below topics, through course work or internship experience:
- Coding language like SystemVerilog, Verilog, C/C++ or Assembly language in Test bench development in any of the languages,
- Verification methodology like UVM or VMM or OVM,
- Design for Test and Simulations using EDA tools,
- Physical design/Implementation using EDA tools,
- Synthesis/STA Timing using EDA tools,
- Low Power Design/Optimization and Reliability signoff using EDA tools,
- Understanding of the fundamentals of circuit design
- Strong intuitive and analytical understanding of transistor-level circuit and layout design
- Should have good knowledge of CMOS process and fabrication
- Custom layout and Physical verification using EDA tools,
- Scripting/programming using Tcl/Tk/Perl/Python/Shell
- Detail oriented, self-motivated team worker, good verbal and written communication skills
- Strong Digital Design concepts and debugging skills

Marvell gives Equal Opportunity Employer and considers applicants for all positions without regard to race, color, creed, religion, ancestry, national origin, age, gender identity, sex, marital status, sexual orientation, physical or mental disability, Be sure to include your name, If you are ready to excel, innovate, and truly enjoy where you work, apply now for the position detailed below.

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[illegible]

Eligibility :	dualB	No	No	No	No	Yes	--	No	No	No	No	No	No	--	No	--	--	No	--	No	No	--
	dualC	No	No	No	No	Yes	No	No	No	No	No	No	No	No	No	--	--	--	--	--	--	--
	Mdes	--	--	--	--	--	--	--	--	--	--	--	No	--	--	--	--	--	--	--	--	
	MBA	--	--	--	--	--	--	--	--	--	--	--	--	No	--	--	--	--	--	--	--	
	Phd	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	No	
	MSc	--	--	--	--	--	--	--	--	No	No	No	--	--	--	--	--	--	--	--	No	
	MSR	No	No	No	No	Yes	--	No	No	--	--	--	--	--	--	No	--	--	--	--	No	--

Cost to Company :

CTC - 19.73 LPA

Package Details :

Fixed Salary - 14.09 LPA

Bond :

False

CPI CutOff :

0.0

Medical Requirments :

Resume Shortlist :

True

Resume Shortlist Criteria:

7/10

Aptitude Test:

True

Aptitude Test

45 Mins

Duration: Group

False

Discussion: Technical

True

Technical Test

45 Mins

Duration: Technical Interview:

True

Technical Interview Duration:

60 Mins

Number of Techincal Interview Rounds:

3

HR Interview:

True

HR Interview Duration:

30 Mins

Additional Information: