Company : **GLOBALFOUNDRIES**

Company Name : **GLOBALFOUNDRIES**

Nature Of Business : **Service Semiconductor Foundry**

Designation : **Principal Design Enablement Engineer/ eFUSE Circuit Design:**

Tentative Job Location : Bangalore

Description :

Your tasks:

In this position you will be integrated in our Technology Enablement team, especially in the Advanced Circuit Design (ACD) department.

In close collaboration with other disciplines across our worldwide engineering teams you will be developing One Time Programmable Memory (OTP) IP which enable our customers to perform product designs at highest quality standards based on Globalfoundries' advanced process nodes.

Your responsibilities include:

The development of product grade eFUSE based OTP IP covering the following phases:

- **Circuit design and verification**
- **Layout Guidance**
- **Sign off and release into dedicated IP validation test chips**
- **Specification and documentation**
- **Support of the silicon bring up and characterization**
- **Customer support at design-in as well as at Si bring up phases**

The expansion into novel OTP/MTPM memory approaches needed for emerging security apps

Requirements:

You have a Master's Degree or PhD in semiconductors/Microelectronics/VLSI engineering from a reputed university/IIT/NIT/BITS.

Ideally you have gained either practical experiences or academic experience as part of your thesis in Custom Mixed-Signal or in Memory design at one or several of the following areas:

- **Memory design (OTP, SRAM, DRAM or NVM)**
- **General analog mixed-signal design**

Further desired skills are:

- **Good knowledge of CMOS technology**
- **Knowledge of state of the art memory or analog design flows**
- **Programming experience applicable to design flow automation tasks**
- **The capability to work within a very dynamic interdisciplinary environment as well as dedicated knowledge of 45/32/28nm and below technology nodes are an advantage.**
- **You are flexible, highly motivated and have a team-oriented working style.**
- **You have shown the ability to communicate as well as work efficiently in an international**
- **Multi-disciplinary environment.**
- **Strong written and verbal communication skills in English are a must.**

Eligibilty :

Program	AE	BSBE	CE	CHE	CSE	EE	ES	ME	MSE	PHY	CHM	MTH	ECO	DES	IME	CGS	HSS	EEM	MSP	NET	PSE	Stats
BT	No	No	No	No	No	No	--	No	No	--	--	--	--	--	--	--	--	--	--	--	--	--
BS	--	--	--	--	--	--	No	--	--	No	No	No	No	--	--	--	--	--	--	--	--	--
MT	No	No	No	No	No	Yes	No	No	Yes	--	--	--	--	--	No	--	--	No	No	No	No	--
DoubleMajor	No	No	No	No	No	Yes	--	No	No	Yes	No	No	No	--	--	--	--	--	--	--	--	--
dual	No	No	No	No	No	Yes	No	No	Yes	Yes	No	No	No	--	--	--	--	--	--	--	--	--
dualB	No	No	No	No	No	Yes	--	No	Yes	Yes	No	No	No	--	No	--	--	No	--	No	No	--
dualC	No	No	No	No	No	Yes	No	No	Yes	Yes	No	No	No	No	No	--	--	--	--	--	--	--
Mdes	--	--	--	--	--	--	--	--	--	--	--	--	--	No	--	--	--	--	--	--	--	--
MBA	--	--	--	--	--	--	--	--	--	--	--	--	--	--	No	--	--	--	--	--	--	--
Phd	No	No	No	No	No	Yes	No	No	Yes	Yes	No	No	No	No	No	No	No	No	No	No	No	No
MSc	--	--	--	--	--	--	--	--	--	Yes	No	No	--	--	--	--	--	--	--	--	--	No
MSR	No	No	No	No	No	Yes	--	No	Yes	--	--	--	--	--	--	No	--	--	--	--	No	--

Cost to Company : **For PhDs- CTC: 2167480 INR**

For Master's- CTC: 1288772 INR

Package Details : **Following is the break up for PhDs:**

Base Pay- 1850000, AIP- 185000, Gratuity- 37908, PF- 94572

Following is the break up for Master's:

Base Pay- 1100000, AIP- 110000, Gratuity- 22540, PF- 56232

Bond :	**False**
CPI CutOff :	**0.0**
Medical Requirments :	**Medical Insurance is provided by the company**
Resume Shortlist :	**True**
Resume Shortlist Criteria:	**N/A**
Aptitude Test:	**False**
Group Discussion:	**False**
Technical Test:	**False**
Technical Interview:	**True**
Technical Interview Duration:	**N/A**
Number of Techincal Interview Rounds:	**3**
HR Interview:	**True**
HR Interview Duration:	**N/A**
Additional Information:	