Company :	**Texas Instruments**
Company Name :	**Texas Instruments**
Nature Of Business :	**Semiconductor R&D**
Designation :	**Digital Engineer**
Tentative Job Location :	Bangalore

Description :

Texas Instruments Incorporated is an American technology company that designs and manufactures semiconductors and various integrated circuits. TI is one of the top-10 semiconductor companies worldwide, based on sales volume and is focused on developing analog chips and embedded processors, which account for more than 80% of their revenue. TI has been a pioneer in many innovations in the semi-conductor domain including the development of the first integrated circuit; the first patent on a single-chip microprocessor, the first single-chip linear predictive coding speech synthesizer, developing prototype of the world's first transistor radio and the invention of the digital light processing device (also known as the DLP chip), which serves as the foundation for the award-winning DLP technology and DLP Cinema.

TI India was set up in 1985 and has R&D presence for all the major business units of TI including Analog - (Data Converters, Amplifiers, Clocks & Synthesizers, Motor Drives, Power Management) and Embedded Processors (Connected Microcontrollers, Radar, ADAS- Advanced Driver Assistance and Infotainment and Industrial Processors etc.) and caters to products for different market segments - Industrial, automotive, personal Electronics, Communication and Enterprise.

As a Digital Engineer at TI, You'll define, design, model, implement and document Integrated Circuits (ICs). You will also have the opportunity to work in exciting areas like audio, energy automation, electronic point of service, industrial automation, infotainment, ADAS, Imaging, high speed interface, clocking medical, high volume linear, automotive, storage, power supply, battery management, linear power, DLP and many more.

Your responsibilities will include:

1) Partnering with business teams and systems engineering to develop mutually agreeable design specifications

2) Providing high-level analysis on chip architecture trade-offs to ensure spec compliance and superior performance at a competitive cost

3) Participating in design reviews and creating the necessary design and product documentation

4) Supervising IC Layouts to ensure a high performance standard

5) Characterizing prototypes, developing test specifications and coordinating with test/product engineering to drive product releases

6) Driving behavioral models

Eligibilty :

Program	AE	BSBE	CE	CHE	CSE	EE	ES	ME	MSE	PHY	CHM	MTH	ECO	DES	IME	CGS	HSS	EEM	MSP	NET	PSE	Stats
BT	No	No	No	No	No	Yes	--	No	No	--	--	--	--	--	--	--	--	--	--	--	--	--
BS	--	--	--	--	--	--	No	--	--	No	No	No	No	--	--	--	--	--	--	--	--	--
MT	No	No	No	No	No	Yes	No	No	No	--	--	--	--	--	No	--	--	No	No	No	Yes	--
DoubleMajor	No	No	No	No	No	Yes	--	No	No	No	No	No	No	--	--	--	--	--	--	--	--	--
dual	No	No	No	No	No	Yes	No	No	No	No	No	No	No	--	--	--	--	--	--	--	--	--
dualB	No	No	No	No	No	Yes	--	No	No	No	No	No	No	--	No	--	--	No	--	No	Yes	--
dualC	No	No	No	No	No	Yes	No	No	No	No	No	No	No	No	No	--	--	--	--	--	--	--
Mdes	--	--	--	--	--	--	--	--	--	--	--	--	--	No	--	--	--	--	--	--	--	--
MBA	--	--	--	--	--	--	--	--	--	--	--	--	--	--	No	--	--	--	--	--	--	--
Phd	No	No	No	No	No	Yes	No	No	No	No	No	No	No	No	No	No	No	No	No	No	Yes	No
MSc	--	--	--	--	--	--	--	--	--	No	No	No	--	--	--	--	--	--	--	--	--	No
MSR	No	No	No	No	No	Yes	--	No	No	--	--	--	--	--	--	No	--	--	--	--	Yes	--

Cost to Company :

B.tech : 21,50,880

M.tech:24,48,905

Package Details :

B.tech : 21,50,880
Fixed: 14,00,000
Variable: 2,10,000
benefits: 1,15,880
Joining Bonus: 350,000 (paid in 2 installments, half immediately on joining and the rest half on completion of 1 year)
Relocation assistance one time: 75,000

M.tech:24,48,905
Fixed: 15,25,000
Variable: 2,28,750
benefits: 1,20,155
Joining Bonus: 500,000 (paid in 2 installments, half immediately on joining and the rest half on completion of 1 year)
Relocation assistance one time: 75,000

Bond :	**False**
CPI CutOff :	**0.0**
Medical Requirments :	
Resume Shortlist :	**False**

Aptitude Test:	**True**
Aptitude Test Duration:	**30 min**
Group Discussion:	**False**
Technical Test:	**True**
Technical Test Duration:	**45 min**
Technical Interview:	**True**
Technical Interview Duration:	**1 hour**
Number of Techincal Interview Rounds:	**2**
HR Interview:	**True**
HR Interview Duration:	**15 min**
Additional Information:	