Samsung Semiconductor India Research Center Company: **Company** Samsung Semiconductor India Research Center Name: **Nature Of** Semiconductor **Business:** Designation Senior Engineer - Hardware Tentative Job Bangalore Location: Hardware: Analog and Digital design (RTL, Synthesis Layout) for CIS, PMIC, HI Speed Interface like PCIe, LPDDR4, SERDES, SATAe, NVMe, UFS and etc, Standard cell and Memory Compiler, PDK, Verification, layout, enabling fabrication **Description:** on latest Nodes, Signal/Image processing with DSP, GPGPU, CPU-SIMD, solutions enabling & tuning on best/latest smartphone platforms. Program AE BSBE CE CHE CSE EE ES ME MSE PHY CHM MTH ECO DES IME CGS HSS EEM MSP NET PSE Stats No No ВТ No No No Yes -- No No BS No --Nο Nο No Nο MT No Yes No No No No No No No ------No No No No No --DoubleMajor No No No No No Yes -- No No No No No No dual No No No No No Yes No No No No No No No **Eligibilty:** dualB No No No No No Yes -- No No No No No No --No No No No dualC No No No No Yes No No No No No No No No No Mdes No MBA -- ----No Phd No Nο No No MSc No No No No MSR No No No No No Yes -- No No No No Bachelors: 22,75,000 Cost to **Company:** Masters: 23,75,000 Bachelors 15,75,000 + 7,00,000 RB 1st year + 5,00,000 2nd year + 2,00,000 3rd year **Package Details:** Masters 16,75,000 + 7,00,000 RB 1st year + 5,00,000 2nd year + 2,00,000 3rd year Bond: False 0.0 **CPI CutOff:** Medical Requirments **Resume** True **Shortlist:** Resume **Shortlist** 7.5 cgpa Criteria: **Aptitude False Test:** Group **False** Discussion: **Technical** True Test: **Technical** 90 mins Test **Duration: Technical** True Interview: **Technical** Interview 45 mins **Duration:** Number of **Techincal** 2 **Interview Rounds:** HR True Interview: HR Interview 20 **Duration: Additional** 7.5 cgpa

Information: