Design of 3T-1D Capacitorless DRAM using CMOS

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Abstract

Many different cell designs exist for modern day DRAM cell. These designs are differentiated by the no. of transistors used in their designing. As the no. of transistors increase, power dissipation also increases. In this paper, 3T1D DRAM cell is designed and analyzed. These DRAMs have an advantage over SRAM, that is, their resistance to process variation. This feature helps it to be used at low feature sizes. Another advantage of 3T1D DRAM is that it does not slow down as its size is scaled down. 3T1D DRAM uses the gated diode instead of capacitor to store the data value. The absence of a capacitor in it provides a significant reduction in power consumption as compared to several DRAM cell designs.

1. Reference Circuit Details

This 3T-1D DRAM cell is very different from all others DRAM cell. Its key feature is that it provides non-destructive read operation and also its speed of operation is high, it gives less leakage power and is more stable than the SRAM and other capacitor-based DRAMs. Variation only affects the operating frequency of the cell, making it much more robust to process variations than the 6T design. Fig. 1[a] represents a 3T-1D DRAM cell and Fig 1[b] shows the transistor-level reference schematic of the cell.

To write to the cell, the write bitline is charged to the value we wish to store in the cell, and the write wordline is strobe. To read from the cell, the read bitline is precharged high and the read wordline is strobe. If a 1 is stored in the cell, transistor T2 turns on and the bitline discharges. The key to fast access times is the gated diode, which is tied to the read wordline. When a 1 is stored in the cell, the diode provides a 'boosting' effect to the value at the storage temporarily giving it a value close to (and sometimes greater than) Vdd, allowing T2 to turn on quickly and discharge the bitline. When a 0 is stored in the cell, the capacitance of D1 is smaller and little to no voltage boosting occurs, keeping T2 turned off. Because the 3T-1D is a dynamic memory, the value at the storage node[s] leaks away with time.

2. Reference Circuit

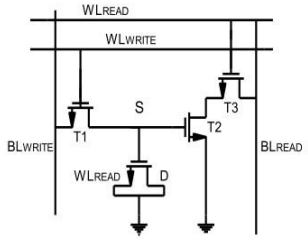

Figure 1[a]: 3T-1D DRAM Cell

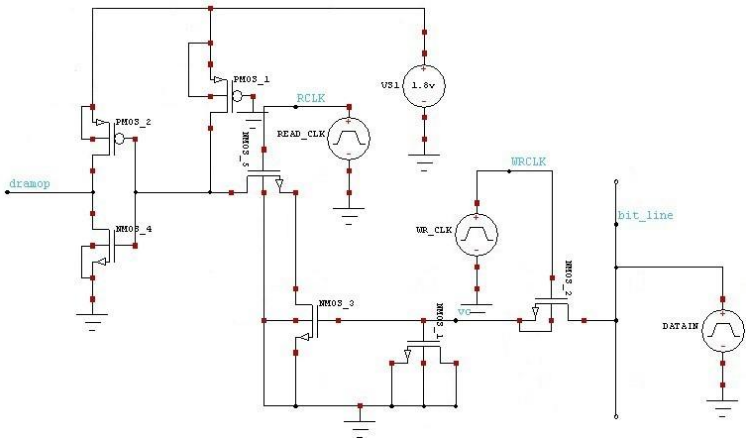

Figure 1[b]
Reference Circuit Diagram of 3T-1D DRAM

3. Reference Circuit Waveform

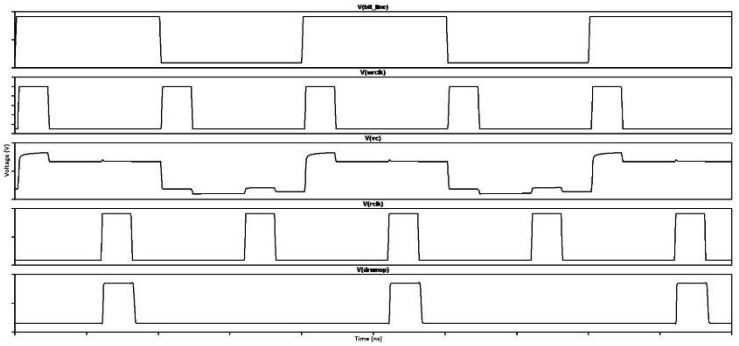

Figure 2: Reference waveform

References

1. Prateek Asthana, Sangeeta Mahesh, "Performance Comparison of 4T, 3T and 3T1D DRAM cell design on 32 nm Technology", 4th International Conference on Computer Science, Engineering and Applications, July 2014

2. Prof Y.N Thakare, Dr. S.N. Kale, "Comparative Analysis of 4T and 3T-1D DRAM to minimize Power Consumption", Journal of Applied Science and Computations, ISSN NO: 1076-5131