MÜHENDİSLİK FAKÜLTESİ
FACULTY OF ENGINEERING
ELEKTRİK-ELEKTRONİK MÜHENDİSLİĞİ BÖLÜMÜ
DEPARTMENT OF ELECTRICAL AND
ELECTRONICS ENGINEERING

ORTA DOĞU TEKNİK ÜNİVERSİTESİ
MIDDLE EAST TECHNICAL UNIVERSITY

DUMLUPINAR BULVARI 06800
ÇANKAYA ANKARA/TURKEY
T: +90 312 210 23 02
F: +90 312 210 23 04
ee@metu.edu.tr
www.eee.metu.edu.tr

EXPERIMENT 4. DECIMATION, INTERPOLATION AND PHASE-LOCKED LOOP
PART 2
LABORATORY REPORT

Student 1: Abdullah Canbolat, 2304244
Student 2: Güray Özgür, 2167054
Student 3: Yunus Bilge Kurt, 2232395

In this part, you will implement decimation, interpolation, resampling, and phase-locked loop operations in LabVIEW.
Do not forget to ATTACH all your block diagrams and front panels to the report. ALSO, UPLOAD your vi files to ODTUClass. If your block diagram does not fit to a single photo, you may consider using multiple photos and showing your block diagrams and front panels part by part.
Choose decimation factor (M), interpolation factor (L), resampling by non-integer ratio, and sampling frequency as in PART 1. Write these values into your report. Arrange the number of samples so that at least four waveforms of the signals are shown in the graphs.
M=4, L=5

Task 1

a) Design a block diagram for the **decimation**. **Attach the time domain** and **frequency contents** of the original and decimated signals on the **same graph.**

The decimation is done with the same .vi file by setting upsampling factor to 1 and decimation factor to 4, and the time domain and frequency domain contents are shown in Figure 1. It is expected to see the time range is decreased and frequency range is increased at the output, which is also observed on Figure 1.

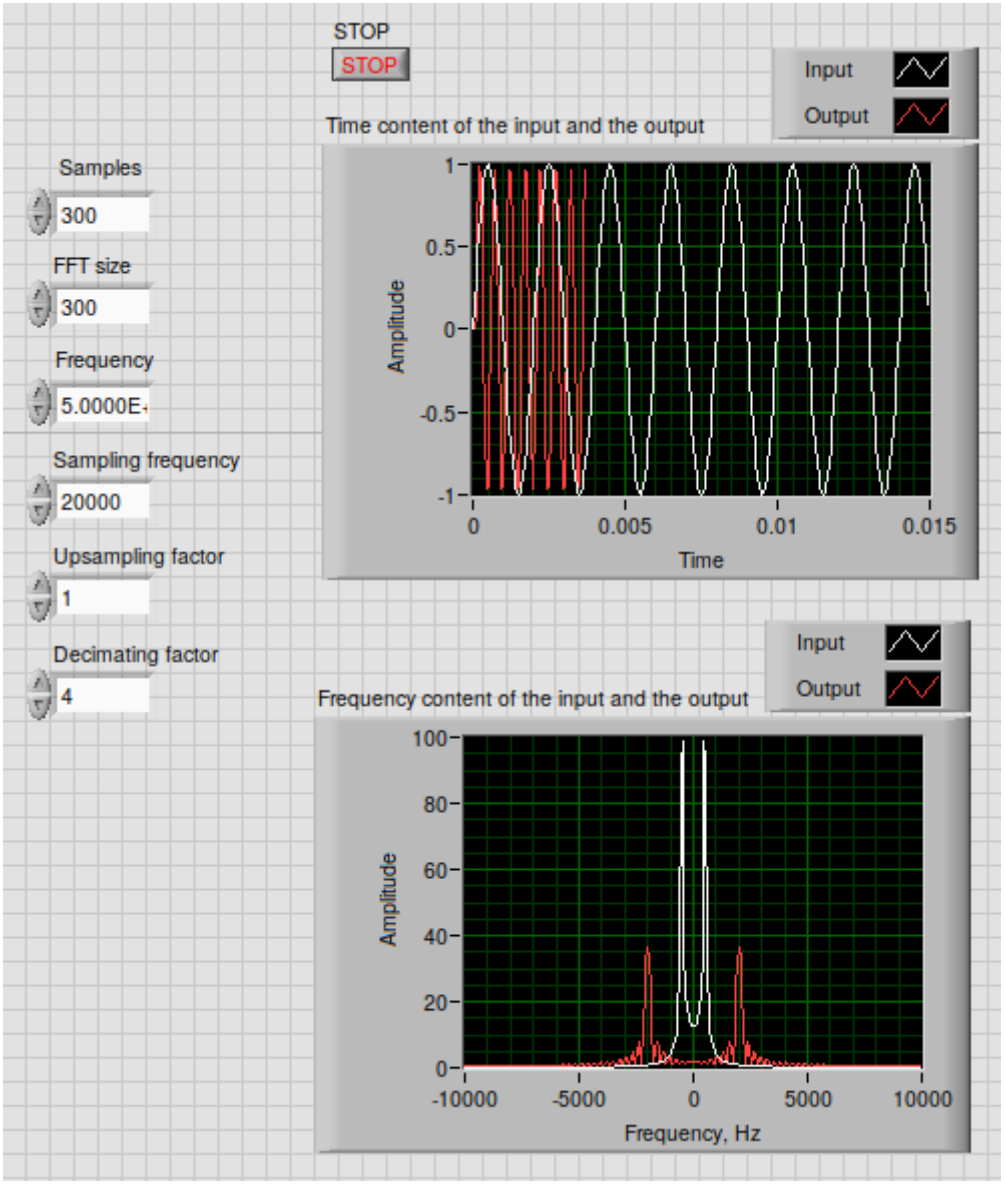

Figure 1: Original and decimated signal with a decimating factor 4

b) Design a block diagram for the **interpolation**. **Attach the time domain** and **frequency contents** of the original and interpolated signals on the **same graph.**

The interpolation is done with the same .vi file by setting upsampling factor to 5 and decimation factor to 1, and the time domain and frequency domain contents are shown in Figure 2.

When we look at Figure 2, we see that the duration of the signal is increased by L=5. It is expected since we add L-1 zeros between consecutive terms in the original signal. Then, we smooth the signal by applying a low-pass filter with a cutoff frequency of π/5 in the discrete domain . That is why it looks similar to the original curve and duration is increased when sampling rate is kept constant. We see that frequency of the output signal is decreased. Also, the zero padded signal has the same power as the original signal, by using a filter with gain 5, we restore the amplitude of the signal in the time domain. Therefore, we see a Fourier coefficient with amplitude increased by 5 and frequency decreased by 5.

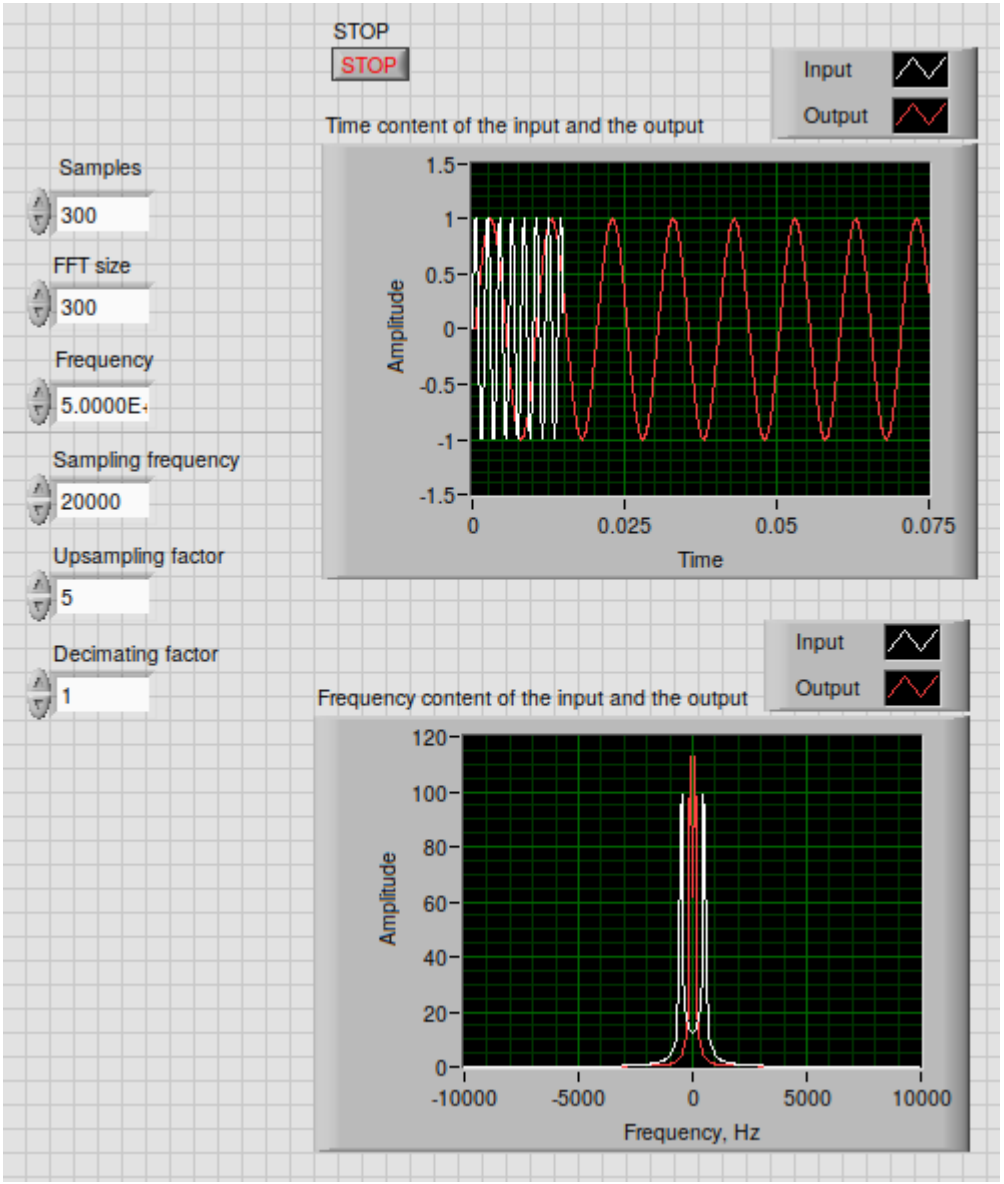

Figure 2: Original and interpolated signal with a decimating factor 5

c) Also, plot **decimated, original and interpolated signals** in time on the **same graph.**

Since all of the operation is done as a whole and approved by the assistant, we did not copy the parts of vi for the decimation and interpolation to obtain such a figure.

d) Design a block diagram for the **resampling with a non-integer ratio**. **Attach the time domain** and **frequency contents** of the original and resampled signals on the **same graph**.

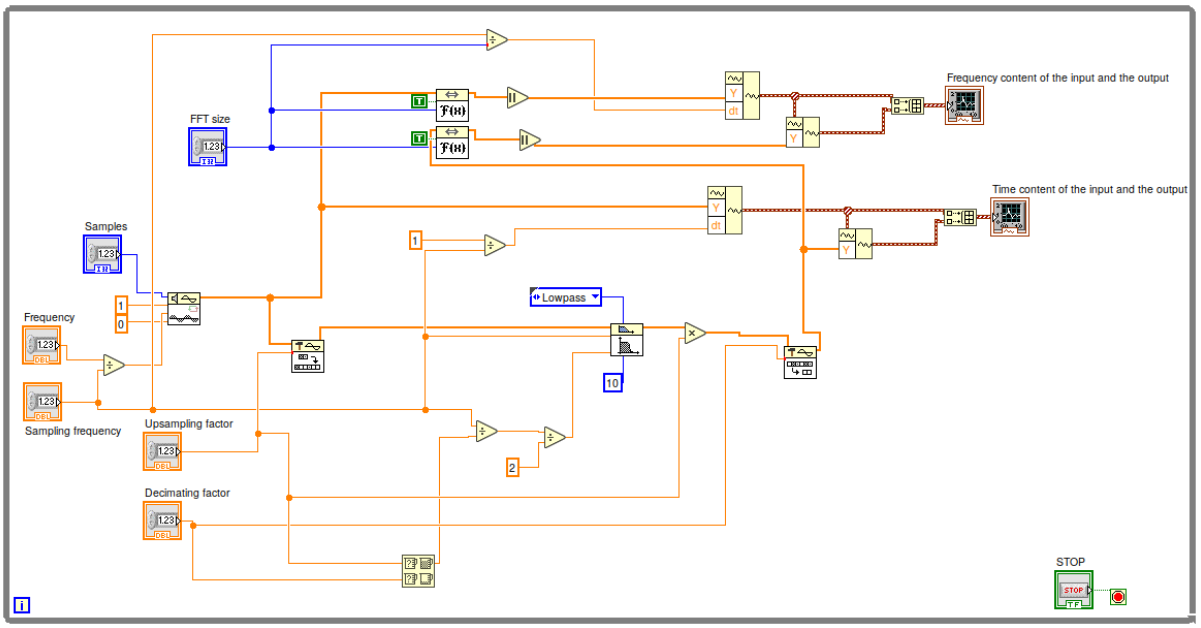

Figure 3: Block diagram for decimation, interpolation and resampling with a non-integer ratio

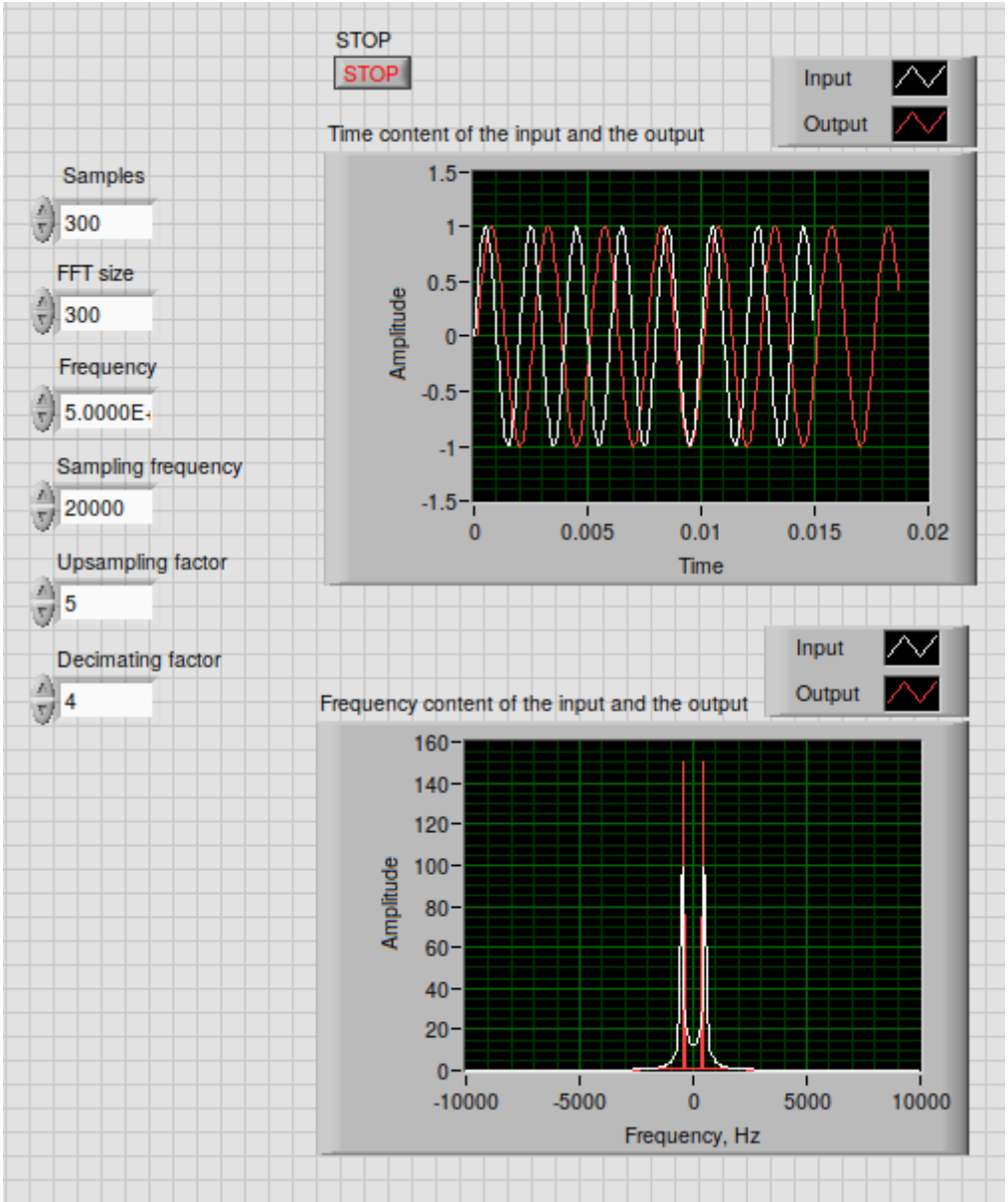

Figure 4: Original and interpolated signal with a resampling factor of 5/4

e) Design a block diagram for **PLL** by using the experiment manual for Part 2 and your MATLAB Codes. For this purpose, you may create another vi file, or you may place all your block diagrams (interpolation, decimation, PLL, etc.) in the same vi.

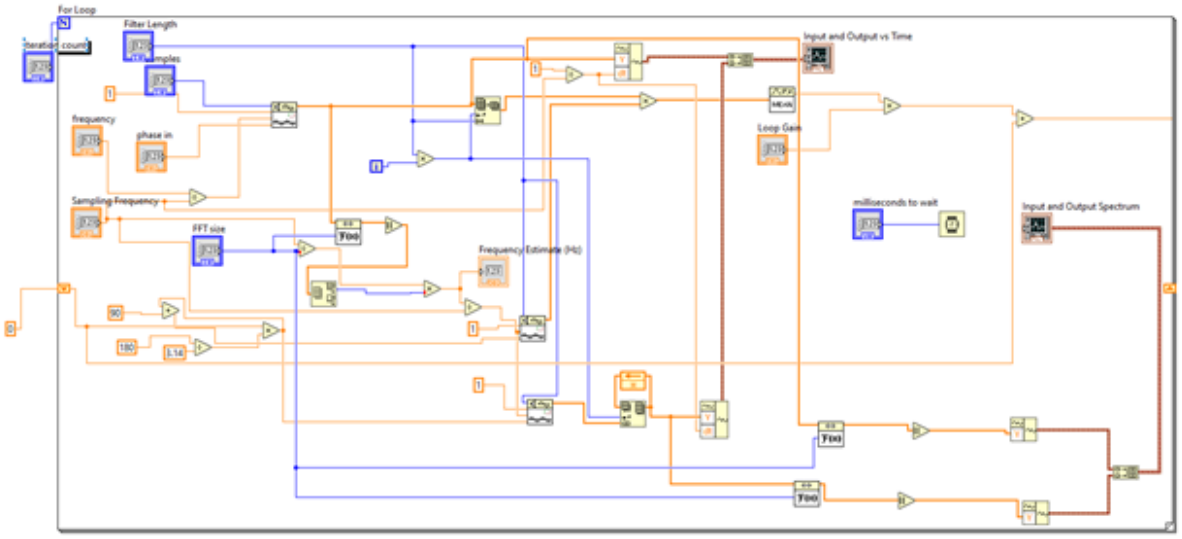

Figure 5: Block diagram for PLL

f) Arrange your parameters, as shown in Fig.1. See whether locking occurs. **Plot input and locked waveforms** on the same graph and **attach** it to the report. Also, add **plots of input and locked waveforms for phase 20 and 80 degrees.**

We observe that locking occurs for every input phase, however if the initial phase is far away from the phase, locking takes time, convergence speed is lower.

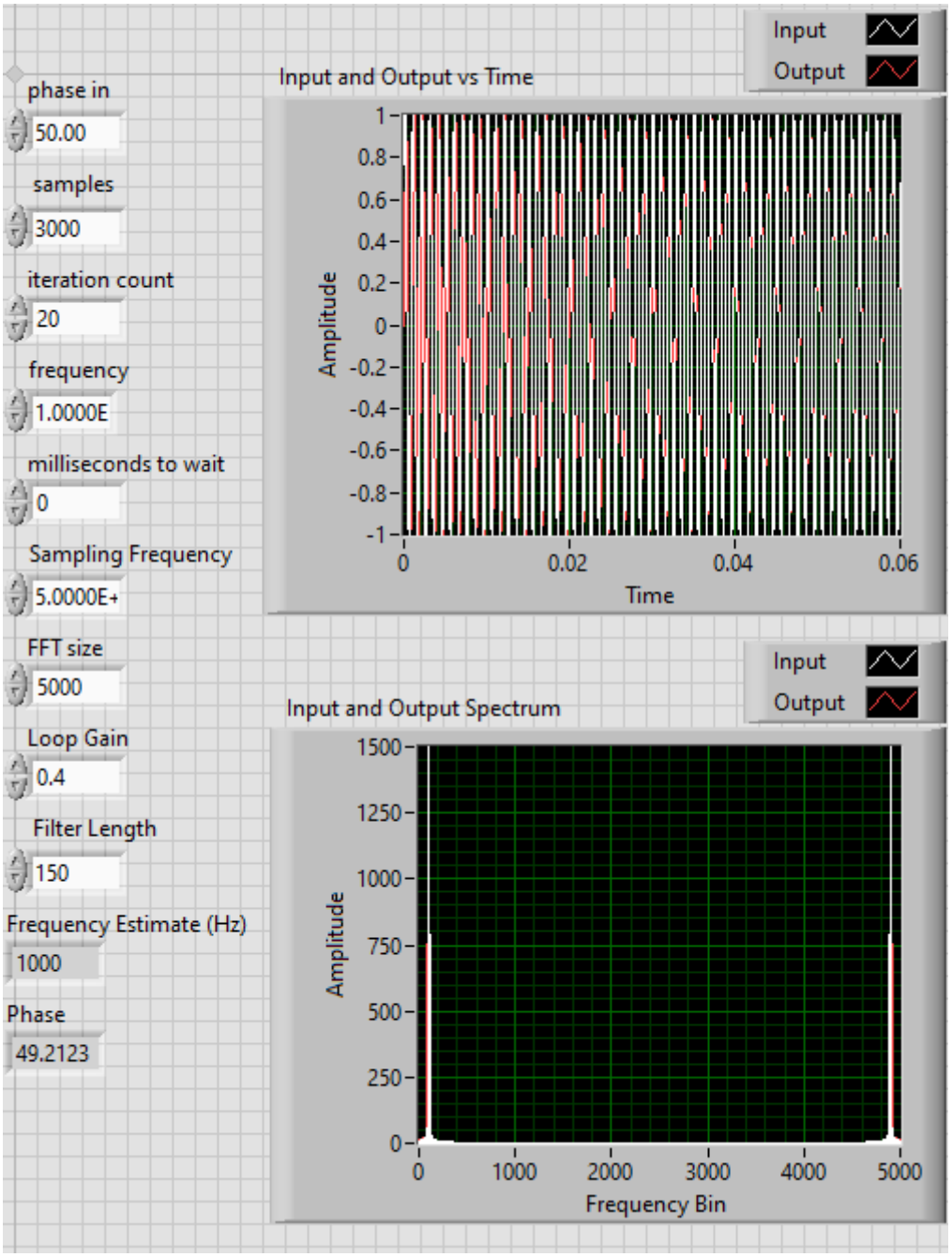

Figure 6: Input and locked waveforms for phase 50 degrees

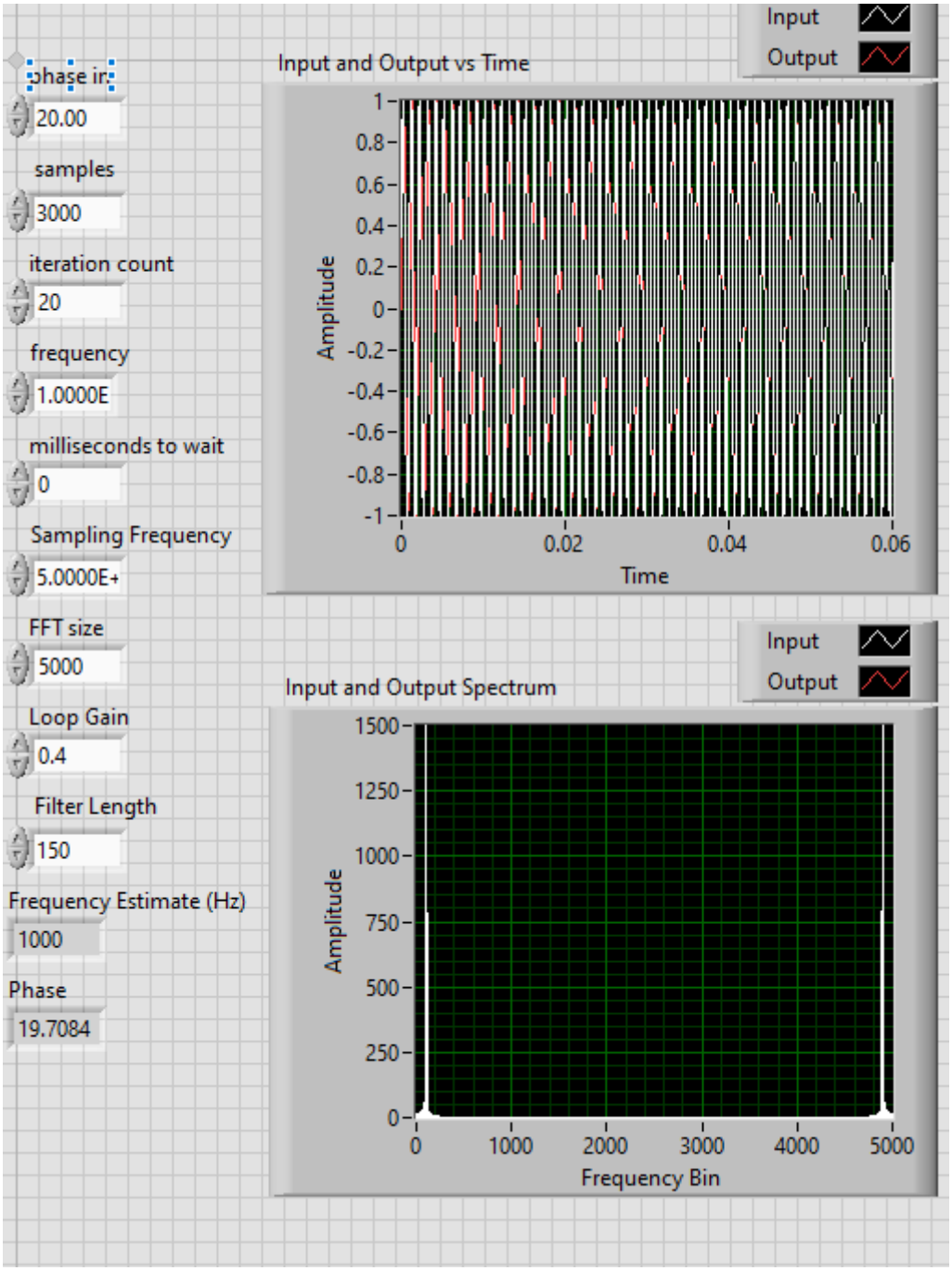

Figure 7: Input and locked waveforms for phase 20 degrees

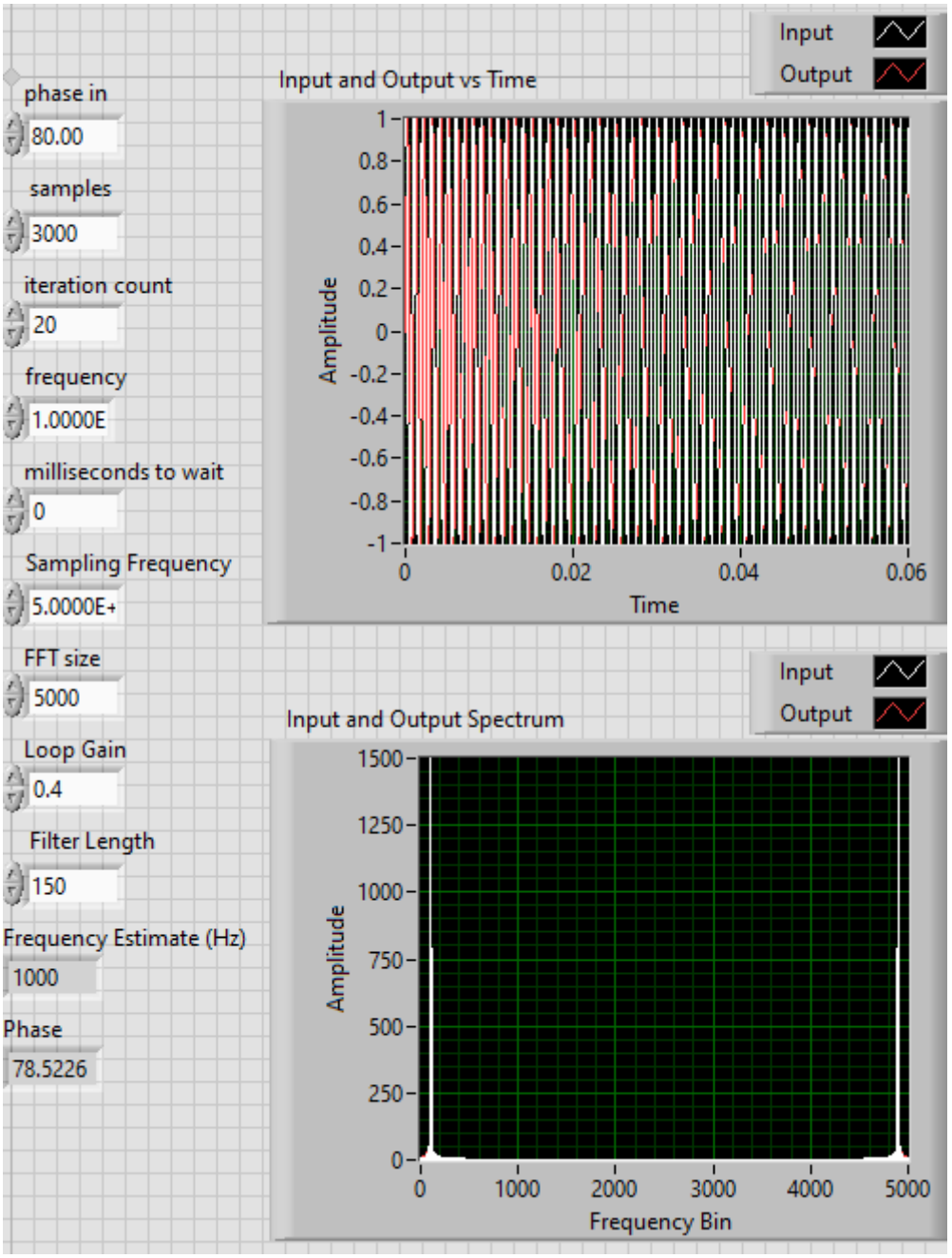

Figure 8: Input and locked waveforms for phase 80 degrees

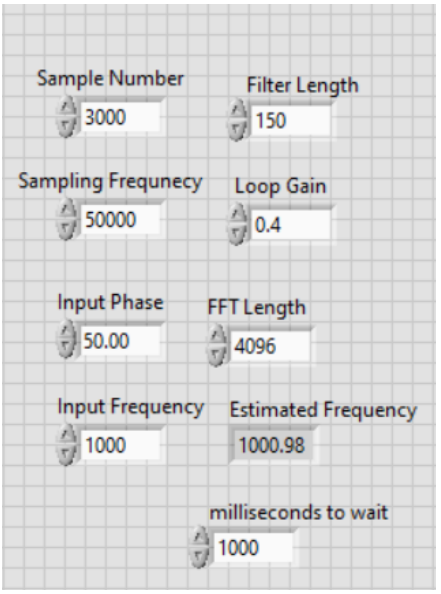

Fig. 1. Default Front Panel Parameters

g) Determine the input frequency where PLL is **not locked any longer**. **Note** this value in your report. Also, **attach the plot of input and locked signals at that frequency.**

Since with given parameters, it is not locked, we have increased the FFT size to have a better frequency estimation. With a good frequency estimation, we have obtained a locked signal. So, in our case, the frequency where PLL is not locked is 1010 Hz for a FFT size of 5000, which is shown in Figure 9.

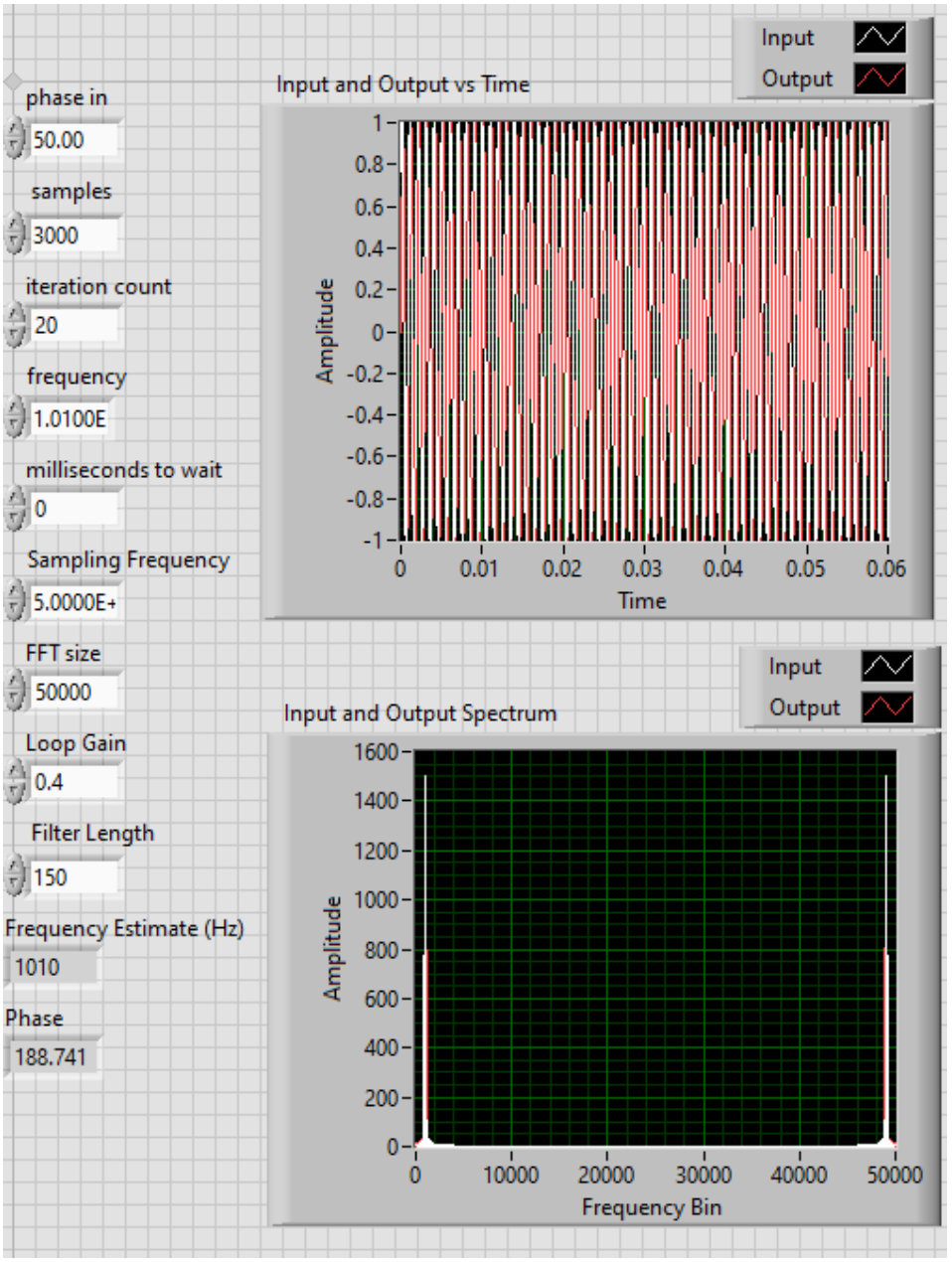

Figure 9: Input and locked waveforms for a frequency where PLL in not locked

h) Set the parameters, as shown in Fig.1. Only for this part, fix the VCO frequency to 1000 Hz, i.e., it is not determined by the estimated frequency. Gradually **increase the** input frequency with 10Hz steps. Determine the **frequency** where PLL is **not locked any longer.** Note this value in your **reports.** Also, **attach** plots of input and not-locked signals at this frequency value. **Comment** on your results.

With a better estimated frequency, which is in this case the actual frequency, locking occurs better. Sometimes, as in our case, while 1000.98 Hz is a good estimation, locking does not occur, with 1000 Hz, with the actual value, locking occurs. So, the estimation is important, since we use the identities of trigonometric functions by assuming it is the same frequency.

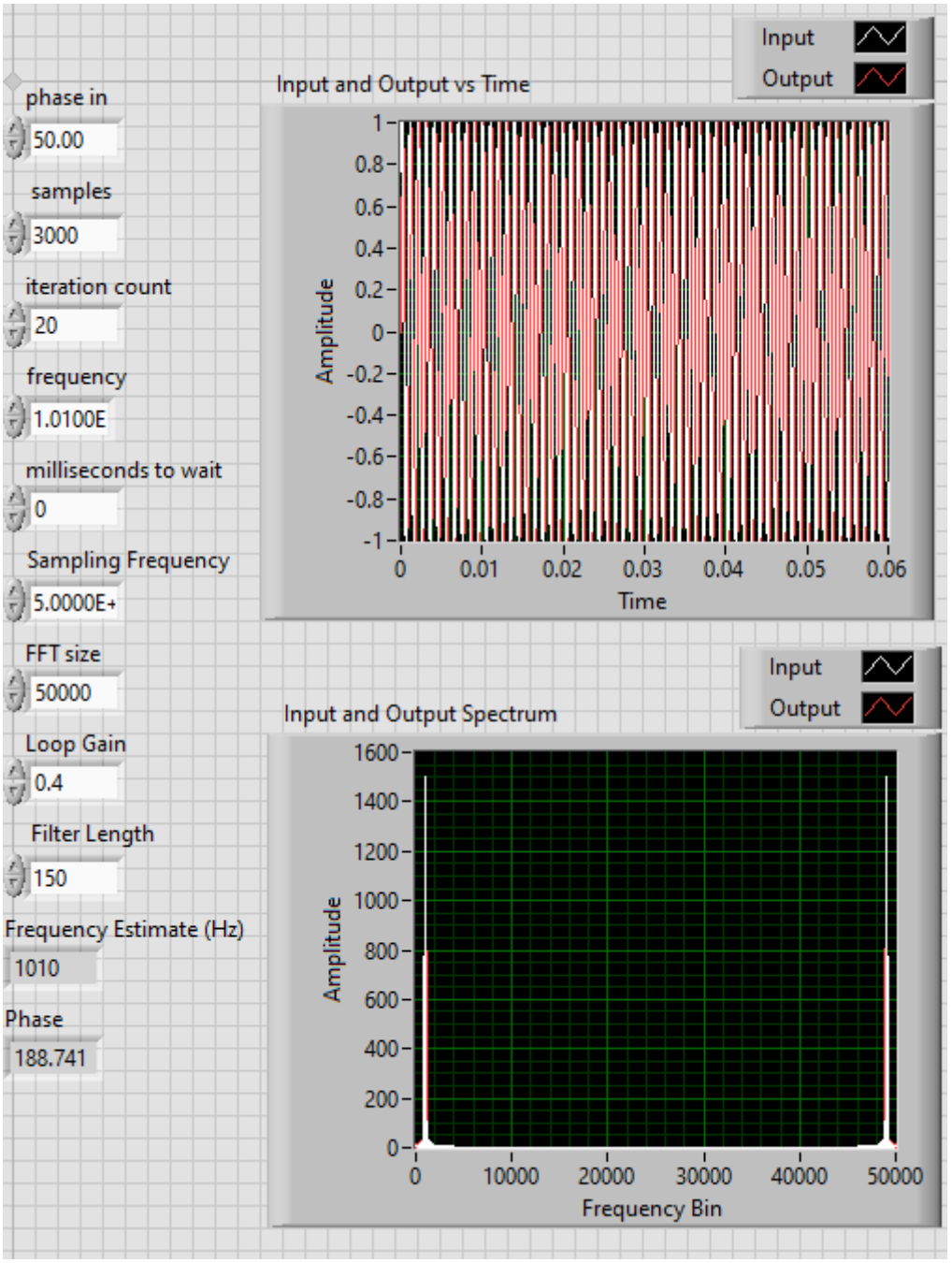

Figure 10: Input and locked waveforms for a frequency where PLL in not locked

i) Set the parameters, as shown in Fig.1. Now you need to observe the effect of the loop gain. **Increase the loop gain** from **0.05 to 2 in 0.2 steps**. **Determine** the value of loop gain where the PLL **does not lock on the input signal**. **Write** this value in your report. Also, **attach** plots of input and locked signals **at this loop gain value**, **and at loop gain value 0.05**. **Comment** on the effect of small and large loop gain. **Briefly compare your results with your theoretical expectations.**

As stated in the lecture notes, the lock range of PLL is $[f_0 - K_0/2, f_0 + K_0/2]$ where K_0 is the Loop Gain and f_0 is the input frequency which is equal to the VCO frequency. For large K_0values the PLL might become unstable, and for small K_0 the lock may not be possible because of the small range.

When the loop gain is 0.05, we couldn't see convergence, because the number of samples is insufficient to see the convergence. Loop gain determines the convergence speed of the PLL as we multiply the phase error with the loop gain, therefore the phase of our output converges more slowly.

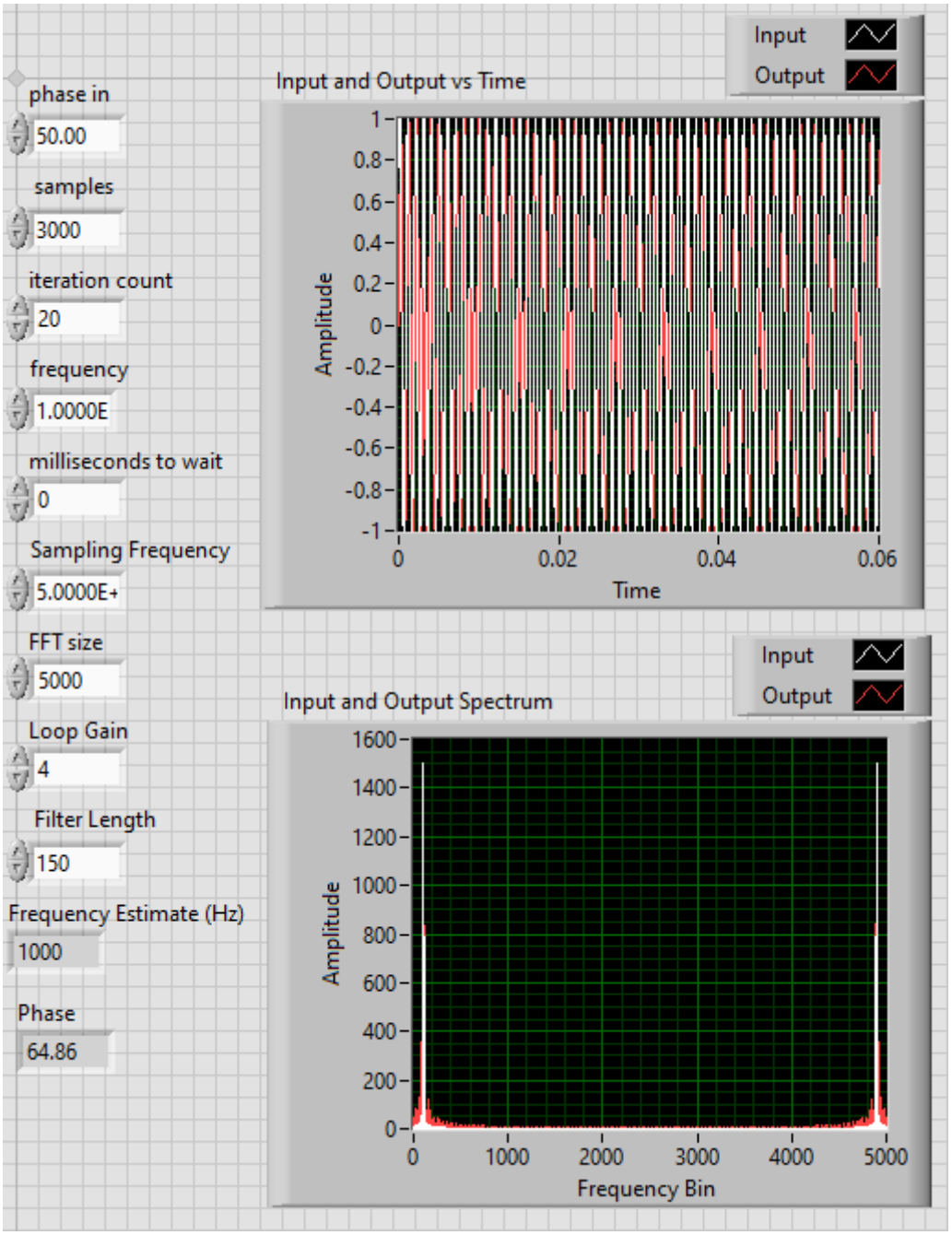

Figure 11: Input and locked waveforms for a loop gain where PLL in not locked, which is 4

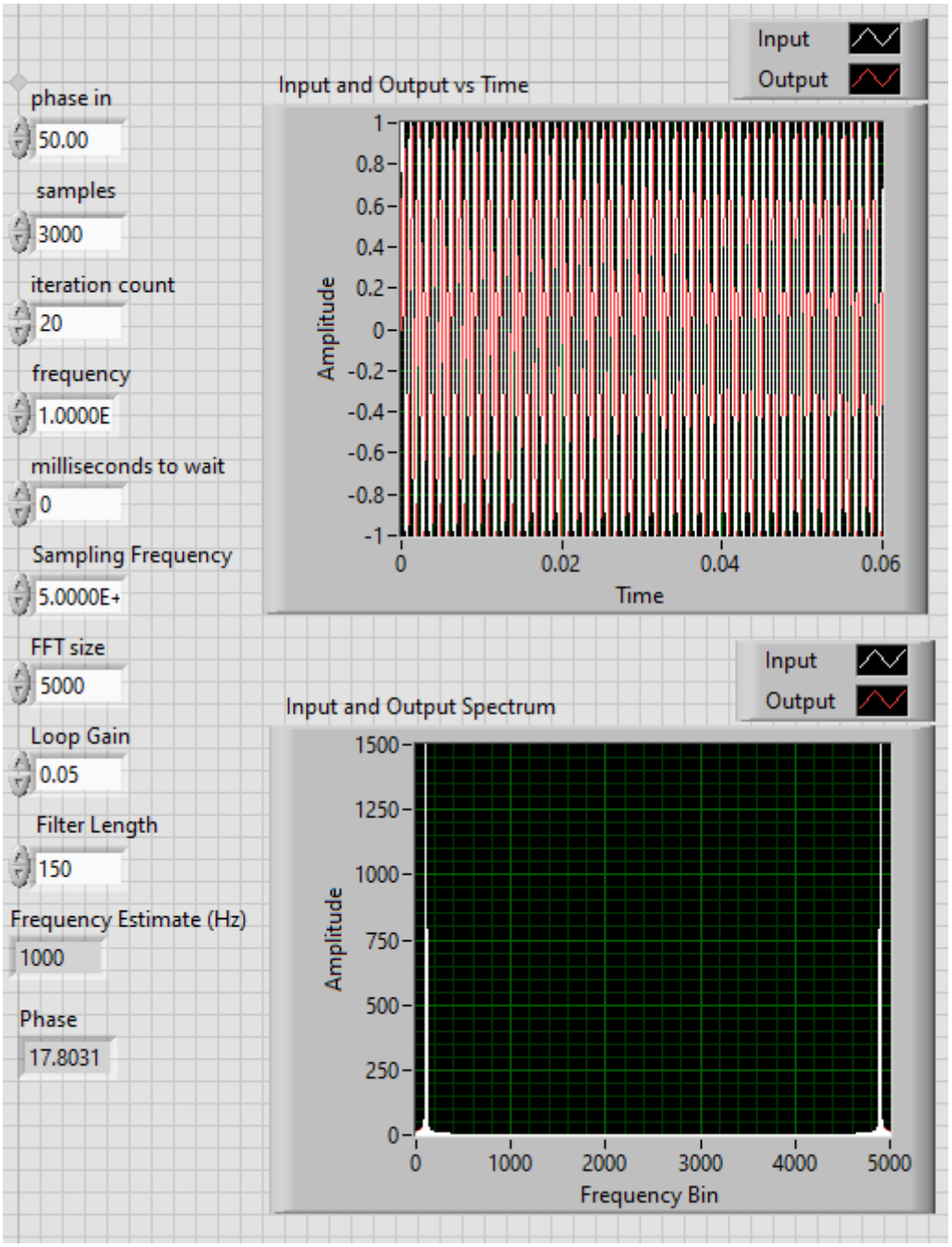

Figure 12: Input and locked waveforms for a loop gain of 0.05

j) Explain your frequency estimation method. What can you say about the frequency estimation method optimality?

For our estimation method, we take FFT of the signal with a certain FFT size. By taking its max index, we determine the location of the frequency and then multiplying that number with Sampling Frequency/FFT size, we find an estimate for frequency in Hertz. There are several factors determining optimality such as FFT size, the type of the signal, and Additive White Gaussian Noise.

- **With increasing FFT size, the estimated frequency is getting better and better. The reason behind this is increasing frequency resolution with increasing DFT length as the DFT is the samples of frequency spectrum and with more samples the maximum error decreases.**

- **If the type of the signal is not pure sinusoidal, this method will fail. For example, for a square wave, it is not a valid approach, since it has multiple peaks and finding the highest is not helpful.**

- **Additive White Gaussian Noise: If the SNR is not high enough the peak frequency value might change due to the AWGN and the system will not produce useful outputs as the operation assumes that the frequency of the sinusoid has the highest magnitude in the spectrum. With high SNR the peak value will not be changed and the VCO will lock to the original signal without any problems.**