

Homework #3

(Deadline: 11:59PM PDT, Tuesday, Mar 3, 2020)

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INSTRUCTIONS

This homework is to be done individually. You may use any tools or refer to published papers or books, but may not seek help from any other person or consult solutions to prior exams or homeworks from this or other courses (including those outside UCLA). You're allowed to make use of tools such as Logisim, WolframAlpha (which has terrific support for boolean logic) etc.

You must submit all sheets in this file based on the procedure below. Because of the grading methodology, it is much easier if you print the document and answer your questions in the space provided in this problem set. It can be even easier if you answer in electronic form and then download the PDF. Answers written on sheets other than the provided space will not be looked at or graded. Please write clearly and neatly - if we cannot easily decipher what you have written, you will get zero credit.

SUBMISSION PROCEDURE: You need to submit your solution online at Gradescope (<https://gradescope.com/>). Please see the following guide from Gradescope for submitting homework. You'd need to upload a PDF and mark where each question is answered.

http://gradescope-static-assets.s3-us-west-2.amazonaws.com/help/submitting_hw_guide.pdf

Problem #1 [30 points]

You are to design a **Mealy** finite state machine by **drawing the state diagram** that implements a routing algorithm. The goal is to go from South to North on a conceptually infinite grid via a series of intersections. Assume that upon reset, *rst*, the "car" is on a South-most grid intersection. The "car" accepts 3-bit input and produces 3-bit output. The 3 input bits, *blked*[2:0] = {*blockLeft*, *blockStraight*, *blockRight*} indicates whether the directions to the left, straight, and right (from the perspective of the entry point) is blocked. For instance, {1,1,1} indicates all paths are blocked, {1,0,1} indicates only the straight path is open, etc. The 3 output bits, *heading*[2:0] = {*goLeft*, *goStraight*, *goRight*} indicate which direction to go, left, straight and right respectively, and *heading* is 1-hot encoded. The exception for the one-hot encoding is {0,0,0} which indicates Wait at the junction due to blockage. The goal is to move whenever a path exists to the North, East, or West, (so that any cars behind you does not get backed up), and to move North whenever possible (regardless of how much to the left or right the car moves on the grid). So, when North is blocked, you should move to the West if possible and if West is blocked to head East (Note that we prioritize the heading direction to constrain the design). When heading East or West, the "car" should try to return heading North as soon as possible. You should never head South and cannot head backwards. You should Wait until another direction is clear if desired directions are blocked. Build this FSM with as few states as possible and explain your thinking.

Answer the question in the space below.

- reset(*rst*) car is on a South-most grid intersection
- 3 bit input *blked*[2:0] = {*bL*, *bS*, *bR*}
- 3 bit output *heading*[2:0] = {*gL*, *gS*, *gR*} {0,0,0} = wait
- main goal is North, second West if N blked, 3rd East
- When going E or W, car should try returning to N
- never head S & never backwards
- wait till clear if all dir are blked

My design originally consisted of 3 states N, W, E, but I then realized I may need an initial state depending on what reset is supposed to do. If reset must put the "car" on a South-most grid intersection relative to the previous path, then a 4th state is needed. Upon reflection, I've realized a 4th state is unnecessary, as reset means the car only has to be facing North in order to be "South-most", as this is an infinite grid.

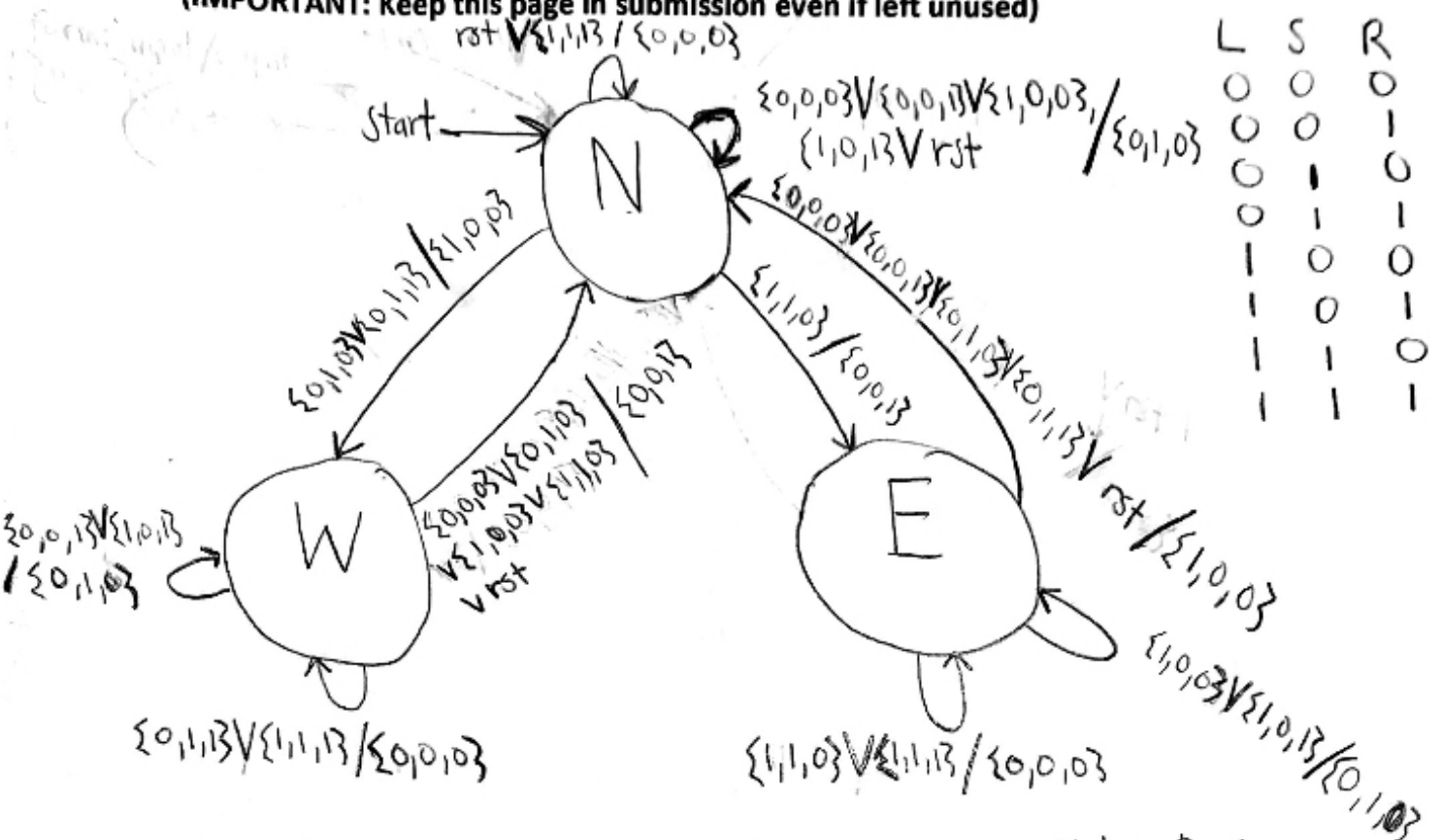
input = blk_d[2:0] → format: { blk[2:0], √{ blk[2:0]_{2,...} } / { heading[2:0] }

. output = heading[2:0] inputs / output

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This design keeps the absolute direction as stated & the inputs consist of the relative directions. The priority is to move North, then West, then East and if the only possible movement is South or backward then the car will wait. If there's no possible movement, obviously the car will wait. So, whenever you're going East and you can go left, do that so you will be facing North. Same goes for when you're facing West and right is open.

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Problem #2 [35 points]

A state transition table is shown below (st: state; nx_st: next_state). The inputs are max, goU and goD; the output is op.

| st | max | goU | goD | op | nx_st |
|-----|-----|-----|-----|----|-------|
| ID | X | 1 | 0 | 0 | UPF |
| ID | X | 0 | 1 | 0 | DNF |
| ID | X | 0 | 0 | 0 | ID |
| UPF | 0 | X | X | 1 | OPU |
| UPF | 1 | X | X | 1 | OPD |
| DNF | 0 | X | X | 1 | OPD |
| DNF | 1 | X | X | 1 | OPU |
| OPU | X | 0 | 0 | 0 | ID |
| OPU | X | 1 | 0 | 0 | UPF |
| OPU | X | 0 | 1 | 0 | DNF |
| OPD | X | 0 | 0 | 0 | ID |
| OPD | X | 1 | 0 | 0 | UPF |
| OPD | X | 0 | 1 | 0 | DNF |

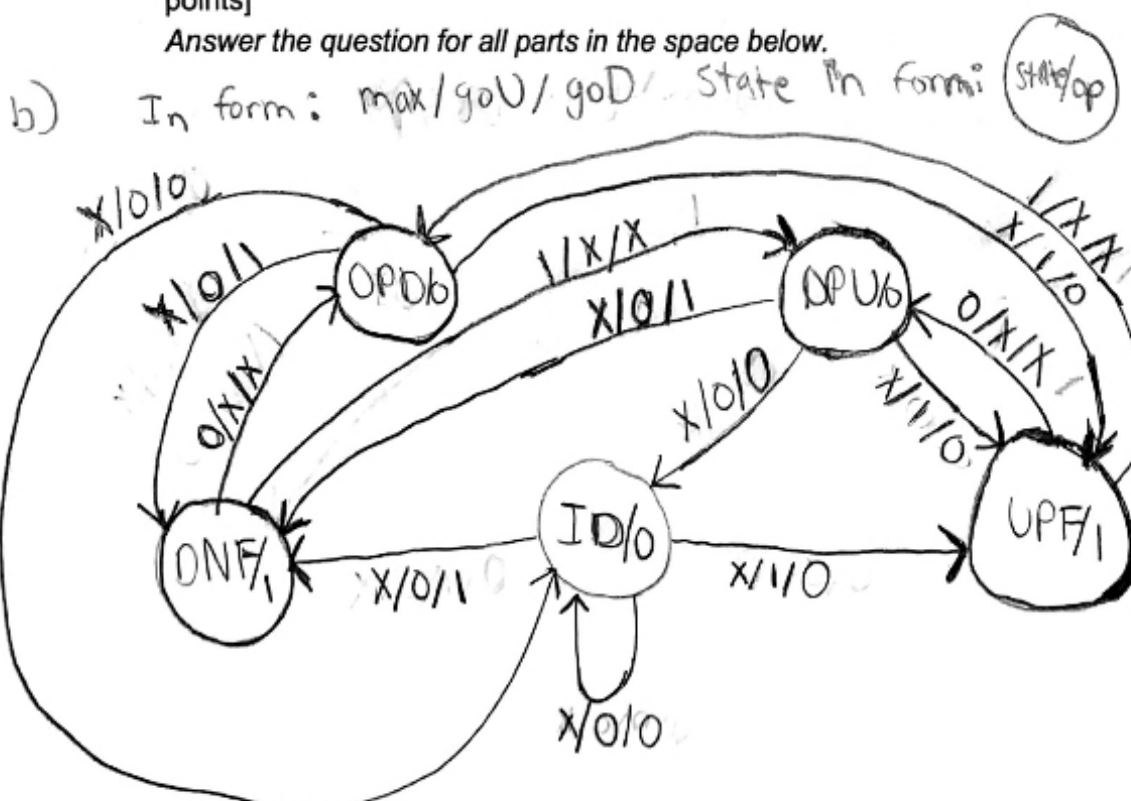
(a) Is this a Mealy or Moore FSM? [5 points]

Moore, since only state is needed to get op.

(b) Draw the state diagram for this. [15 points]

(c) We encode states with one-hot encoding where $ID:st[4:0] = 5'b00001$, $UPF:st[4:0] = 5'b00010$, $DNF:st[5:0] = 5'b00100$, $OPU:st[5:0] = 5'b01000$, and $OPD:st[5:0] = 5'b10000$. Note that state ID is essentially the assertion of $st[0]$, i.e., $state = ID$ iff $st[0] = 1$. Write the logic for the output signal, op . Write the logic for the transitions to state ID ($nx_st[0]$), and state UPF ($nx_st[1]$). [15 points]

Answer the question for all parts in the space below.



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c) $\text{state} = \text{ID} \text{ iff } \text{st}[0] = \text{VUF} \text{ iff } \text{st}[1] = \text{DNF} \text{ iff } \text{st}[2] = \text{OPU} \text{ iff } \text{st}[3] = \text{OPD} \text{ iff } \text{st}[4]$

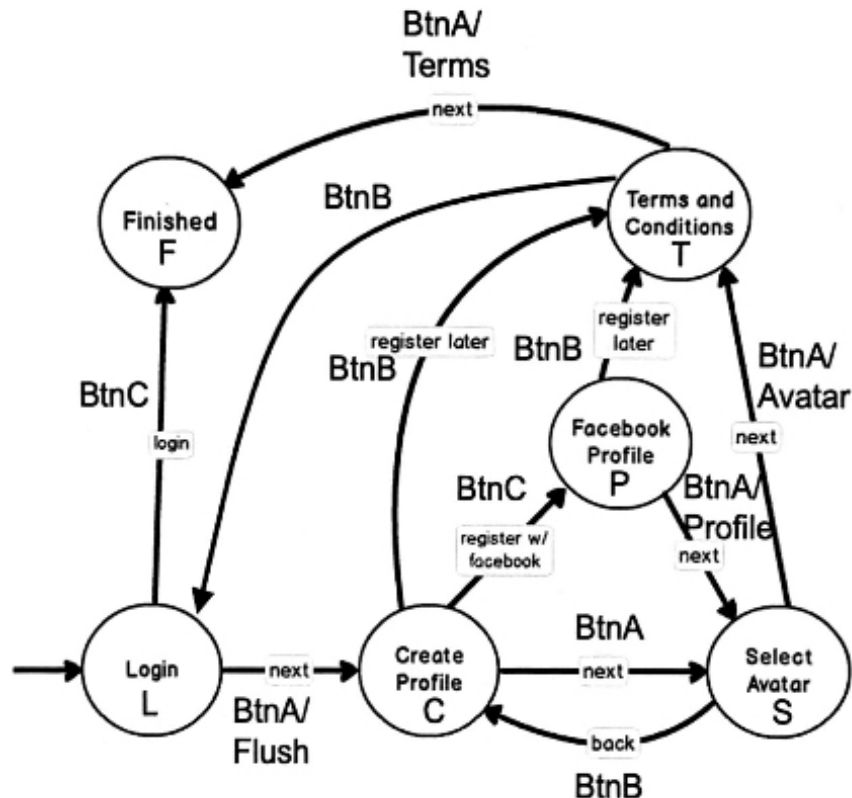
$$\text{op} = \text{st}[1] \vee \text{st}[2]$$

$$\text{nx_st}[0] = (\neg \text{goU}) \wedge (\neg \text{goD})$$

$$\text{nx_st}[1] = (\text{goU}) \wedge (\neg \text{goD})$$

Problem #3 [35 points]

State machines come in many forms. Software FSMs are extremely common. We can implement any software FSMs in hardware and vice versa. Below is such an example for a user interface. This interface for a registration page is implemented as a Mealy state machine. For the hardware implementation, we accept 3 button inputs $\{BtnA, BtnB, BtnC\}$ and only one of the buttons are asserted to 1'b1 at one time or all are zeros. For inputs not shown on the arcs, the assumption should be that the state feeds back to itself. There are 4 outputs that are asserted to 1'b1 only on specific arcs $\{Terms, Profile, Avatar, Flush\}$. On all other arcs, the outputs are zeros.



- Draw the State Transition Table for this state machine. You can simplify the table size by noting that only one input can be asserted at any time. [15 points]
- If the 6 states are binary encoded into 3 bits, $state[2:0]$, $\{L, C, S, P, T, F\} = \{3'b000, 3'b001, 3'b010, 3'b011, 3'b100, 3'b101\}$, determine the logic for the output Profile, and Avatar based on input and/or state. [15 points]
- With the same assumption as (b), write the logical expression for the $next_state[0]$ as a minimal sum-of-products. You can use symbols (e.g., BtnA, L, C, S). [5 points]

Answer the question for all parts in the space below.

6 states, 3 inputs (one hot)

Input format: since only one button can be asserted at a time, stating
 BtnA implies $\{1,0,0\}$, BtnB implies $\{0,1,0\}$, BtnC implies $\{0,0,1\}$, while 0 implies $\{0,0,0\}$

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| a) | state | input | output | next state |
|----|-----------------------|--------------|--------|------------|
| | Login (L) | BtnA = '1'b1 | 1 | C • |
| | Login (L) | BtnB = '1'b1 | 0 | L |
| | Login (L) | BtnC = '1'b1 | 0 | F • |
| | Login (L) | 0 | 0 | L |
| | Create Profile (C) | BtnA = '1'b1 | 0 | S |
| | Create Profile (C) | BtnB | 0 | T |
| | Create Profile (C) | BtnC | 0 | P • |
| | Create Profile (C) | 0 | 0 | C • |
| | Select Avatar (S) | BtnA | 1 | T |
| | S | BtnB | 0 | C • |
| | S | BtnC | 0 | S |
| | S | 0 | 0 | S |
| | Terms & Condition (T) | BtnA | 1 | F • |
| | T | BtnB | 0 | L |
| | T | BtnC | 0 | T |
| | T | 0 | 0 | T |
| | Facebook Post (P) | BtnA | 1 | S |
| | P | BtnB | 0 | T |
| | P | BtnC | 0 | P • |
| | P | 0 | 0 | P • |

b)

Profile = $\neg \text{state}[2] \wedge \text{state}[1] \wedge \text{state}[0] \wedge \text{BtnA}$

Avatar = $\neg \text{state}[2] \wedge \text{state}[1] \wedge \neg \text{state}[0] \wedge \text{BtnA}$

BtnA = $\{1,0,0\}$ as input
 where BtnA = '1'b1, BtnB = '1'b0, BtnC = '1'b0

c) next state[0] = $C(\neg \text{BtnA})(\neg \text{BtnB})(\neg \text{BtnC}) + P(\neg \text{BtnA})(\neg \text{BtnB})(\text{BtnC})$

★
 4/2

$L(\text{BtnA}) + L(\text{BtnC}) + C(\text{BtnC}) + S(\text{BtnB}) + T(\text{BtnA}) + P(\text{BtnC})$

$= C(\neg \text{BtnA})(\neg \text{BtnB}) + P(\neg \text{BtnA})(\neg \text{BtnB}) + S(\text{BtnB}) + T(\text{BtnA}) + L(\text{BtnA}) + L(\text{BtnC})$

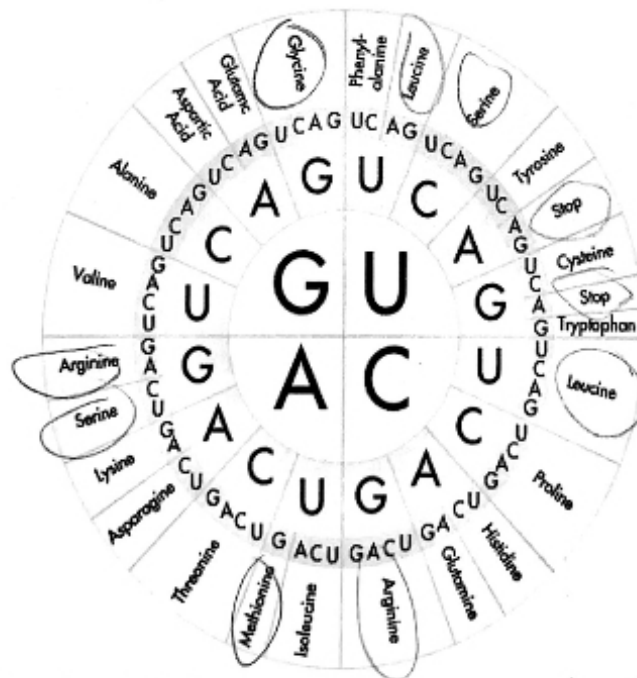
★ Profile

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1) $\text{ReLU}(x) = \max(0, x)$

[Extra] Problem #4 [+10 points]

Recall the nucleotides in Homework #1 and #2. The translation of a messenger RNA into amino acid is actually not done by looking at 3 nucleotides at once (as we had done in previously) but rather done sequentially where each nucleotide enters a machine. Again, the nucleotides are represented as 2-bit binary digits. $G=2'b00$, $C=2'b11$, $A=2'b10$, and $U=2'b01$. There are 23 possible amino acids can be identified and are represented as 5-bit binary. A graph of the composition of these amino acids is shown below. There are 2 special amino acids, Methionine and Stop. You are to design a **Moore FSM** by drawing the state transition diagram that can identify a subset of these amino acids. The state machine starts in an initial set of states that is looking for Methionine. After Methionine is detected, it cycles through more states to identify other amino acids. The machine returns to its initial set of states when it detects a Stop codon. Instead of identifying all 20 of the remaining amino acids, we will simplify the design to only detect *Glycine*, *Leucine*, *Serine*, and *Arginine* (note that many of these occur with multiple possible codes). The input to the machine is 2 bits indicating the nucleotide that is arriving every cycle. The outputs are 4 signals, *gly*, *leu*, *ser*, and *arg*, that are asserted when the proper sequence is detected. Design this as a Moore state machine.



Answer the question for all parts in the space below.

Input: 2 bit nucleotide
Output: 4 sig: gly, leu, ser, arg

Stop: UAA, UAG, UGA

Methionine: AUG

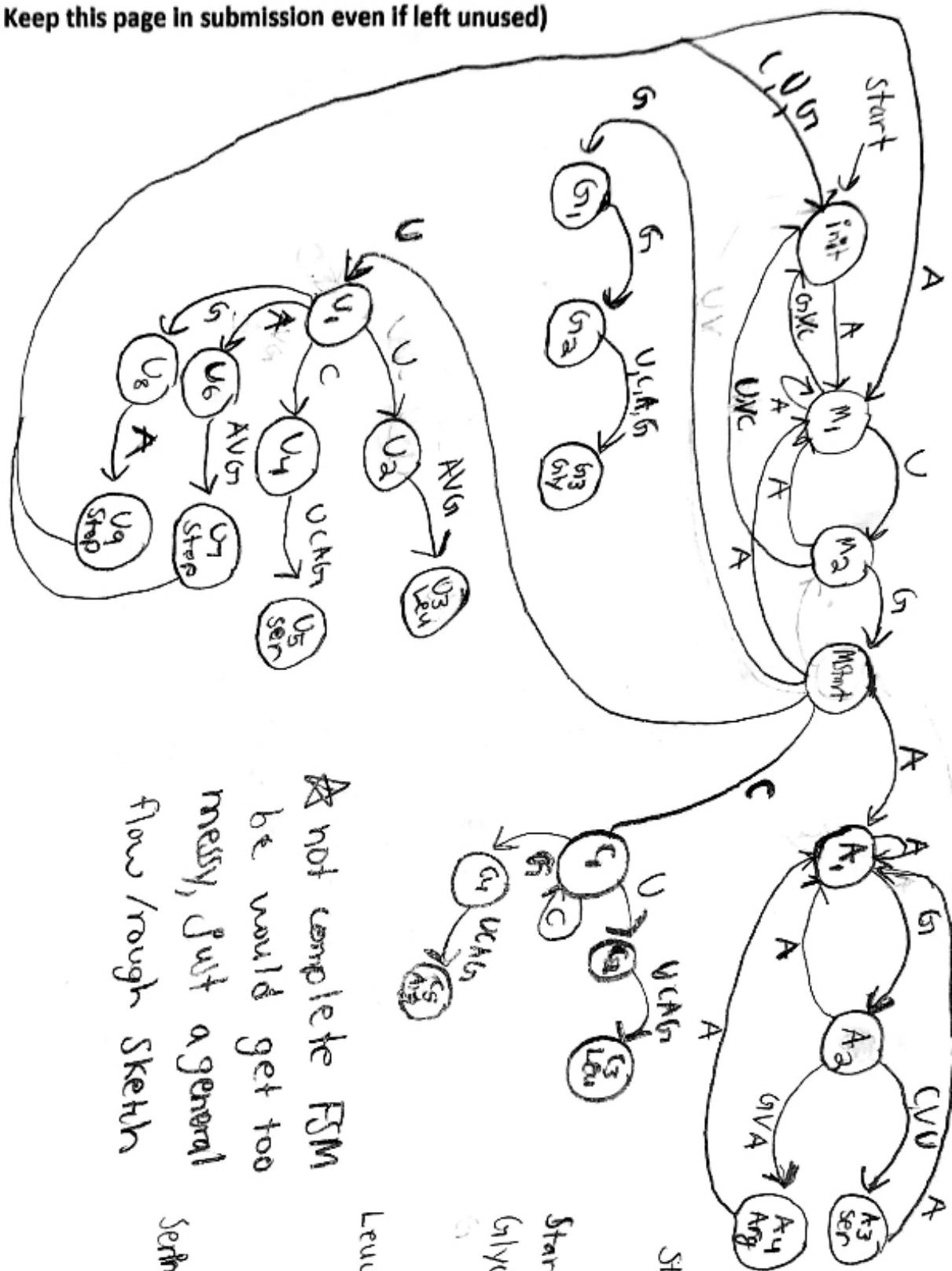
Glycine: GGU, GGC, GGA, GGG

Leucine: CUU, CUC, CUA, CUG, UUA, UUG

Serine: UCU, UCC, UCA, UCG, AGC, AGU

Arginine: CGU, CGC, CGA, CGG, AGG, AGA

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★ not complete FSM
be would get too
messy, just a general
flow/rough sketch

Stop: UAA

Start: A06

Only ydne:

5

Leucone:

Serine:

Arginine:

UAA
UAG
UGA
AU
GAU
GGU
GGA
GAA
CUU
CUC
CUA
CUU
UUA
UUG
UCU
UCC
UCA
UCG
AGC
AGU
AGU
CGU
CGU
CGA
CGA
AAG
AAG
AAG

Input: $A = 2'b10, C = 2'b11, G = 2'b00, U = 2'b01$

Output: $\{gly, leu, ser, arg\}$, not dependent on input since Moore FSM

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output not dependent on input

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only on State

| State | Input | Output | Next State | State | Input | Output | Next State |
|----------------|-------|-----------|----------------|----------------|-------|-----------|----------------|
| Init | A | {0,0,0,0} | M ₁ | V ₁ | A | {0,0,0,0} | V ₆ |
| Init | C | | Init | U ₁ | C | | U ₄ |
| Init | G | | Init | U ₁ | G | | U ₈ |
| Init | U | | Init | U ₁ | U | | U ₂ |
| M ₁ | A | {0,0,0,0} | M ₁ | U ₂ | A | {0,0,0,0} | U ₃ |
| M ₁ | C | | Init | U ₂ | C | | C ₁ |
| M ₁ | G | | Init | U ₂ | G | | U ₃ |
| M ₁ | U | | M ₂ | U ₂ | U | | U ₄ |
| M ₂ | A | {0,0,0,0} | M ₁ | U ₃ | A | {0,1,0,0} | A ₁ |
| M ₂ | C | | Init | U ₃ | C | | C ₁ |
| M ₂ | G | | MStart | U ₃ | G | | G ₁ |
| M ₂ | U | | Init | U ₃ | U | | U ₁ |
| MStart | A | {0,0,0,0} | A ₁ | U ₄ | A | {0,0,0,0} | U ₅ |
| MStart | C | | C ₁ | U ₄ | C | | U ₅ |
| MStart | G | | G ₁ | U ₄ | G | | U ₅ |
| MStart | U | | U ₁ | U ₄ | U | | U ₅ |
| A ₁ | A | {0,0,0,0} | A ₁ | U ₅ | A | {0,0,1,0} | A ₁ |
| A ₁ | C | | C ₁ | U ₅ | C | | C ₁ |
| A ₁ | G | | A ₂ | U ₅ | G | | G ₁ |
| A ₁ | U | | U ₁ | U ₅ | U | | U ₁ |
| A ₂ | A | {0,0,0,0} | A ₄ | U ₆ | A | {0,0,0,0} | U ₇ |
| A ₂ | C | | A ₃ | U ₆ | C | | C ₁ |
| A ₂ | G | | A ₄ | U ₆ | G | | U ₇ |
| A ₂ | U | | A ₃ | U ₆ | U | | U ₁ |
| A ₃ | A | {0,0,1,0} | A ₁ | U ₇ | A | {0,0,0,0} | M ₁ |
| A ₃ | C | | C ₁ | U ₇ | C | | Init |
| A ₃ | G | | G ₁ | U ₇ | G | | Init |
| A ₃ | U | | U ₁ | U ₇ | U | | Init |
| A ₄ | A | {0,0,0,1} | A ₁ | U ₈ | A | {0,0,0,0} | U ₉ |
| A ₄ | C | | C ₁ | U ₈ | C | | C ₁ |
| A ₄ | G | | G ₁ | U ₈ | G | | G ₁ |
| A ₄ | U | | U ₁ | U ₈ | U | | U ₁ |

| State | Input | Output | Next State | State | Input | Output | Next State |
|----------------|-------|-----------|----------------|----------------|-------|-----------|----------------|
| U _q | A | | M ₁ | C ₄ | A | | C ₅ |
| U _q | C | {0,0,0,0} | Init | C ₄ | C | {0,0,0,0} | C ₅ |
| U _q | G | | Init | C ₄ | G | | C ₅ |
| U _q | U | | Init | C ₄ | U | | C ₅ |
| G ₁ | A | | A ₁ | C ₅ | A | | A ₁ |
| G ₁ | C | {0,0,0,0} | C ₁ | C ₅ | C | {0,0,0,1} | C ₁ |
| G ₁ | G | | G ₂ | C ₅ | G | | G ₁ |
| G ₁ | U | | U ₁ | C ₅ | U | | U ₁ |
| G ₂ | A | | G ₃ | | | | |
| G ₂ | C | {0,0,0,0} | G ₃ | | | | |
| G ₂ | G | | G ₃ | | | | |
| G ₂ | U | | G ₃ | | | | |
| G ₃ | A | | A ₁ | | | | |
| G ₃ | C | {1,0,0,0} | C ₁ | | | | |
| G ₃ | G | | G ₁ | | | | |
| G ₃ | U | | U ₁ | | | | |
| C ₁ | A | | A ₁ | | | | |
| C ₁ | C | {0,0,0,0} | C ₁ | | | | |
| C ₁ | G | | C ₄ | | | | |
| C ₁ | U | | C ₂ | | | | |
| C ₂ | A | | C ₃ | | | | |
| C ₂ | C | {0,0,0,0} | C ₃ | | | | |
| C ₂ | G | | C ₃ | | | | |
| C ₂ | U | | C ₃ | | | | |
| C ₃ | A | | A ₁ | | | | |
| C ₃ | C | {0,1,0,0} | C ₁ | | | | |
| C ₃ | G | | G ₁ | | | | |
| C ₃ | U | | U ₁ | | | | |
| | | | | | | | |