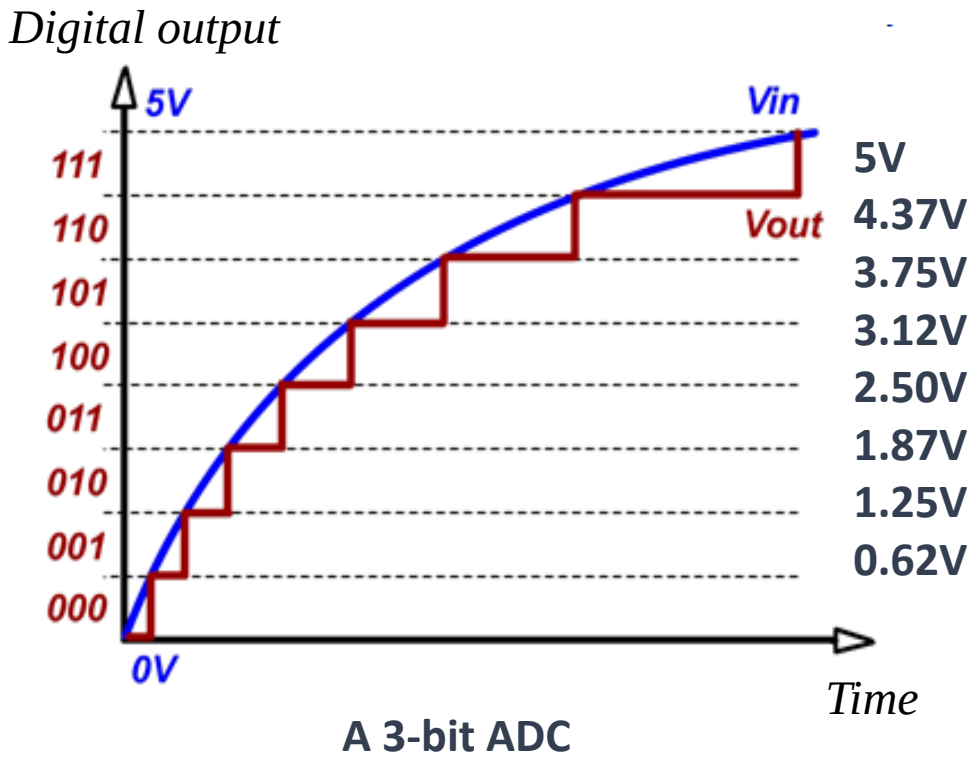
CENG 336
INT. TO EMBEDDED SYSTEMS DEVELOPMENT
Spring 2022-2023
Recitation-3

OUTLINE

- ADC (Analog-to-Digital Converter)
- XC8 C Compiler Data Types
- LCD

A/D CONVERSION



A 3-bit ADC

In real world:

ANALOG signals

(the sensors used to monitor real world produce analog continuous voltage signals)

↓ Converted by ADC

In computer world:

DIGITAL signals

A/D MODULE in PIC18F4620

- 13 Analog input channels
- 10-bit resolution
- Software selectable reference voltages
- Can operate in SLEEP mode using its own internal RC oscillator
- Can generate interrupts after the conversion
- Conversions can be initiated via both software and hardware

REGISTERS

- A/D Control Register0 (ADCON0)

  Controls the operation of the A/D module
- A/D Control Register1 (ADCON1)

  Configures the functions of the port pins
- A/D Control Register 2 (ADCON2)

  Configures the A/D clock source, programmed acquisition time and justification
- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)

ADCON0

REGISTER 19-1: ADCON0: A/D CONTROL REGISTER 0

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 1 **GO/$\overline{\text{DONE}}$:** A/D Conversion Status bit
When ADON = 1:
1 = A/D conversion in progress
0 = A/D Idle

bit 0 **ADON:** A/D On bit
1 = A/D Converter module is enabled
0 = A/D Converter module is disabled

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits
0000 = Channel 0 (AN0)
0001 = Channel 1 (AN1)
0010 = Channel 2 (AN2)
0011 = Channel 3 (AN3)
0100 = Channel 4 (AN4)
0101 = Channel 5 (AN5)(1,2)
0110 = Channel 6 (AN6)(1,2)
0111 = Channel 7 (AN7)(1,2)
1000 = Channel 8 (AN8)
1001 = Channel 9 (AN9)
1010 = Channel 10 (AN10)
1011 = Channel 11 (AN11)
1100 = Channel 12 (AN12)
1101 = Unimplemented)(2)
1110 = Unimplemented)(2)
1111 = Unimplemented)(2)

Note 1: These channels are not implemented on 28-pin devices.
2: Performing a conversion on unimplemented channels will return a floating input measurement.

ADCON1

REGISTER 19-2: ADCON1: A/D CONTROL REGISTER 1

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-q(1)	R/W-q(1)	R/W-q(1)
—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5 **VCFG1:** Voltage Reference Configuration bit (V_{REF-} source)
1 = V_{REF-} (AN2)
0 = V_{SS}

bit 4 **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)
1 = V_{REF+} (AN3)
0 = V_{DD}

ADCON1

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

PCFG3: PCFG0	AN12	AN11	AN10	AN9	AN8	AN7(2)	AN6(2)	AN5(2)	AN4	AN3	AN2	AN1	AN0
0000(1)	A	A	A	A	A	A	A	A	A	A	A	A	A
0001	A	A	A	A	A	A	A	A	A	A	A	A	A
0010	A	A	A	A	A	A	A	A	A	A	A	A	A
0011	D	A	A	A	A	A	A	A	A	A	A	A	A
0100	D	D	A	A	A	A	A	A	A	A	A	A	A
0101	D	D	D	A	A	A	A	A	A	A	A	A	A
0110	D	D	D	D	A	A	A	A	A	A	A	A	A
0111(1)	D	D	D	D	D	A	A	A	A	A	A	A	A
1000	D	D	D	D	D	D	A	A	A	A	A	A	A
1001	D	D	D	D	D	D	D	A	A	A	A	A	A
1010	D	D	D	D	D	D	D	D	A	A	A	A	A
1011	D	D	D	D	D	D	D	D	D	A	A	A	A
1100	D	D	D	D	D	D	D	D	D	D	A	A	A
1101	D	D	D	D	D	D	D	D	D	D	D	A	A
1110	D	D	D	D	D	D	D	D	D	D	D	D	A
1111	D	D	D	D	D	D	D	D	D	D	D	D	D

A = Analog input D = Digital I/O

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<2:0> = 000; when PBADEN = 0, PCFG<2:0> = 111.

2: AN5 through AN7 are available only on 40/44-pin devices.

ADCON2

REGISTER 19-3: ADCON2: A/D CONTROL REGISTER 2

R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	—	ACQT2	ACQT1	ACQT0	ADCS2	ADCS1	ADCS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADFM:** A/D Result Format Select bit
1 = Right justified
0 = Left justified

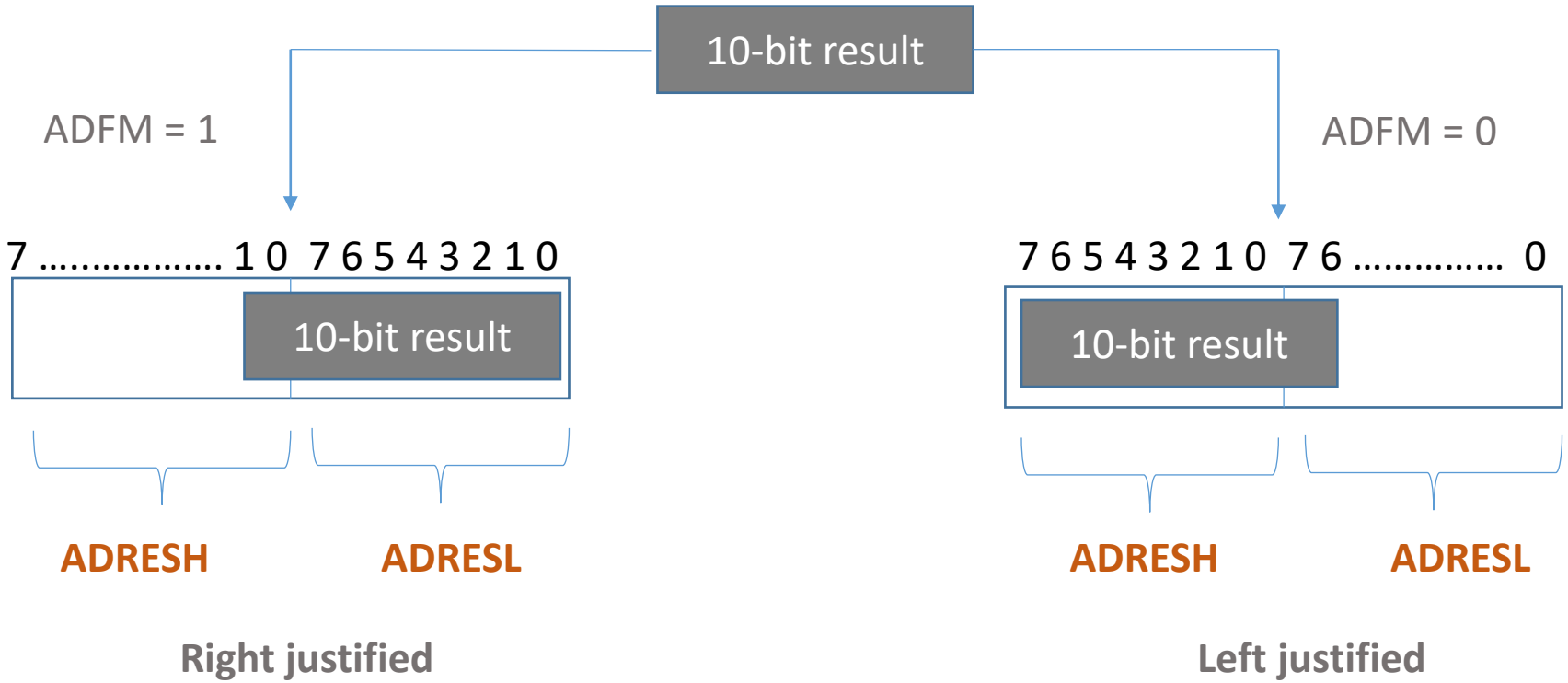
bit 6 **Unimplemented:** Read as '0'

bit 5-3 **ACQT2:ACQT0:** A/D Acquisition Time Select bits
111 = 20 TAD
110 = 16 TAD
101 = 12 TAD
100 = 8 TAD
011 = 6 TAD
010 = 4 TAD
001 = 2 TAD
000 = 0 TAD(1)

bit 2-0 **ADCS2:ADCS0:** A/D Conversion Clock Select bits
111 = FRC (clock derived from A/D RC oscillator)(1)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock derived from A/D RC oscillator)(1)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

Note 1: If the A/D FRC clock source is selected, a delay of one TCY (instruction cycle) is added before the A/D clock starts. This allows the SLEEP instruction to be executed before starting a conversion.

A/D CONVERSION RESULT

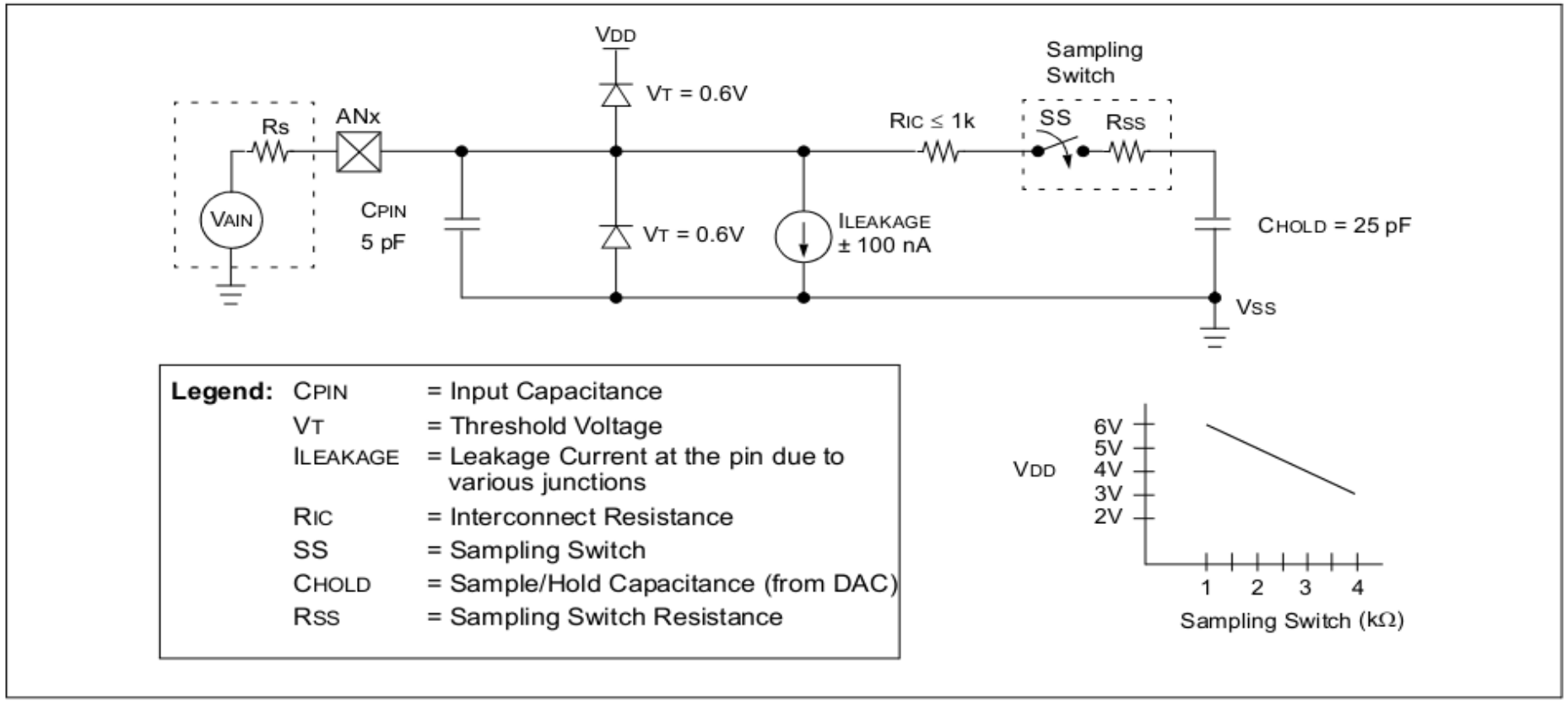


A/D MODULE OPERATION

- The analog input charges a sample and hold capacitor to get a stable input voltage for the conversion.
- The analog input is disconnected from the sample and hold capacitor to eliminate the wrong conversion results due to possible input voltage changes during the conversion.
- The output of the sample and hold capacitor is the input into the converter.
- The converter then generates a digital result of this analog level.

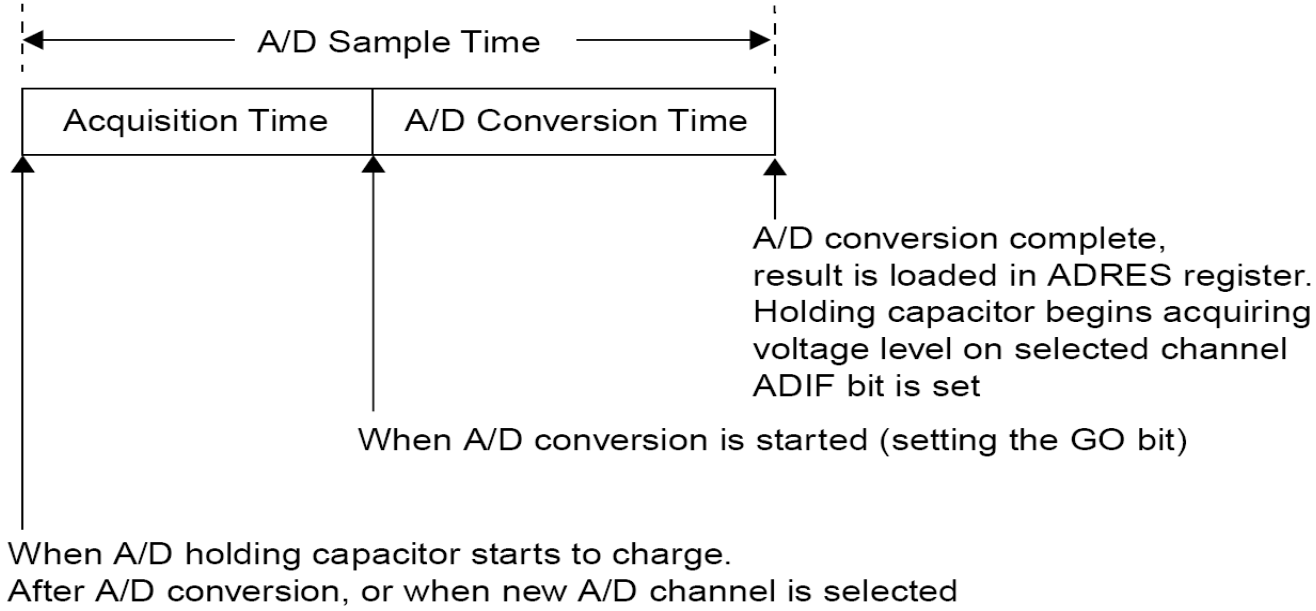
ANALOG INPUT MODEL

FIGURE 21-3: ANALOG INPUT MODEL



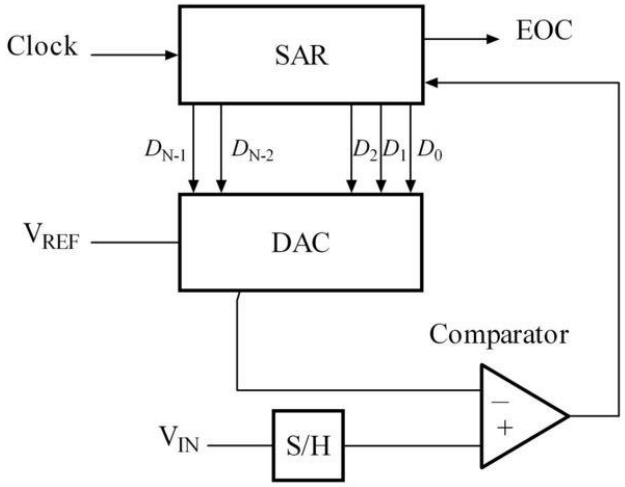
A/D ACQUISITION TIME REQ

There is a minimum acquisition time to ensure that the holding capacitor is charged to a level that will give the desired accuracy for the A/D conversion. Look at the data sheet for calculations.



PIC18F4620
SUCCESSIVE APPROXIMATION ADC

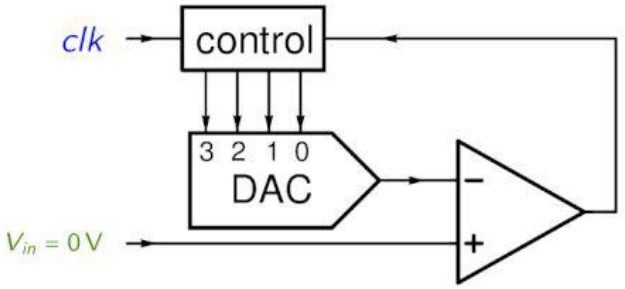
- The analog voltage level is converted to a digital value by performing iterative comparisons with a generated voltage reference value.
- In each iterative step, a different voltage level is tested and depending on the comparison result the corresponding step bit is set or reset.



DAC = digital-to-analog converter
EOC = end of conversion
SAR = successive approximation register
S/H = sample and hold circuit
V_{IN} = input voltage
V_{REF} = reference voltage

SUCCESSIVE APPROXIMATION ADC EXAMPLE - 1

Successive Approximation – example of a 4-bit ADC

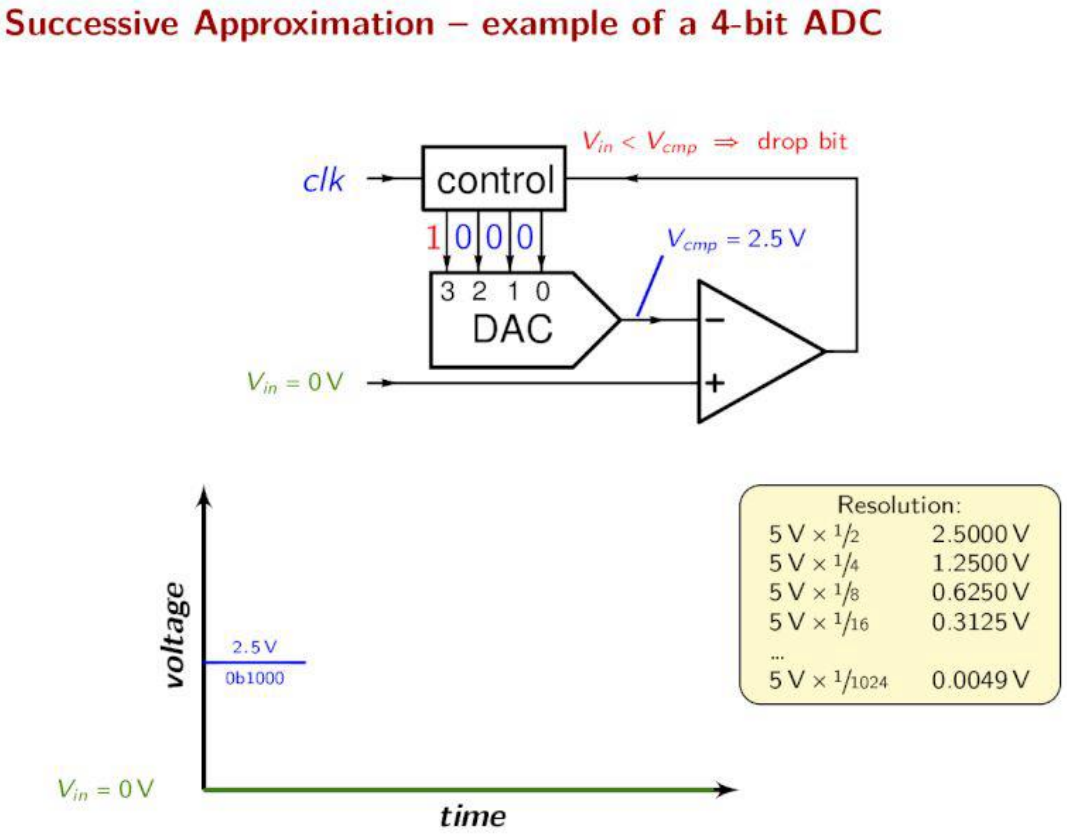


Resolution:	
5 V × 1/2	2.5000 V
5 V × 1/4	1.2500 V
5 V × 1/8	0.6250 V
5 V × 1/16	0.3125 V
...	
5 V × 1/1024	0.0049 V

Comparator outputs 1 when V+>V-, otherwise 0.

Reference: https://en.wikipedia.org/wiki/Successive-approximation_ADC

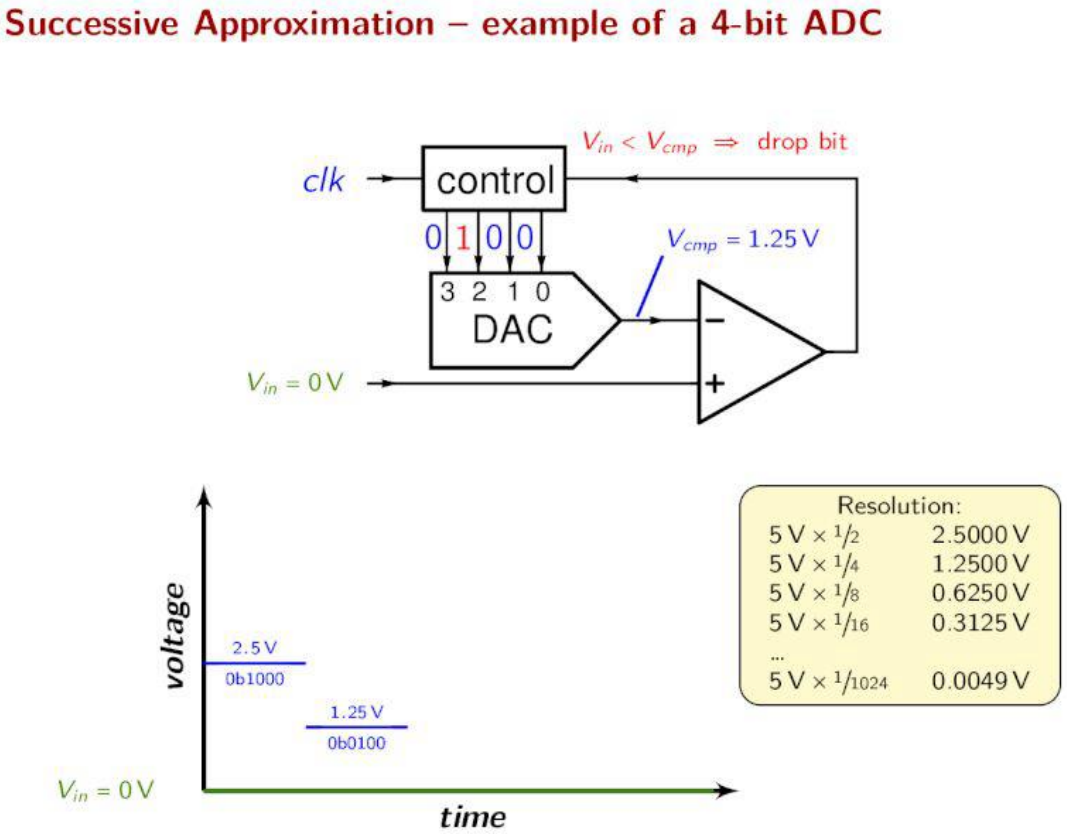
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 1



Comparator outputs 1 when V+>V-, otherwise 0.

Reference:
https://en.wikipedia.org/wiki/Successive-approximation_ADC

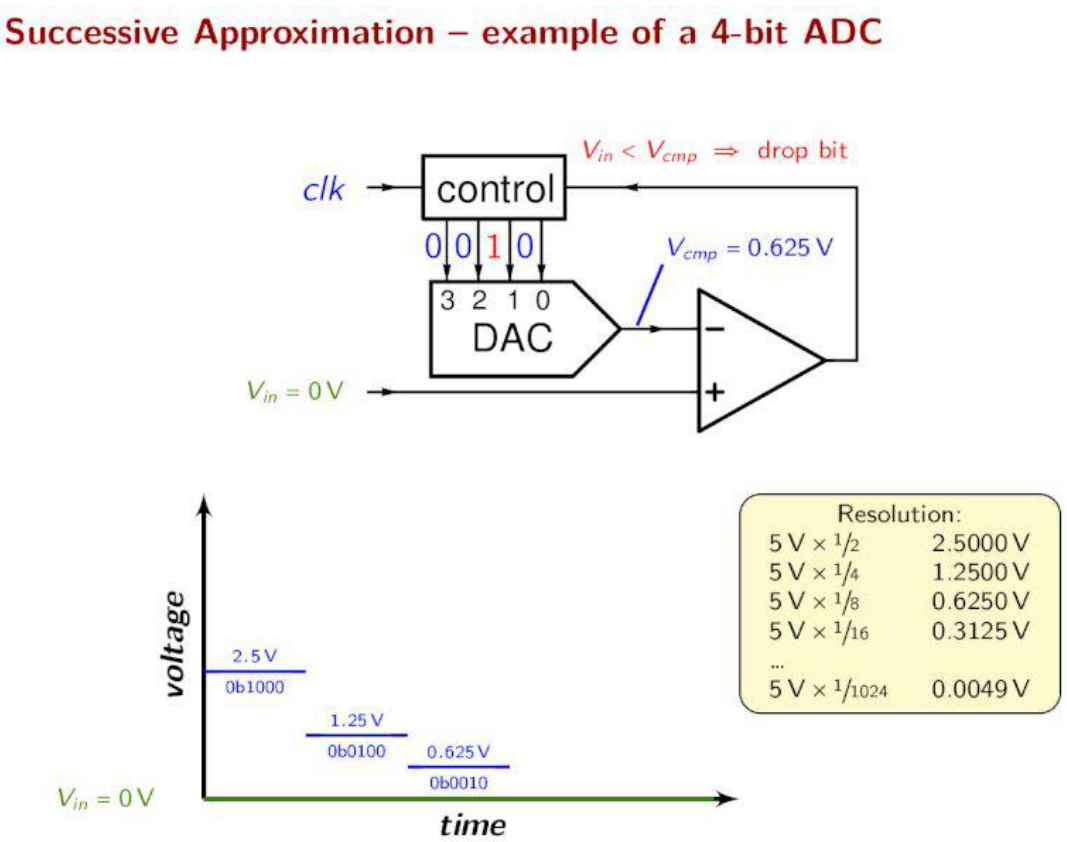
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 1



Comparator outputs 1 when V+>V-, otherwise 0.

Reference: https://en.wikipedia.org/wiki/Successive-approximation_ADC

SUCCESSIVE APPROXIMATION ADC EXAMPLE - 1



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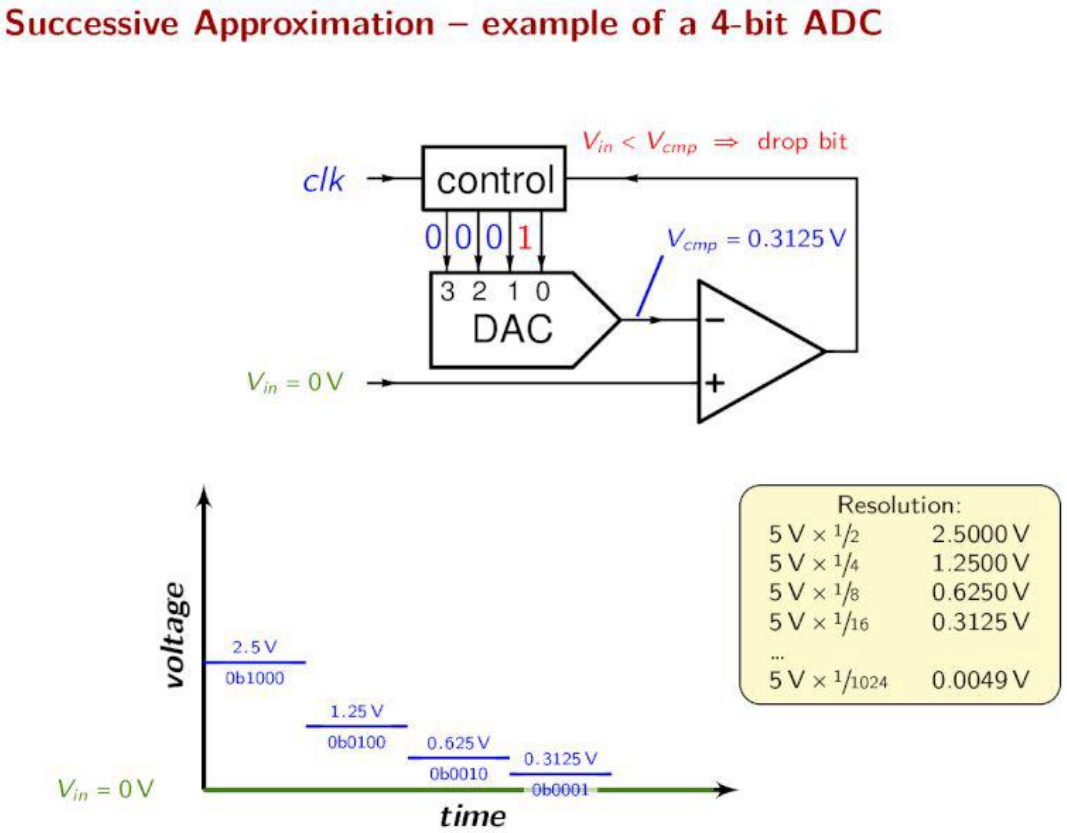
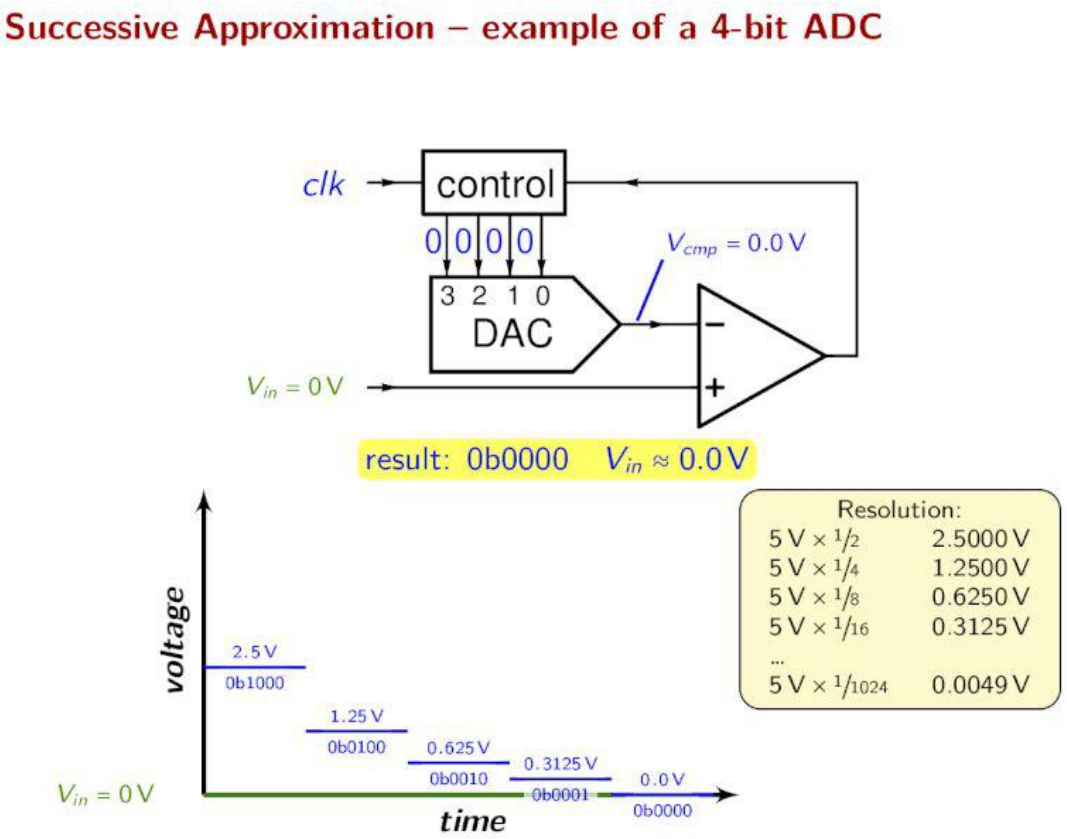
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 1



Comparator outputs 1 when V+>V-, otherwise 0.

Reference: https://en.wikipedia.org/wiki/Successive-approximation_ADC

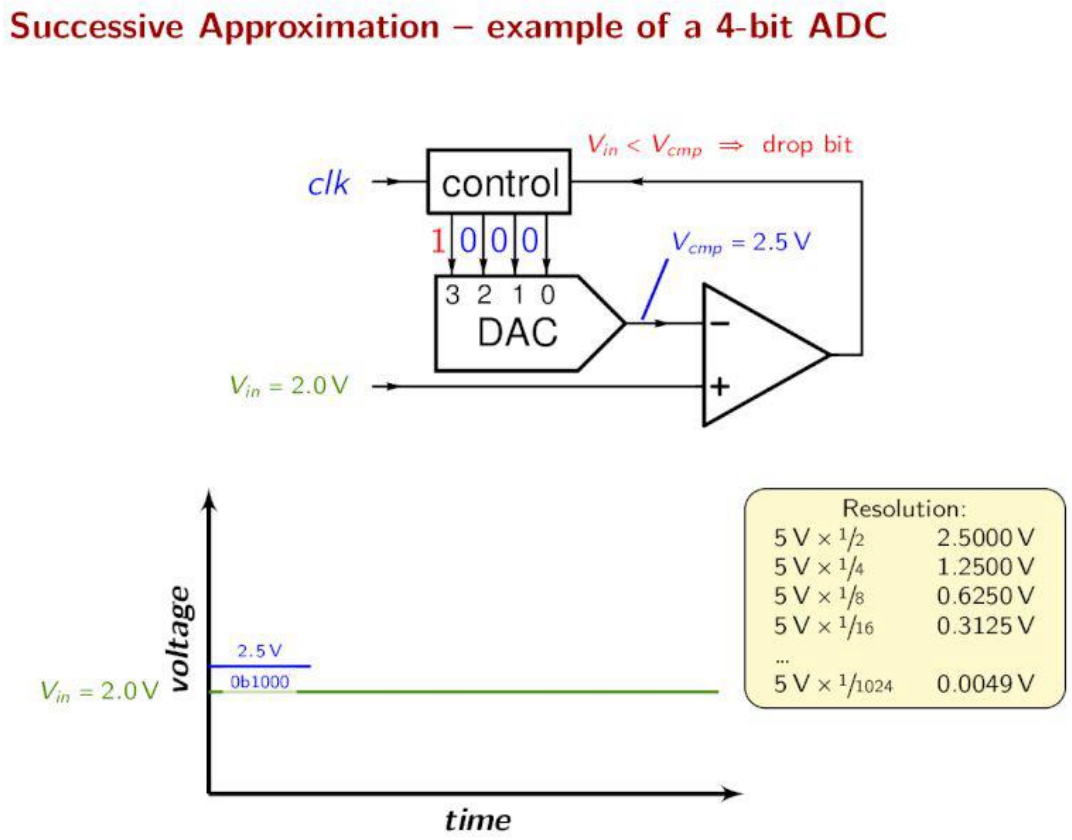
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 1



Comparator outputs 1 when V+>V-, otherwise 0.

Reference: https://en.wikipedia.org/wiki/Successive-approximation_ADC

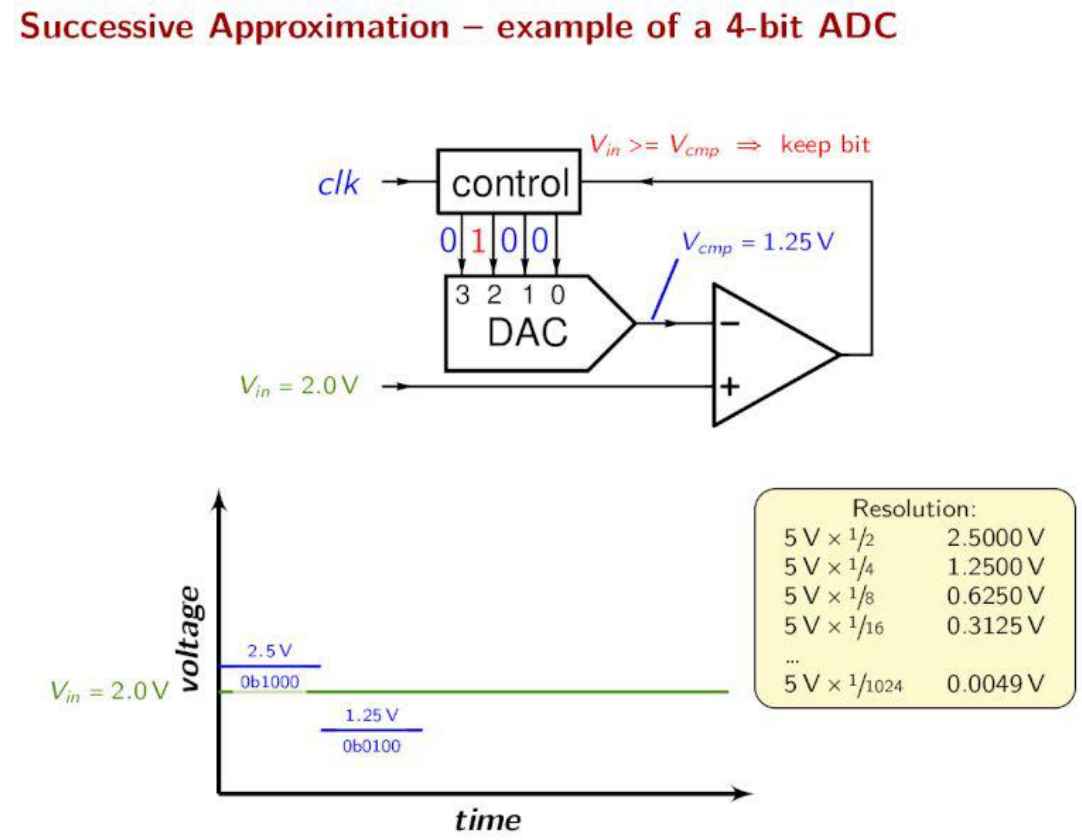
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 2



Comparator outputs 1 when V+>V-, otherwise 0.

Reference:
https://en.wikipedia.org/wiki/Successive-approximation_ADC

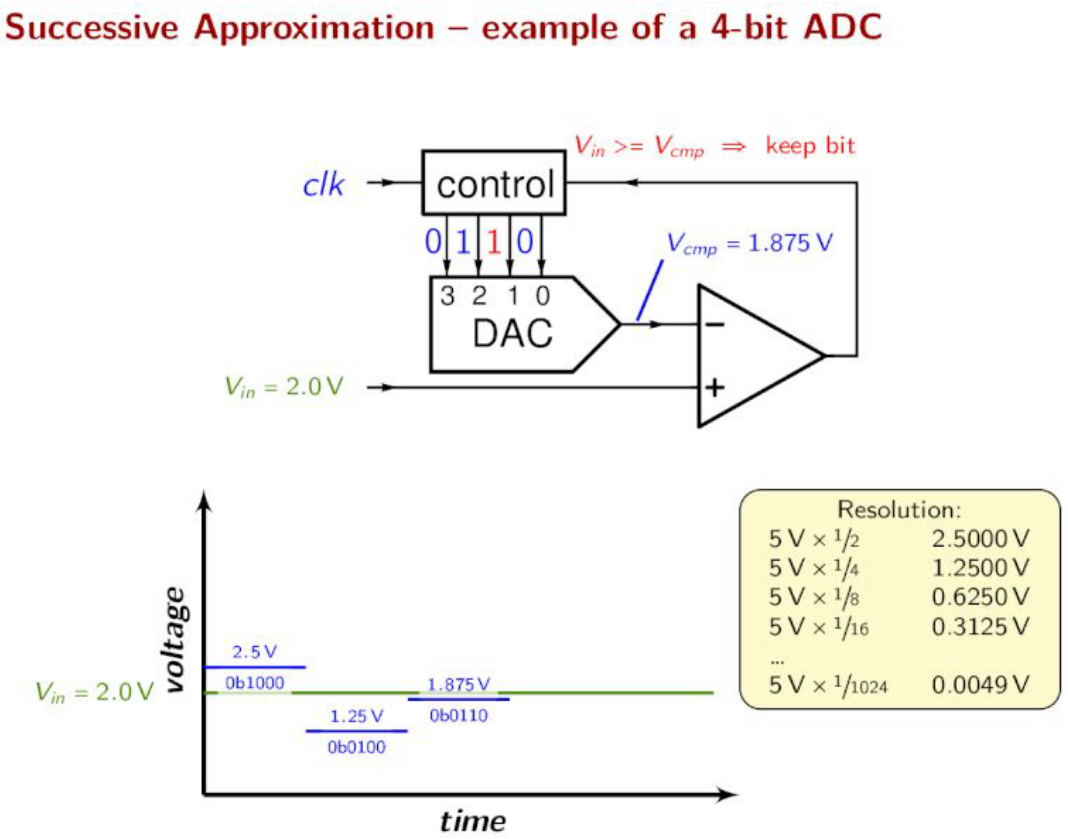
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 2



Comparator outputs 1 when V+>V-, otherwise 0.

Reference: https://en.wikipedia.org/wiki/Successive-approximation_ADC

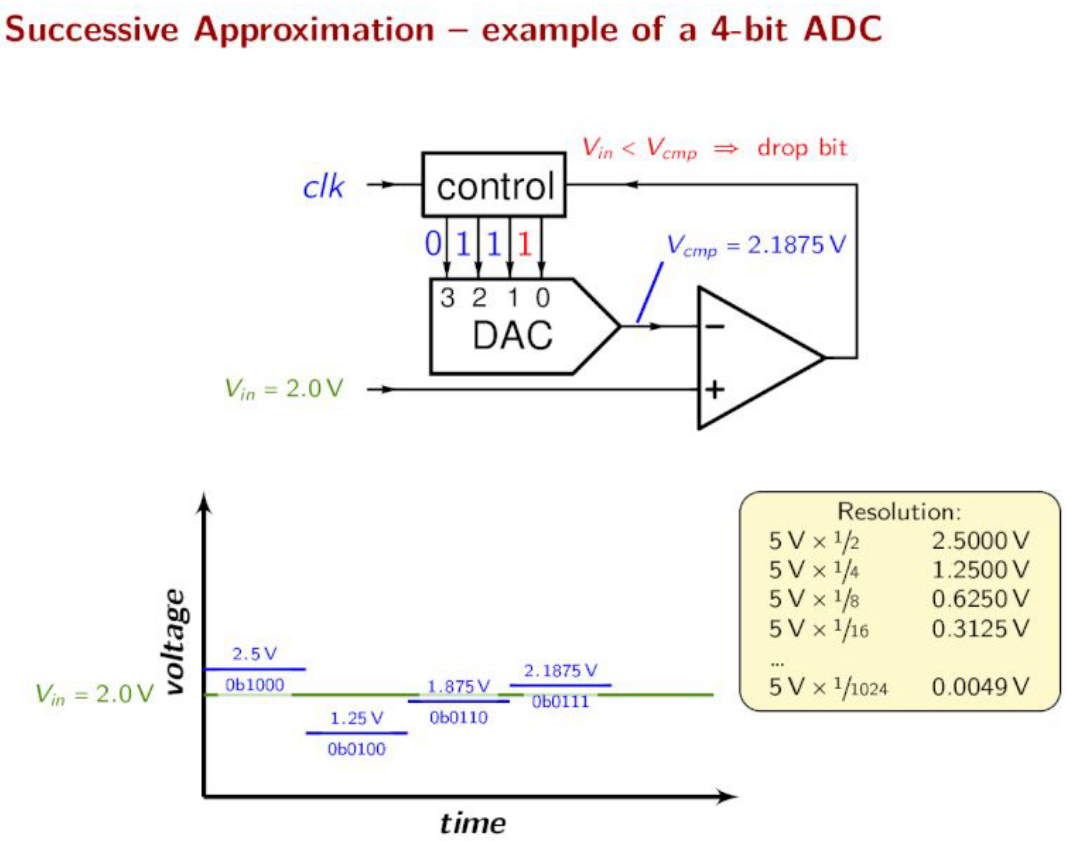
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 2



Comparator outputs 1 when V+>V-, otherwise 0.

Reference:
https://en.wikipedia.org/wiki/Successive-approximation_ADC

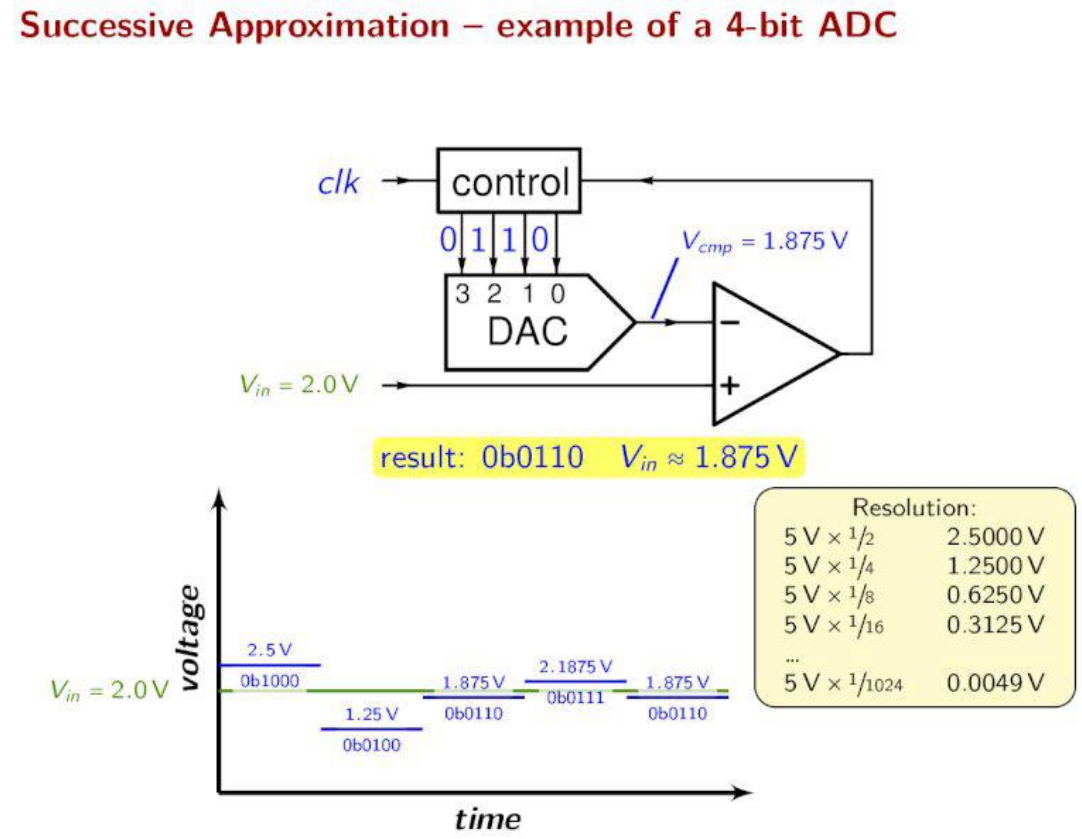
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 2



Comparator outputs 1 when V+>V-, otherwise 0.

Reference: https://en.wikipedia.org/wiki/Successive-approximation_ADC

SUCCESSIVE APPROXIMATION ADC EXAMPLE - 2

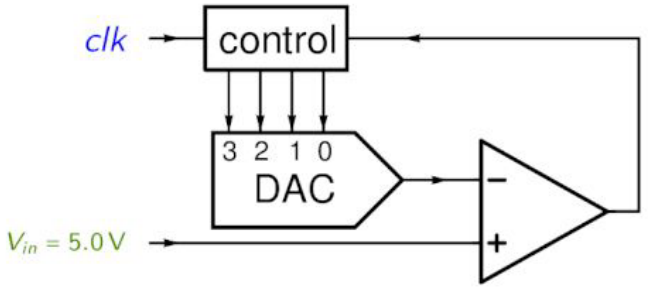


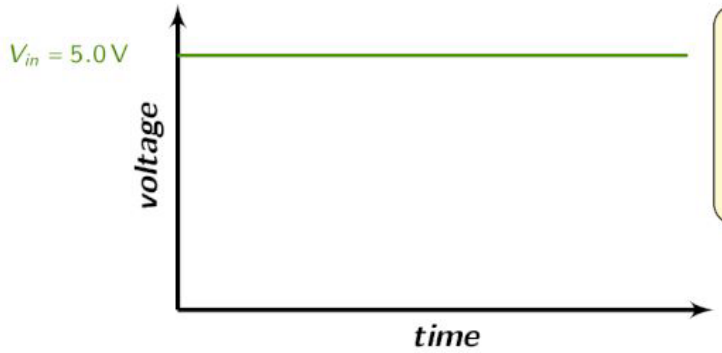
Comparator outputs 1 when V+>V-, otherwise 0.

Reference: https://en.wikipedia.org/wiki/Successive-approximation_ADC

SUCCESSIVE APPROXIMATION ADC EXAMPLE - 3

Successive Approximation – example of a 4-bit ADC



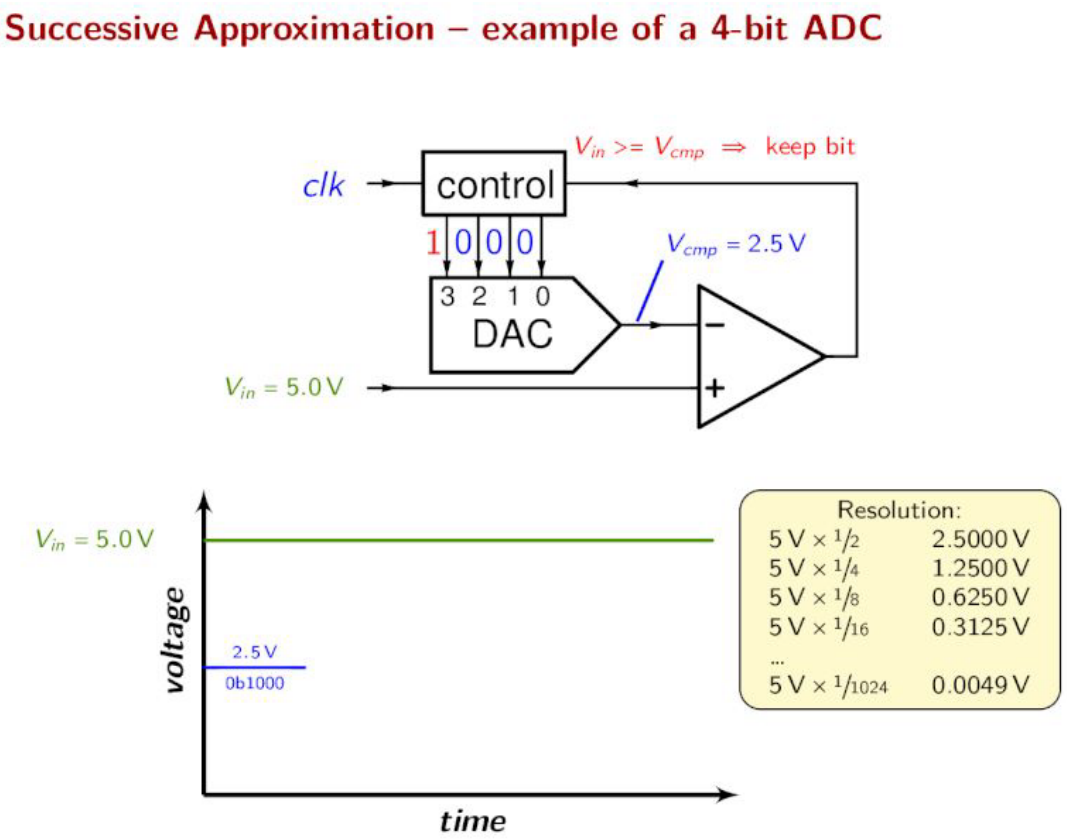


Resolution:	
5 V × 1/2	2.5000 V
5 V × 1/4	1.2500 V
5 V × 1/8	0.6250 V
5 V × 1/16	0.3125 V
...	
5 V × 1/1024	0.0049 V

Comparator outputs 1 when V+>V-, otherwise 0.

Reference:
https://en.wikipedia.org/wiki/Successive-approximation_ADC

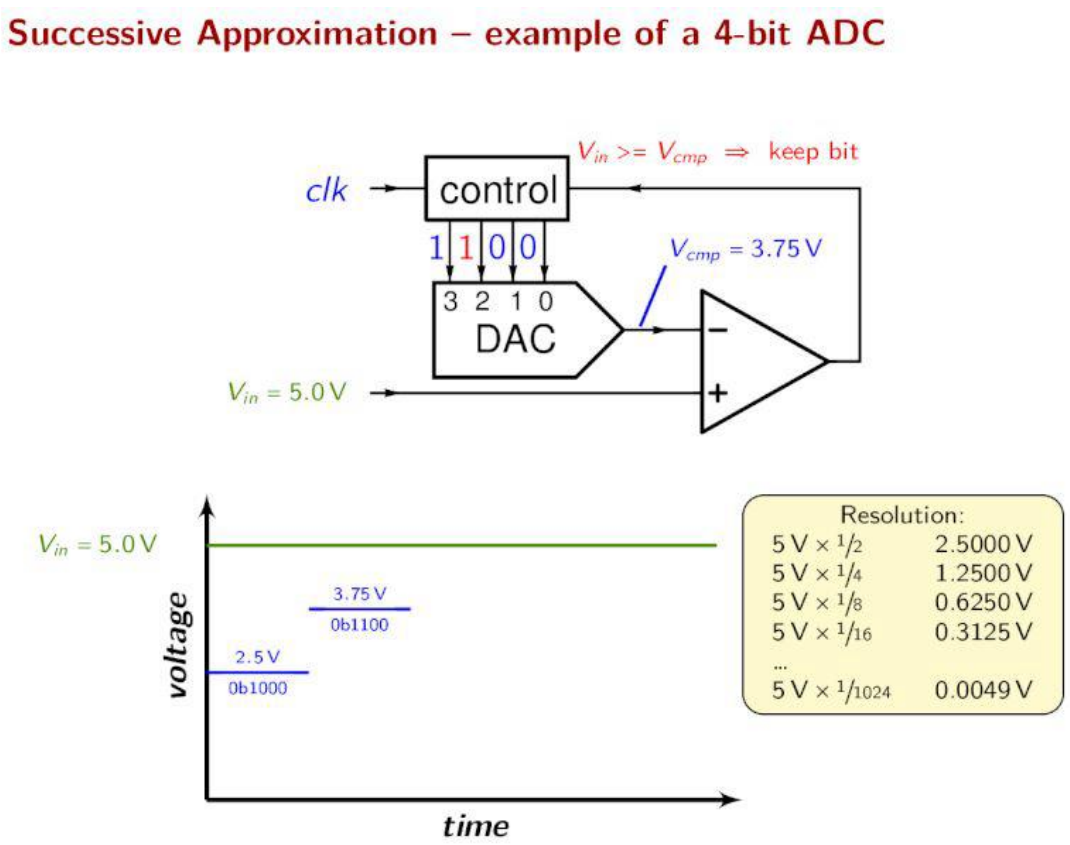
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 3



Comparator outputs 1 when V+>V-, otherwise 0.

Reference: https://en.wikipedia.org/wiki/Successive-approximation_ADC

SUCCESSIVE APPROXIMATION ADC EXAMPLE - 3



Comparator outputs 1 when V+>V-, otherwise 0.

Reference:
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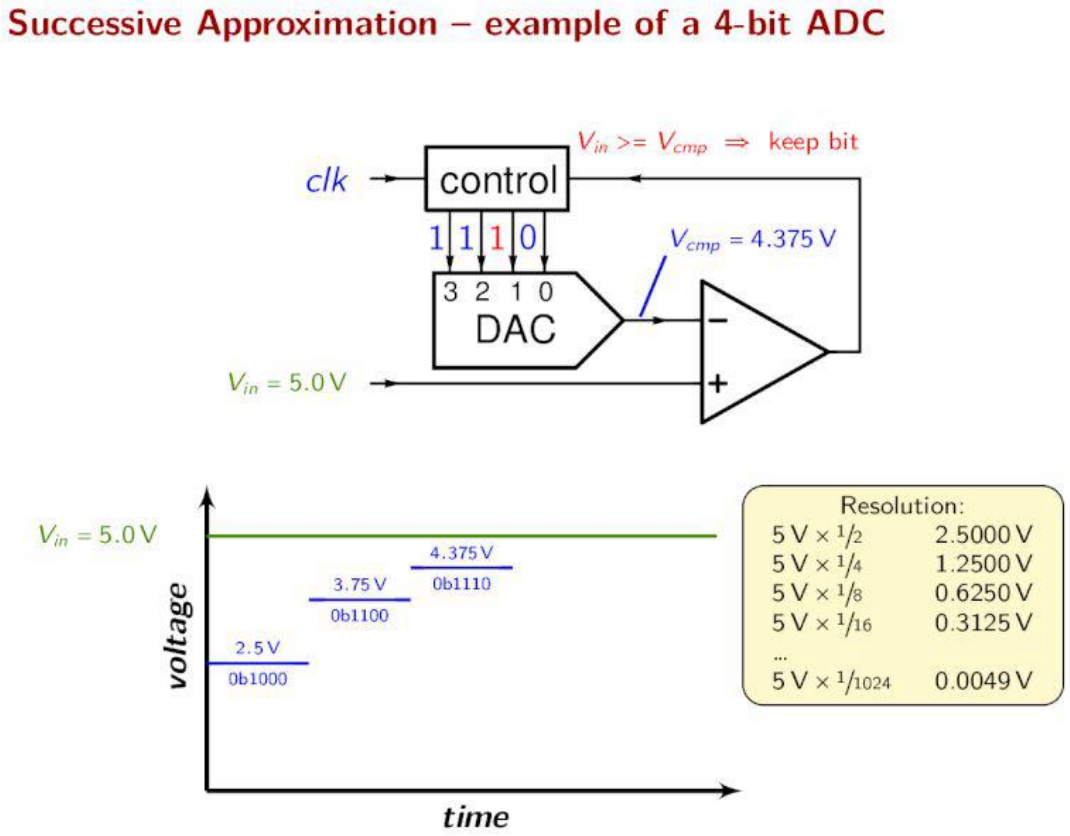
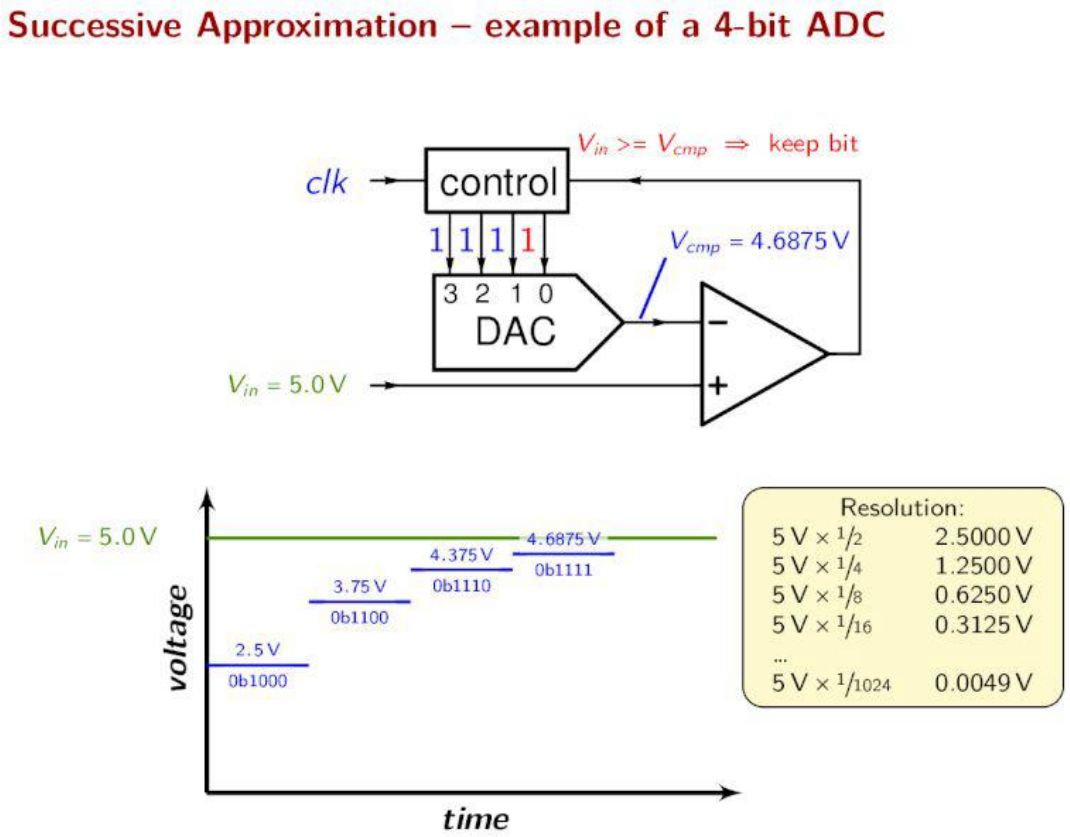
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 3



Comparator outputs 1 when V+>V-, otherwise 0.

Reference: https://en.wikipedia.org/wiki/Successive-approximation_ADC

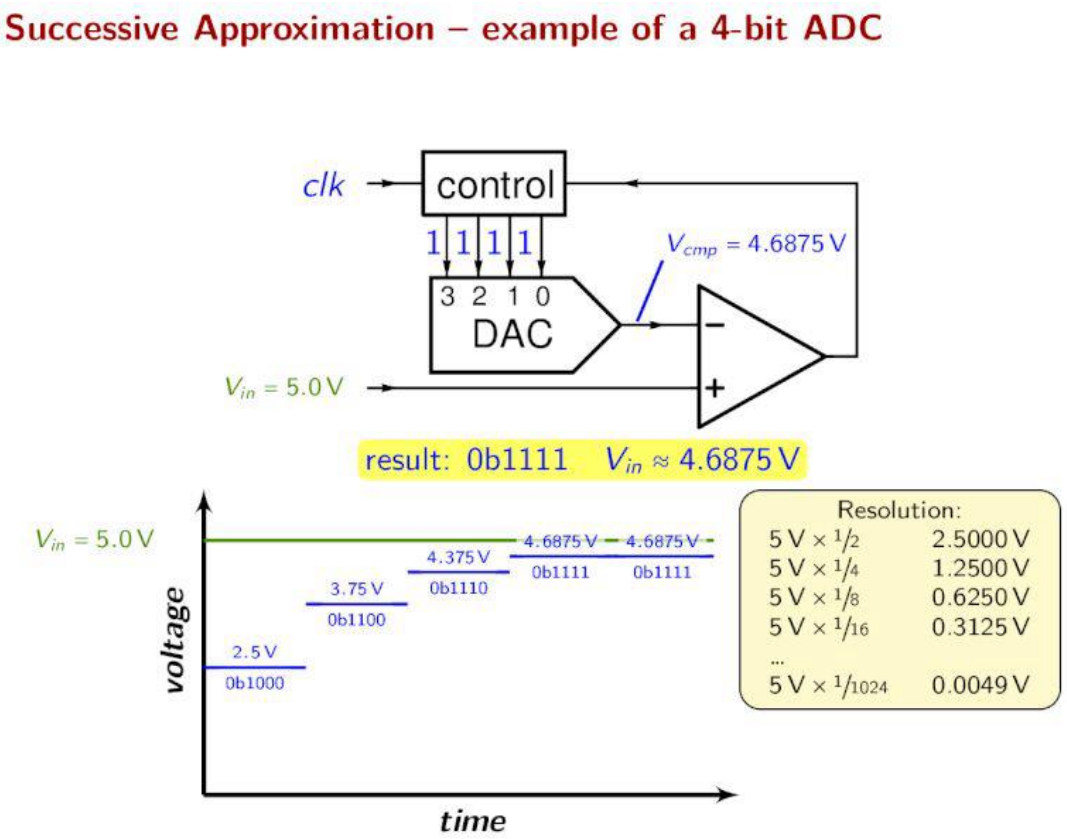
SUCCESSIVE APPROXIMATION ADC EXAMPLE - 3



Comparator outputs 1 when V+>V-, otherwise 0.

Reference:
https://en.wikipedia.org/wiki/Successive-approximation_ADC

SUCCESSIVE APPROXIMATION ADC EXAMPLE - 3



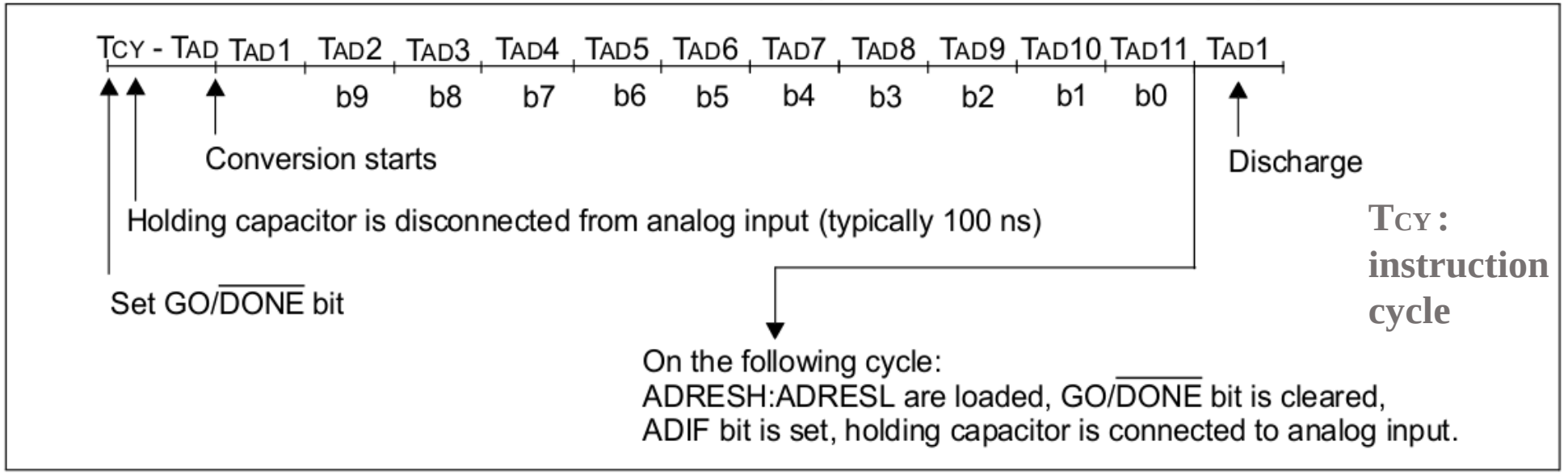
Comparator outputs 1 when V+>V-, otherwise 0.

Reference:
https://en.wikipedia.org/wiki/Successive-approximation_ADC

A/D CONVERSION T_{AD} CYCLES

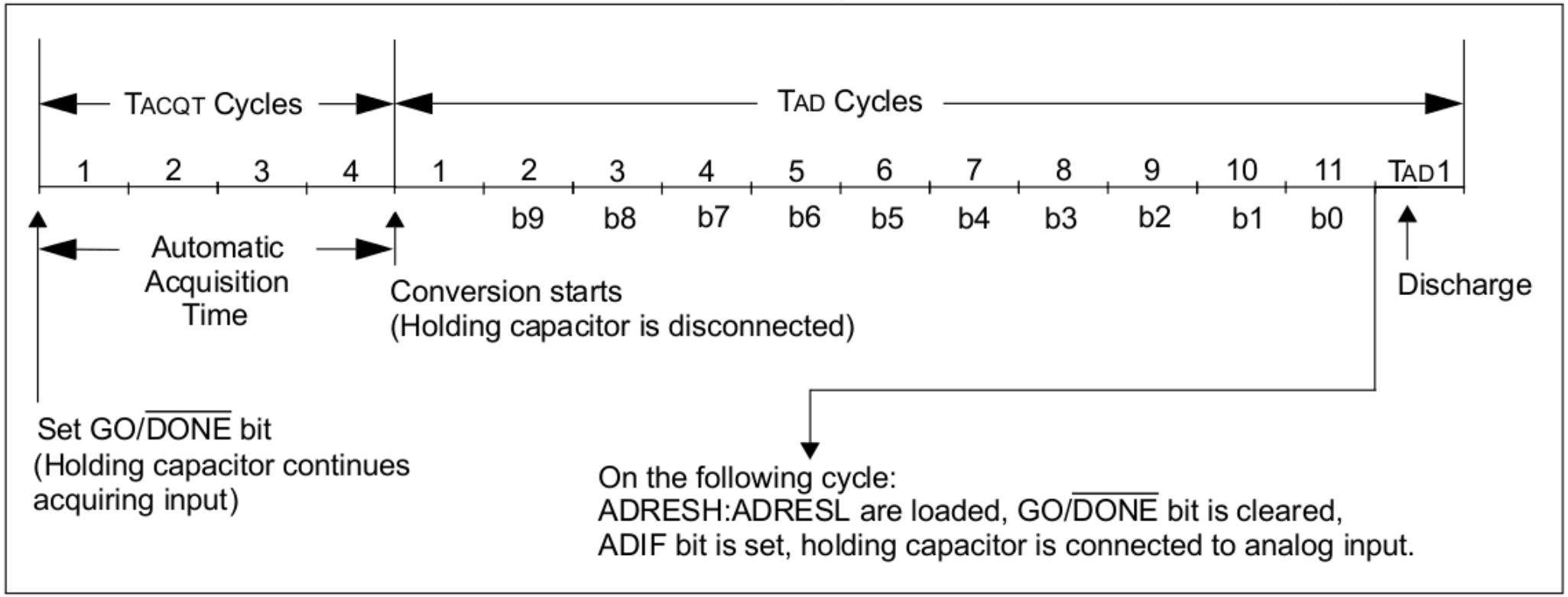
- The A/D conversion time per bit is defined as T_{AD}.
- The A/D conversion requires 11 T_{AD} per 10-bit conversion.

FIGURE 21-4: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 000, TACQ = 0)



A/D CONVERSION T_{AD} CYCLES

FIGURE 21-5: A/D CONVERSION TAD CYCLES (ACQT<2:0> = 010, TACQ = 4 TAD)



SELECTING A/D CONVERSION CLOCK

The seven possible options for TAD are: $2T_{OSC}$, $4T_{OSC}$, $8T_{OSC}$, $16T_{OSC}$, $32T_{OSC}$, $64T_{OSC}$

TABLE 19-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Maximum Device Frequency	
Operation	**ADCS2:ADCS0**	**PIC18F2X20/4X20**	**PIC18LF2X20/4X20(4)**
2 TOSC	000	2.86 MHz	1.43 kHz
4 TOSC	100	5.71 MHz	2.86 MHz
8 TOSC	001	11.43 MHz	5.72 MHz
16 TOSC	101	22.86 MHz	11.43 MHz
32 TOSC	010	40.0 MHz	22.86 MHz
64 TOSC	110	40.0 MHz	22.86 MHz
RC(3)	x11	1.00 MHz(1)	1.00 MHz(2)

Note 1: The RC source has a typical TAD time of 1.2 μs.
2: The RC source has a typical TAD time of 2.5 μs.
3: For device frequencies above 1 MHz. the device must be in Sleep for the entire conversion or the A/D accuracy may be out of specification.
4: Low-power (PIC18LFXXXX) devices only.

see parameter 130, Table 26-28, page 360 for more information

For correct A/D conversions, the A/D conversion clock (T_{AD}) must be as short as possible (e.g. hold capacitor may discharge more), but greater than the minimum TAD (min 0.7 μs, max 25.0 μs (TOSC based, V REF ≥ 3.0V)).

A/D MODULE OPERATION

1. Configure the A/D module:
   - Configure analog pins, voltage reference and digital I/O (ADCON1)
   - Select A/D input channel (ADCON0)
   - Select A/D acquisition time (ADCON2)
   - Select A/D conversion clock (ADCON2)
   - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
   - Clear ADIF bit
   - Set ADIE bit
   - Set GIE bit
3. Wait the required acquisition time (if required).
4. Start conversion:
   - Set GO/$\overline{\text{DONE}}$ bit (ADCON0 register)
5. Wait for A/D conversion to complete, by either:
   - Polling for the GO/$\overline{\text{DONE}}$ bit to be cleared

   OR
   - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as T_{AD}. A minimum wait of 2 T_{AD} is required before the next acquisition starts.

See the notes on the next page ->

A/D MODULE OPERATION

- The analog input channels must have their corresponding TRIS bits selected as inputs.
- When the A/D conversion is complete, the result is loaded into the ADRESH:ADRESL register pair, the GO/DONE bit (ADCON0 register) is cleared and A/D Interrupt Flag bit, ADIF (PIR1<6>), is set.
- If acquisition time is programmed (ACQT2:ACQT0 bit, ADCON2<5:3>), as soon as the GO/DONE is set A/D module continues to sample the selected input for the programmed acquisition time then it starts the conversion.
- If acquisition time is not programmed, it is in the responsibility of the user to ensure that sufficient time passes after the selecting the analog input for input sampling. Then the user can initiate the conversion by setting the GO/DONE bit. Programming the acquisiton time exempts the user from handling the correct action time.

A/D MODULE SOME NOTES

- Resolution indicates the minimum voltage level that an ADC is sensitive to.

$$\text{Resolution} = \frac{\text{Vref}_+ - \text{Vref}_-}{2^{\text{ADC bits}}}$$

$$\text{Resolution of 10-bit ADC } (\text{Vref}_+ = 5.0V, \text{Vref}_- = 0.0V) = \frac{5.0V}{2^{10}} = \sim 0.0049V$$

- The GO/DONE bit should NOT be set in the same instruction that turns on the A/D, due to the required acquisition time requirement.

- If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

XC8 COMPILER

MPLAB XC8 C COMPILER

- Official C compiler from Microchip
- Can be downloaded from:
  https://www.microchip.com/pagehandler/en-us/family/mplabx/
- Can be used with MPLAB X IDE
- Getting Started and User's Guides can be downloaded from:
  https://www.microchip.com/pagehandler/en_us/devtools/mplabxc/

SUPPORTING DATA TYPES

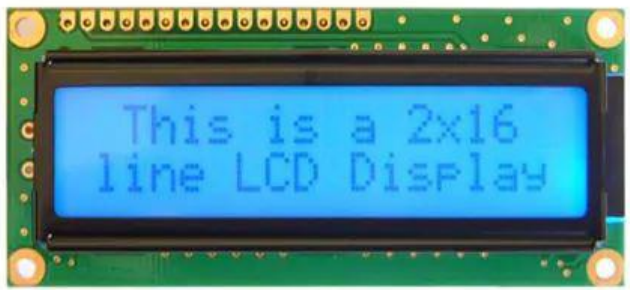
TABLE 5-1: INTEGER DATA TYPES

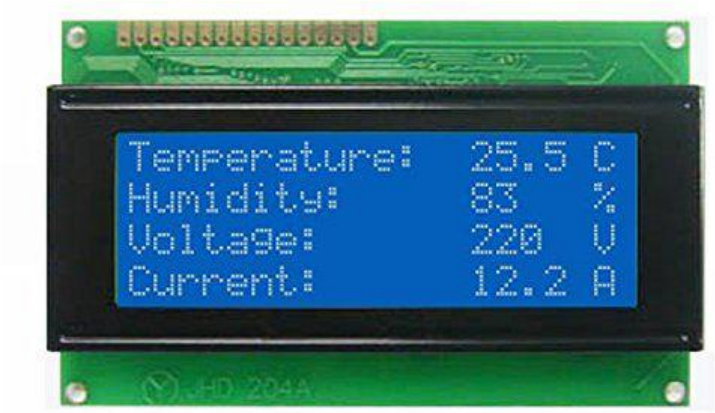
Type	Size (bits)	Arithmetic Type
`bit`	1	Unsigned integer
`signed char`	8	Signed integer
`unsigned char`	8	Unsigned integer
`signed short`	16	Signed integer
`unsigned short`	16	Unsigned integer
`signed int`	16	Signed integer
`unsigned int`	16	Unsigned integer
`signed short long`	24	Signed integer
`unsigned short long`	24	Unsigned integer
`signed long`	32	Signed integer
`unsigned long`	32	Unsigned integer
`signed long long`	32	Signed integer
`unsigned long long`	32	Unsigned integer

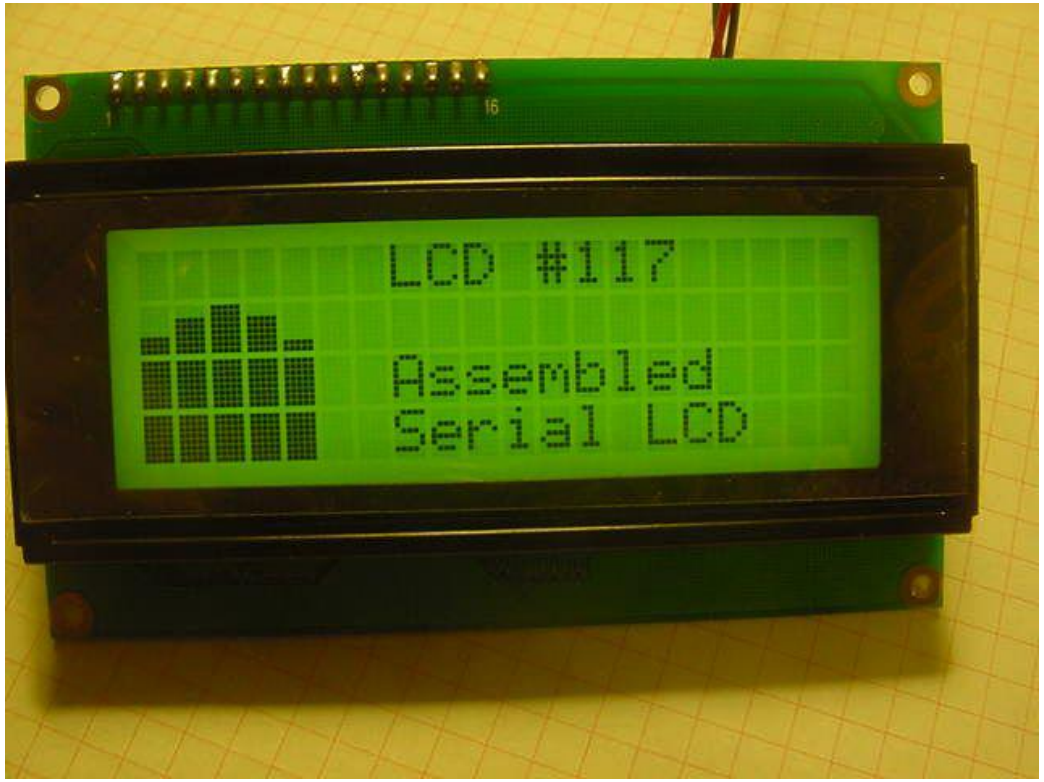
Type	Size (bits)	Arithmetic Type
`float`	24 or 32	Real
`double`	24 or 32	Real
`long double`	same as `double`	Real

LCD

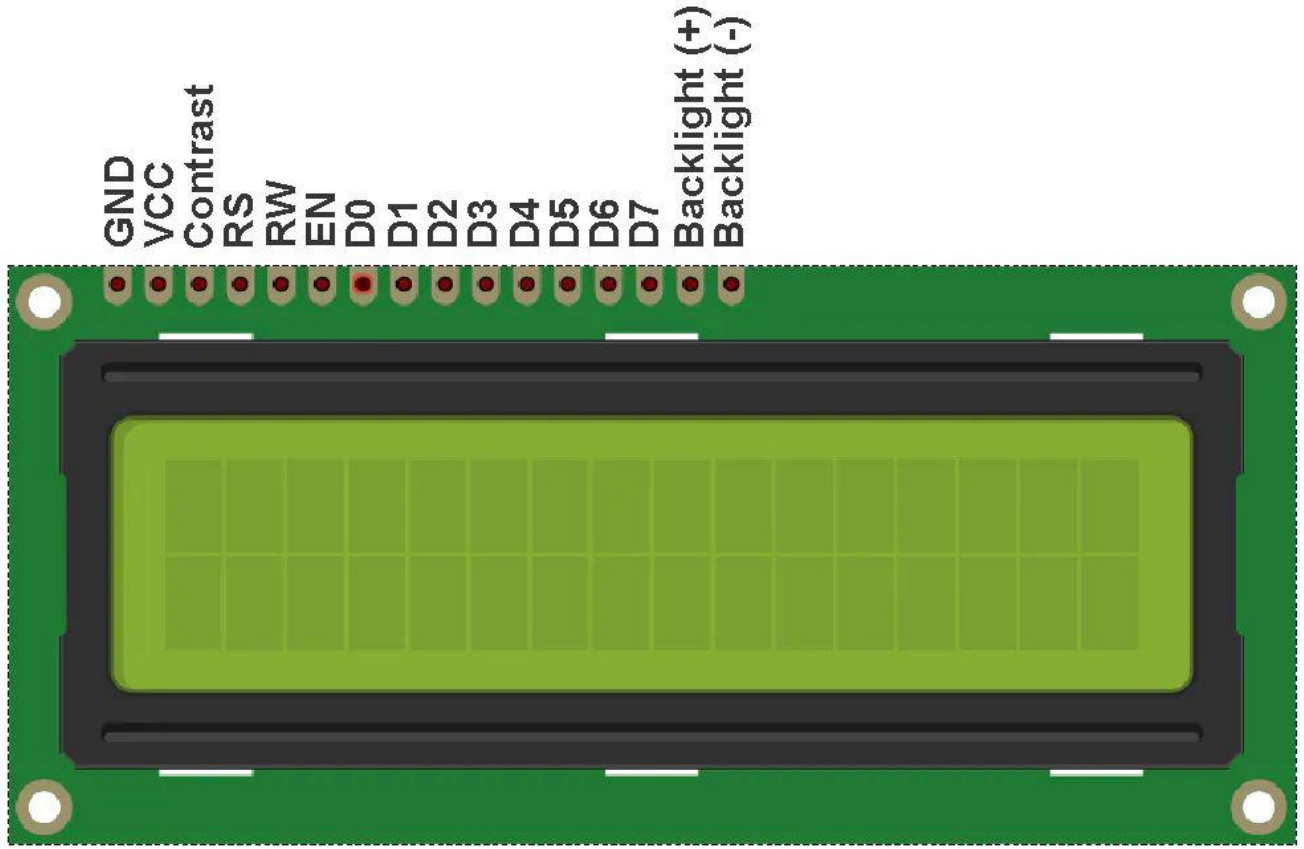
LCD


This is a 2x16
line LCD Display


Temperature: 25.5 C
Humidity: 83 %
Voltage: 220 V
Current: 12.2 A
JHD 204A


LCD #117
Assembled
Serial LCD

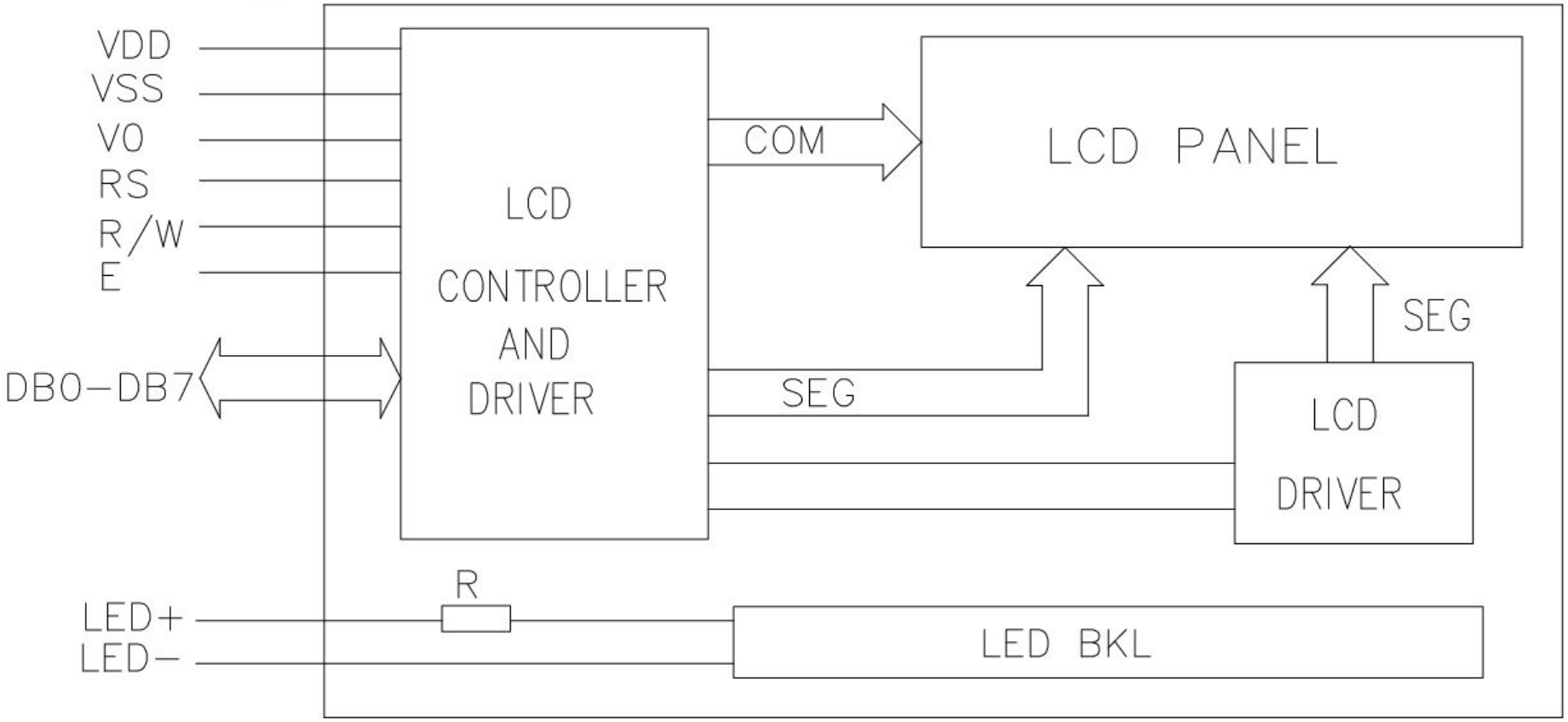
LCD PINOUTS


GND
VCC
Contrast
RS
RW
EN
D0
D1
D2
D3
D4
D5
D6
D7
Backlight (+)
Backlight (-)

LCD PINOUTS

Pin	Level	Description	Connection
1	0 V	Ground	GND
2	+5 V	Vcc	+5V
3	Variable	Contrast Voltage	Pot.
4	H/L	"R/S", H:DATA, L:Instruction	RE2
5	H/L	"R/W", H:Read (Lcd →Pic), L:Write(Pic → Lcd)	GND
6	H, H→L	"E" Clock input	RE1
7-14	H/L	I/O Pins	PORTD
15	-	Backlight anode	+5V
16	-	Backlight cathode	RA5(INVERTED)

LCD BLOCK DIAGRAM



MEMORIES INSIDE LCD

DDRAM : Data Display RAM is the working data buffer of the display. Each character on the display has a corresponding DDRAM location and the byte loaded in DDRAM controls which character is displayed.

Relationship between DDRAM addresses (7-bit) and positions on the liquid crystal display.

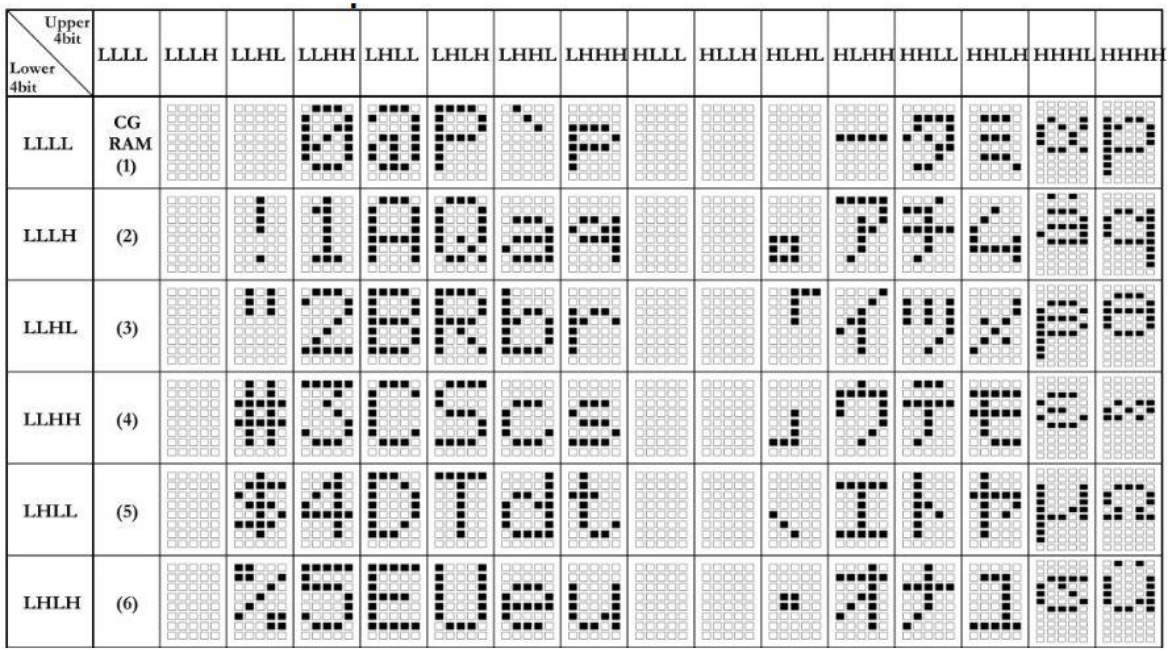
Display position	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DDRAM address	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F
DDRAM address	40	41	42	43	44	45	46	47	48	49	4A	4B	4C	4D	4E	4F

2-Line by 16-Character Display

DDRAM address counter (AC) points where to display character. This address can be set via LCD instructions.

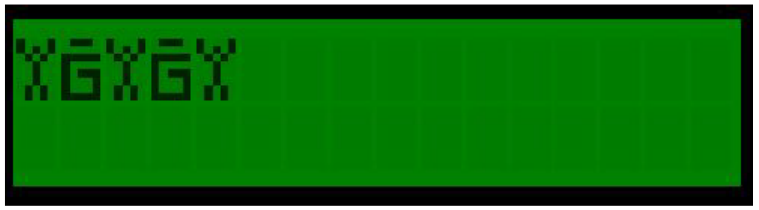
MEMORIES INSIDE LCD

CGROM : Character Graphics ROM that holds the fixed character set, namely all the standard patterns of dots for dot matrix characters



MEMORIES INSIDE LCD

CGRAM : Character Graphics RAM that allows the user to define special supplementary non-standard character types that are not in the CGROM. You can load your own dot pattern shapes and display them. You can define maximum 8 characters.



INTERFACING WITH LCD

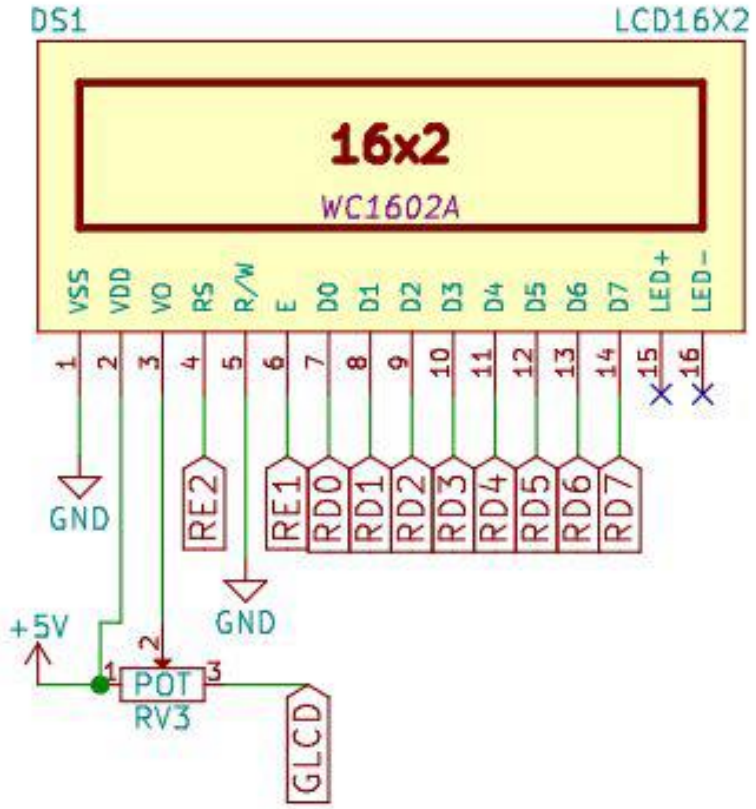
- LCD- "RS" → Used to select whether data or an instruction is being transferred between the microcontroller and the LCD.

  H : Data, L : Instruction.
- LCD- "R/W" → Used to read data from LCD or write data to LCD.

  H : Read (LCD → PIC), L : Write (PIC → LCD).

  On PicGENIOS, R/W is connected to the Ground.
- LCD- "E" → After an instruction code or a data presented to the I/O pins a clock pulse should be sent to this pin. (High to Low)

INTERFACING WITH LCD



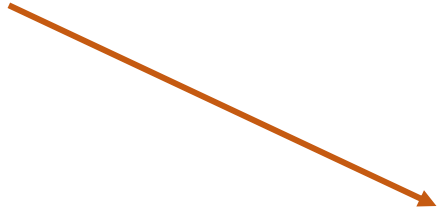
Attention: RE1 and RE2 pins are also analog pins. PCFG 4:0 bits of ADCON1 should be set for configuring them as digital outputs.

11.9 Instruction Table

Instruction	Instruction code										Description	Execution time (fosc= 270 KHZ
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0		
Clear Display	0	0	0	0	0	0	0	0	0	1	Write “20H” to DDRA and set DDRAM address to “00H” from AC	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	-	Set DDRAM address to “00H” From AC and return cursor to Its original position if shifted. The contents of DDRAM are not changed.	1.53ms
Entry mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction And blinking of entire display	39us
Display ON/ OFF control	0	0	0	0	0	0	1	D	C	B	Set display (D), cursor (C), and Blinking of cursor (B) on/off Control bit.	
Cursor or Display shift	0	0	0	0	0	1	S/C	R/L	-	-	Set cursor moving and display Shift control bit, and the Direction, without changing of DDRAM data.	39us
Function set	0	0	0	0	1	DL	N	F	-	-	Set interface data length (DL: 8-Bit/4-bit), numbers of display Line (N: =2-line/1-line) and, Display font type (F: 5x11/5x8)	39us
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address Counter.	39us
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address Counter.	39us
Read busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal Operation or not can be known By reading BF. The contents of Address counter can also be read.	0us
Write data to Address	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43us
Read data From RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43us

LCD INSTRUCTION CODES

LCD Instruction Codes



The value of R/S bit: Low

CLEAR DISPLAY

- Clears all display memory and returns the cursor to the home position.

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	0	1

RETURN HOME

- Returns the cursor to the home position (left top).
- DDRAM contents remain unchanged.

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	0	1	X

ENTRY MODE SET

- Sets the cursor move direction and specifies whether or not to shift the display. These operations are performed during data write and read.

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	0	1	I/D	S

I/D = 1 : Increment DDRAM address
I/D = 0 : Decrement DDRAM address

S = 1 : Display shift [I/D = 1 : Left, I/D = 0 : Right]
S = 0 : No display shift

ENTRY MODE SET

Command : 00000110
Increment Address Counter
Display Shift : OFF

Command : 0000100
Decrement Address Counter
Display Shift : OFF

Command : 00000111
Display Shift : ON
Shift LEFT

Command : 00000101
Display Shift : ON
Shift RIGHT

Example entry mode settings

DISPLAY & CURSOR CONTROL

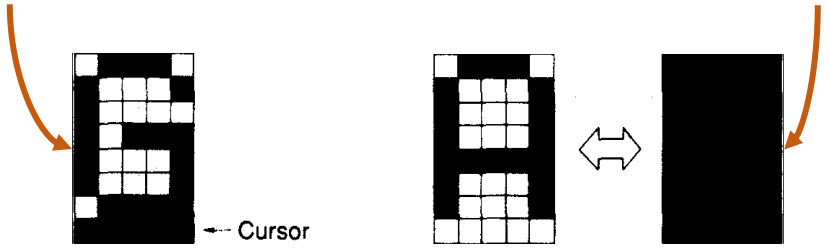
- Sets display (D), cursor (C), and blinking of cursor (B) on/off control bit.

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1	D	C	B

D = 1 : Display ON
D = 0 : Display OFF

C = 1 : Cursor ON
C = 0 : Cursor OFF

B = 1 : Blink ON
B = 0 : Blink OFF



CURSOR OR DISPLAY SHIFT

- Moves the cursor or shifts the display without changing DD RAM contents.

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	1	S/C	R/L	X	X

S/C	R/L	Operation
0	0	The cursor position is shifted to the left
0	1	The cursor position is shifted to the right
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

FUNCTION SET

- Sets interface data length (DL), number of display lines (N), and character font (F).

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1	DL	N	F	X	X

F = 1 : 5x11 dots
F = 0 : 5x8 dots

N = 1 : 2 lines
N = 0 : 1 line

DL = 1 : 8-bit
DL = 0 : 4-bit

SET DDRAM ADDRESS

- Sets the DDRAM address (where the character will be displayed on the screen).

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	A6	A5	A4	A3	A2	A1	A0

Line1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F
Line2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF
Line3	90	91	92	93	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F
Line4	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF

Relationship between I/O port (PORTD in our case) values and positions on the liquid crystal display.

SET CGRAM ADDRESS

- Sets the CGRAM address (where custom characters can be populated) (maximum 8 characters).

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	A5	A4	A3	A2	A1	A0

WRITE DATA TO RAM

- Writes data into the RAM.

RS	R/W	D7	D6	D5	D4	D3	D2	D1	D0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

EXAMPLES