

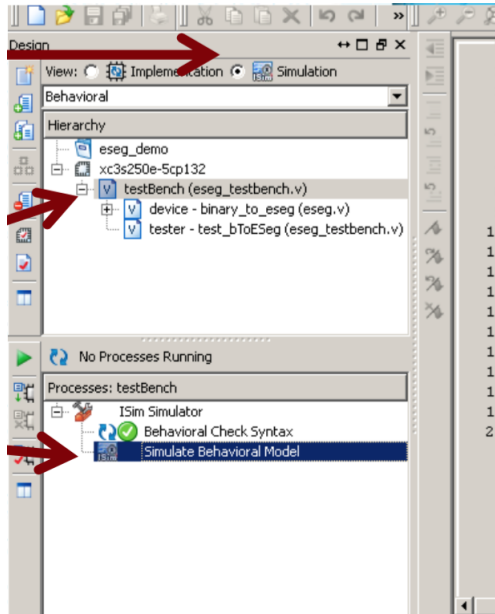


# CENG 232 - How to use the FPGA board

*Middle East Technical University*

*Department of Computer Engineering*

# XILINX - SIMULATING WITH A TEST BENCH



# XILINX - ISIM SIMULATOR

The screenshot displays the Xilinx ISE ISIM simulator interface. The top toolbar contains various icons for simulation and file operations. A red circle highlights a subset of these icons, with a red arrow pointing to the text "Controls Timing Diagram scale".

The main window is divided into three panes:

- Left Pane:** A table listing signals w1, w2, w3, w4, and w5. w4 is selected.
- Center Pane:** A timing diagram showing signal waveforms. A red circle highlights the bottom toolbar of this pane, with a red arrow pointing to the text "Timing Diagram Vs Source Code view".
- Bottom Pane:** The console window showing simulation output.

**Timing Diagram**

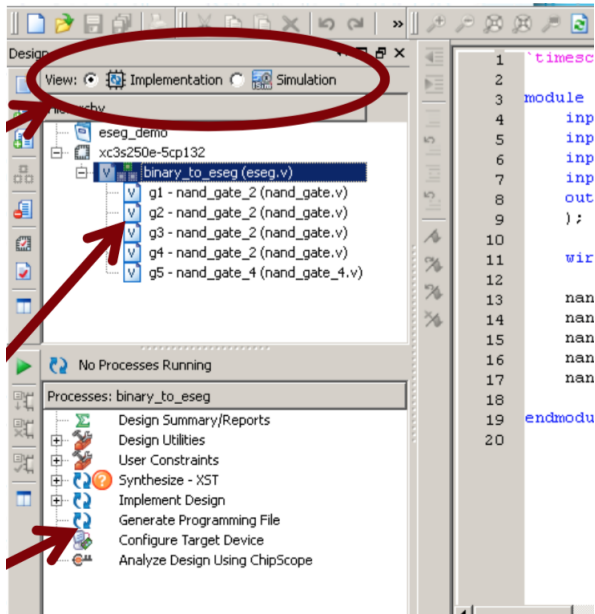
The timing diagram shows a clock signal (w4) and several data signals (w1, w2, w3, w5). A vertical yellow line indicates a specific time point at 13.943 ns.

**Simulator Output**

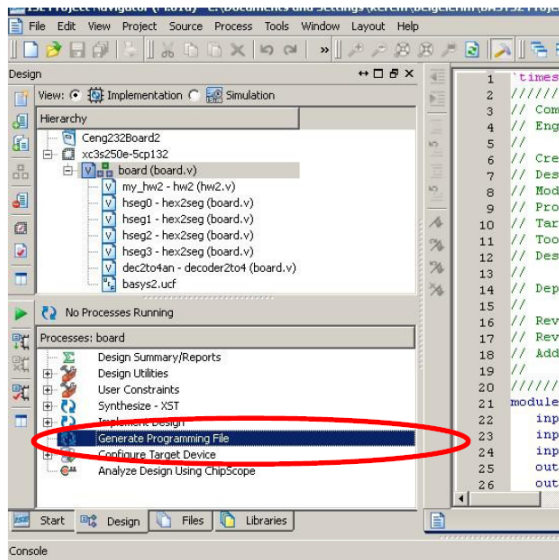
```
mmi-source-version: 1.0m
Time resolution is 1 ps
Simulator is doing circuit initialization process.
Finished circuit initialization process.
0 A=0 B=0 C=0 D=0 eSeg=0
Setting all inputs to 0
10 A=0 B=0 C=0 D=0 eSeg=1
Setting D to 1
20 A=0 B=0 C=0 D=1 eSeg=0
Setting C to 1, D to 0
30 A=0 B=0 C=1 D=0 eSeg=1
Ending simulation
Stopped at time : 40 ns : File "C:/Documents and Settings/Keren/Belgelerim/cors232-1st recitation/verilog/eseg_demo/eseg_testbench.v"
```

Sim Time: 40,000 ps

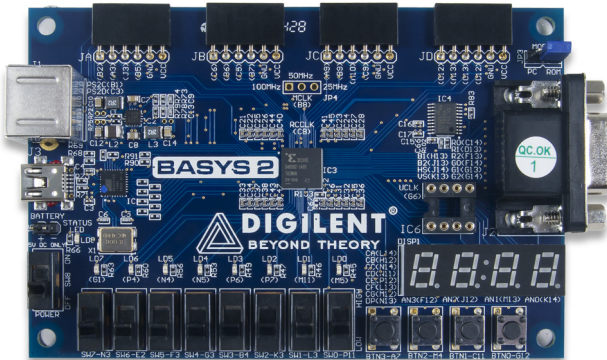
# XILINX - CREATING A BIT FILE



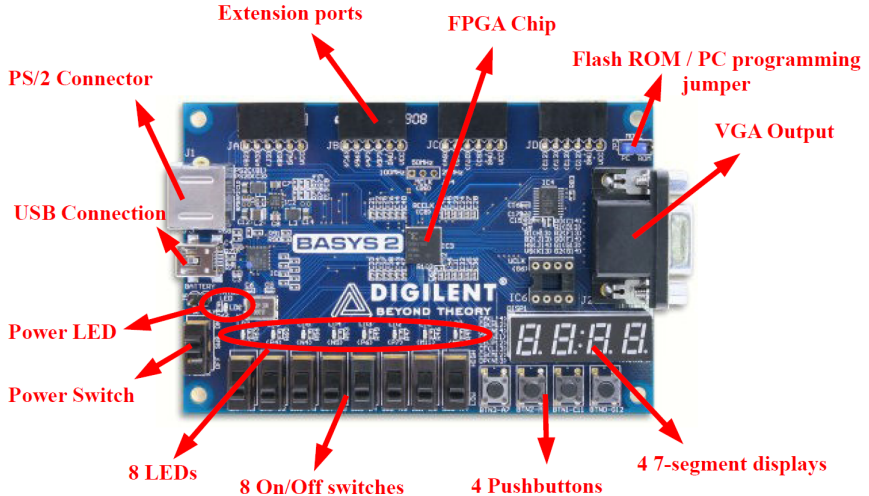
# XILINX - CREATING A BIT FILE



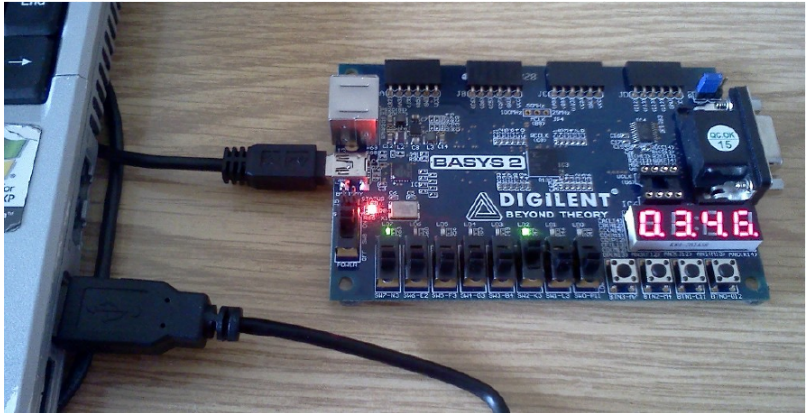
# THE FPGA BOARD TO BE USED



# PARTS OF THE FPGA BOARD



# HOW TO CONNECT FPGA BOARD TO COMPUTER



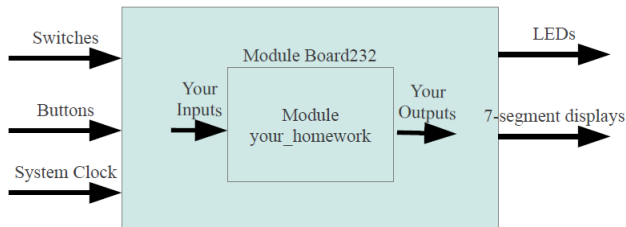


# HOW TO CONNECT FPGA BOARD TO COMPUTER

- ▶ When connecting the board to the computer, board should be off.
- ▶ Open the board from the switch before you will upload your data. (After connecting)
- ▶ Before uploading data, make sure that the jumper is to the left.
- ▶ If you need the change the place of the jumper, make it when the board is off.

# INPUTS AND OUTPUTS OF THE BOARD

- ▶ Switches, push buttons and the clock can be used as inputs.
- ▶ Leds and seven segment display can be used as a output.
- ▶ You should connect these parts carefully in your verilog module with your inputs and outputs.

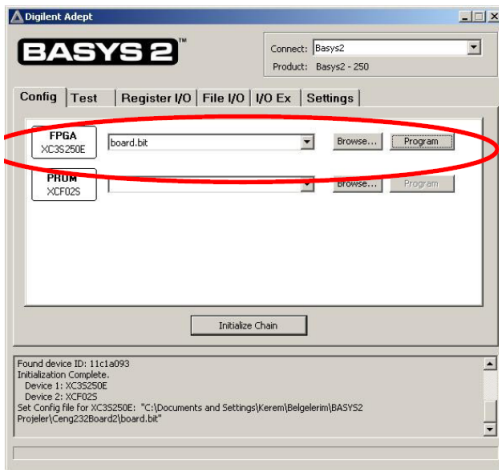


# UPLOADING THE BIT FILE

- ▶ Is done via digilent adept.
- ▶ Digilent adept link
- ▶ Download both utilities and runtime executables.
- ▶ After installing, open the board (from the switches).
- ▶ Then upload the bitfile.

# UPLOADING THE BIT FILE - WINDOWS

- Just upload the bitfile to the user interface of the adept.



# UPLOADING THE BIT FILE - LINUX

- ▶ Run the following command from the terminal.
- ▶ `djtgcfg prog -d Basys2 -i 0 -f Board232.bit`

## AFTER THE UPLOAD

- ▶ The board will behave as you coded it in the verilog.
- ▶ To run it second time, you have to upload it again, it is uploaded to board for only one usage.
- ▶ After you make the switch off, all the information will be vanished from the board and you have to upload the bitfile again.