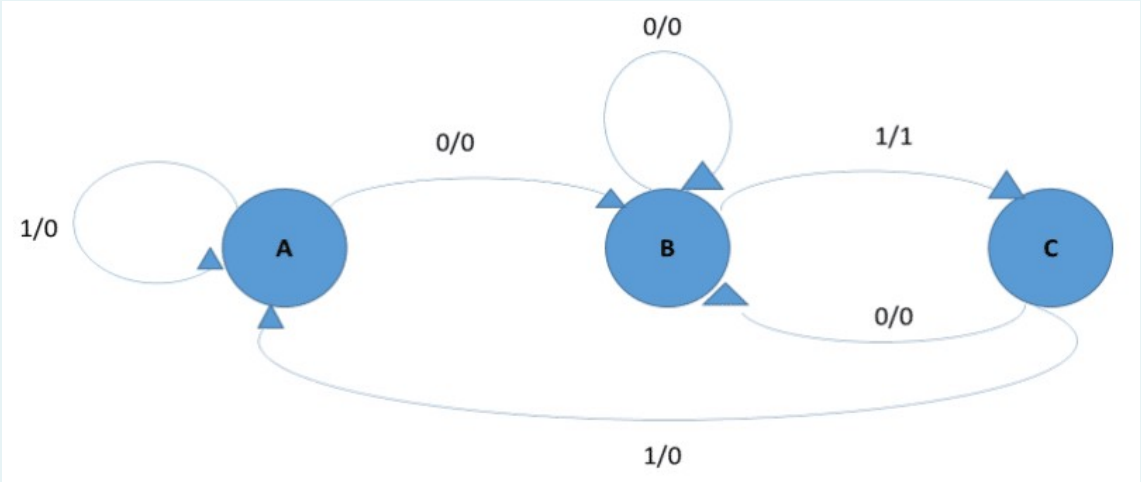
Started on	Tuesday, June 1, 2021, 10:40 AM
State	Finished
Completed on	Tuesday, June 1, 2021, 12:09 PM
Time taken	1 hour 29 mins
Grade	**72.00** out of 100.00

Question **1**

Correct

4.00 points out of 4.00

Describe the function of the sequential circuit having the following state diagram. Note that the circuit has one input, X, and one output Y.



a. Detects 00 patterns coming through an input line X. The circuit output Y is 1 when a 00 pattern is detected, 0 otherwise.

b. Detects 01 patterns coming through an input line X. The circuit output Y is 1 when a 01 pattern is detected, 0 otherwise. ✔

c. Detects 10 patterns coming through an input line X. The circuit output Y is 1 when a 10 pattern is detected, 0 otherwise.

d. Detects 11 patterns coming through an input line X. The circuit output Y is 1 when a 11 pattern is detected, 0 otherwise.

Your answer is correct.

The correct answer is:

Detects 01 patterns coming through an input line X. The circuit output Y is 1 when a 01 pattern is detected, 0 otherwise.

Question **2**

Incorrect

0.00 points out of 3.00

A binary ripple counter uses flip-flops that trigger on the positive edge of the clock. What will be the count if the complement outputs of the flip-flops are connected to the clock

- a. A count down counter ✖
- b. A BCD counter
- c. Nothing happens
- d. A count up counter

Your answer is incorrect.

The correct answer is:
A count up counter

Question **3**

Incorrect

0.00 points out of 4.00

How many states are left when you reduce the number of states in the following state table?

	Next State		Output	
Present State	$x = 0$	$x = 1$	$x = 0$	$x = 1$
a	f	b	0	0
b	d	c	0	0
c	f	e	0	0
d	g	a	1	0
e	d	c	0	0
f	f	b	1	1
g	g	h	0	1
h	g	a	1	0

- a. 4
- b. 5
- c. 6 ✖
- d. 3

Your answer is incorrect.

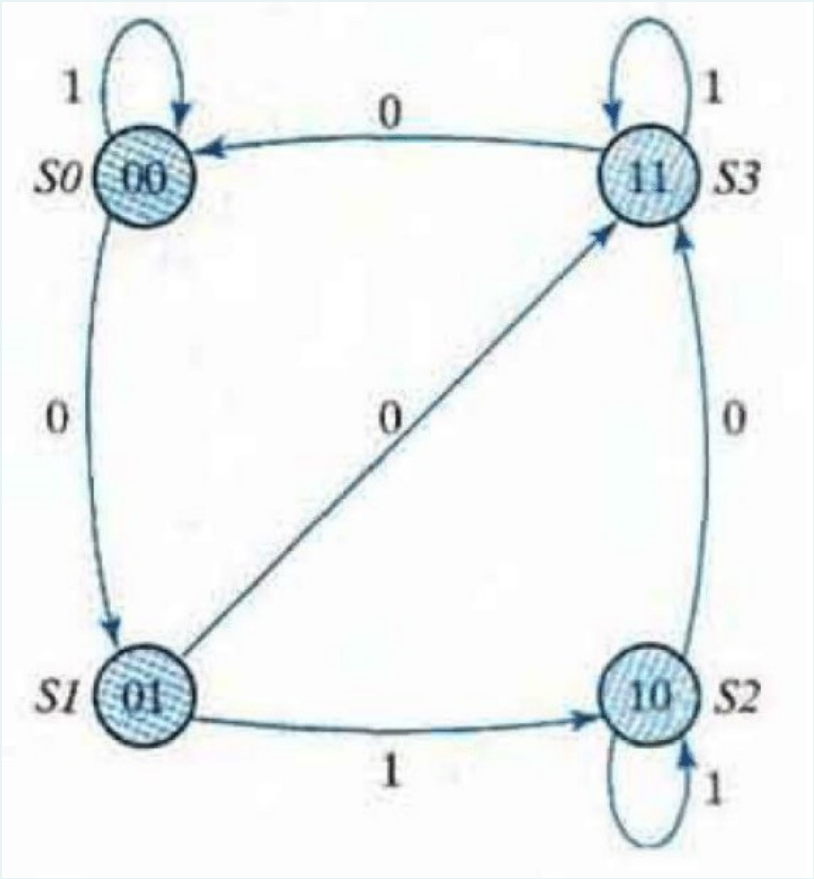
The correct answer is:
5

Question **4**

Correct

4.00 points out of 4.00

Starting from state 00 in the state diagram below, determine the state transitions that will be generated when an input sequence of 011000110 is applied.



a. input: 0 1 1 0 0 0 1 1 0
state: 01-10-10-10-11-00-00-01-10

b. input: 0 1 1 0 0 0 1 1 0
state: 01-11-00-01-10-10-11-11-00

c. input: 0 1 1 0 0 0 1 1 0
state: 01-10-10-11-00-01-10-10-11

d. input: 0 1 1 0 0 0 1 1 0
state: 01-10-10-11-00-01-11-10-10

Your answer is correct.

The correct answer is:
input: 0 1 1 0 0 0 1 1 0
state: 01-10-10-11-00-01-10-10-11

Question **5**

Correct

4.00 points out of 4.00

Given the state table of a sequential circuit, what are the FF input equations if D-FFs are used and unused states are treated as don't care conditions?

Present State Q_1 Q_2	Input (X)	Next State Q_1 Q_2	Output (Z)
0 0	0	0 1	0
0 0	1	0 0	0
0 1	0	0 1	0
0 1	1	1 0	1
1 0	0	0 1	0
1 0	1	0 0	0
1 1	0	x	x
1 1	1	x	x

a. $D_2 = Q_2' X$
$D_1 = X(Q_1' + Q_2')$

b. $D_2 = Q_2' Q_1 X$
$D_1 = Q_2' X$

c. $D_2 = Q_2 X$
$D_1 = X'$ ✔

d. $D_2 = Q_2' X$
$D_1 = Q_2' Q_1 X$

Your answer is correct.

The correct answers are:

$D_2 = Q_2' Q_1 X$
$D_1 = Q_2' X,$

$D_2 = Q_2 X$
$D_1 = X',$

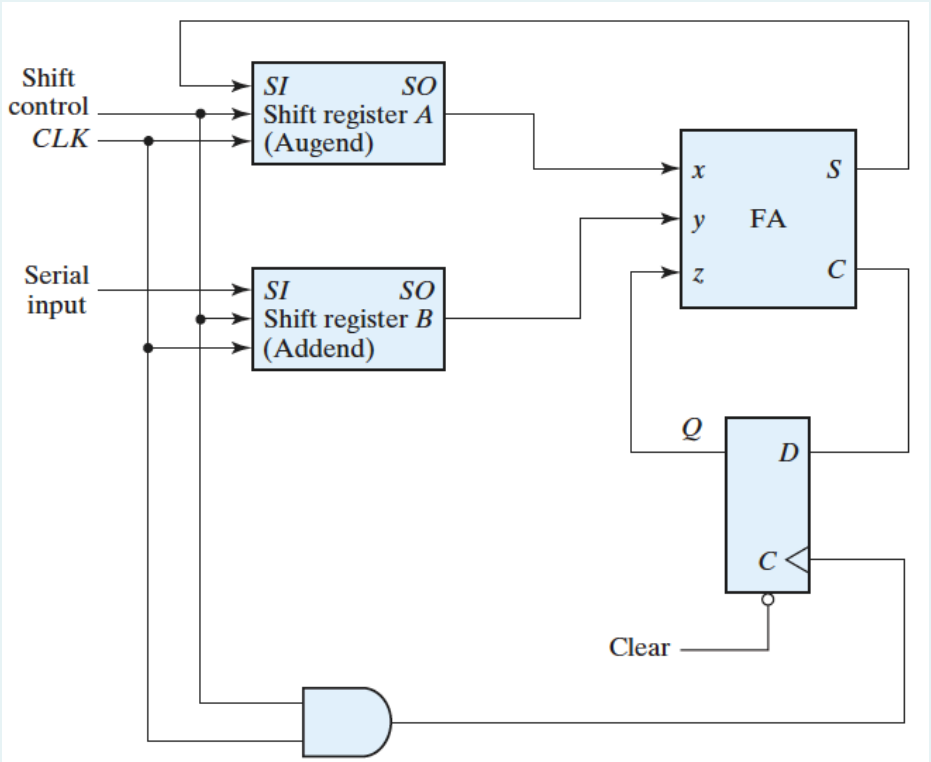
$D_2 = Q_2' X$
$D_1 = Q_2' Q_1 X,$

$D_2 = Q_2' X$
$D_1 = X(Q_1' + Q_2')$

Question **6**

Incorrect

0.00 points out of 3.00



Which of the following changes convert the above serial adder (A+B) to a serial subtractor (A-B)?

a. Replace D flip-flop with JK flip-flop

b. Complement the serial output of shift register B with an inverter and set the initial value of the carry to 1

c. Replace Full Adder (FA) with Full Subtractor (FS) ✖

d. Replace AND gate with NAND gate and set the initial value of the carry to 0

Your answer is incorrect.

The correct answer is:

Complement the serial output of shift register B with an inverter and set the initial value of the carry to 1

Question **7**

Incorrect

0.00 points out of 3.00

The characteristic equation of D-flip-flop implies that

- a. the next state is dependent on present state ✖
- b. the next state is dependent on previous state.
- c. the next state is independent on previous state.
- d. the next state is independent of present state.

Your answer is incorrect.

The correct answer is:
the next state is independent of present state.

Question **8**

Correct

3.00 points out of 3.00

A DRAM must be

- a. always enabled
- b. programmed before each use
- c. refreshed periodically ✔
- d. replaced periodically

Your answer is correct.

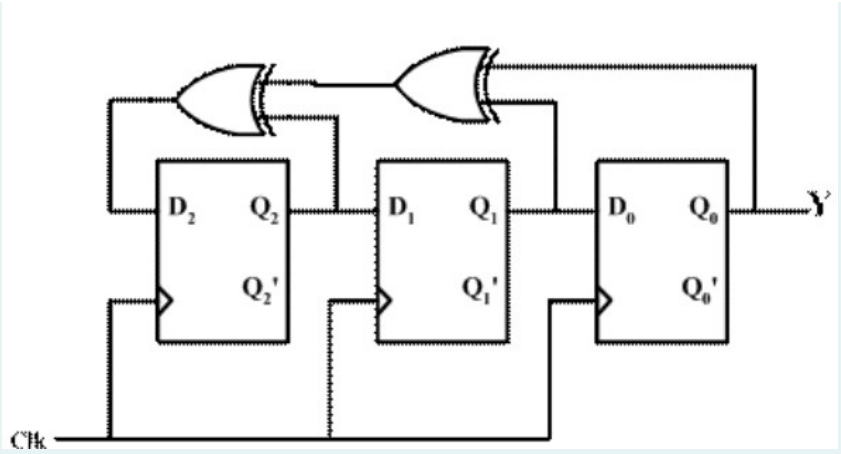
The correct answer is:
refreshed periodically

Question **9**

Correct

4.00 points out of 4.00

Given the following circuit diagram, which one is the state table of this circuit ?



a.

Present State			Next State			Output	FF Inputs		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Y	D_2	D_1	D_0
0	0	0	0	0	1	0	0	0	0
0	0	1	1	0	1	1	1	0	0
0	1	0	1	0	0	0	1	0	1
0	1	1	0	0	0	1	0	0	1
1	0	0	1	1	1	0	1	1	0
1	0	1	0	1	1	1	0	1	0
1	1	0	0	1	0	0	0	1	1
1	1	1	1	1	0	1	1	1	1

b.

Present State			Next State			Output	FF Inputs		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Y	D_2	D_1	D_0
0	0	0	0	1	0	0	0	0	0
0	0	1	1	1	0	1	1	0	0
0	1	0	1	1	1	0	1	0	1
0	1	1	0	1	1	1	0	0	1
1	0	0	1	0	0	0	1	1	0
1	0	1	0	0	0	1	0	1	0
1	1	0	0	0	1	0	0	1	1
1	1	1	1	0	1	1	1	1	1

c.

Present State			Next State			Output	FF Inputs		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Y	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1	0	0
0	1	0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0	0	1
1	0	0	1	1	0	0	1	1	0
1	0	1	0	1	0	1	0	1	0
1	1	0	0	1	1	0	0	1	1
1	1	1	1	1	1	1	1	1	1

d.

Present State			Next State			Output	FF Inputs		
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Y	D_2	D_1	D_0
0	0	0	1	0	0	0	0	0	0
0	0	1	0	0	0	1	1	0	0
0	1	0	0	0	1	0	1	0	1
0	1	1	1	0	1	1	0	0	1
1	0	0	0	1	0	0	1	1	0
1	0	1	1	1	0	1	0	1	0
1	1	0	1	1	1	0	0	1	1
1	1	1	0	1	1	1	1	1	1

Your answer is correct.

The correct answer is:

Present State			Next State			Output	FF	Inputs	
Q_2	Q_1	Q_0	Q_2	Q_1	Q_0	Y	D_2	D_1	D_0
0	0	0	0	0	0	0	0	0	0
0	0	1	1	0	0	1	1	0	0
0	1	0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	0	0	1
1	0	0	1	1	0	0	1	1	0
1	0	1	0	1	0	1	0	1	0
1	1	0	0	1	1	0	0	1	1
1	1	1	1	1	1	1	1	1	1

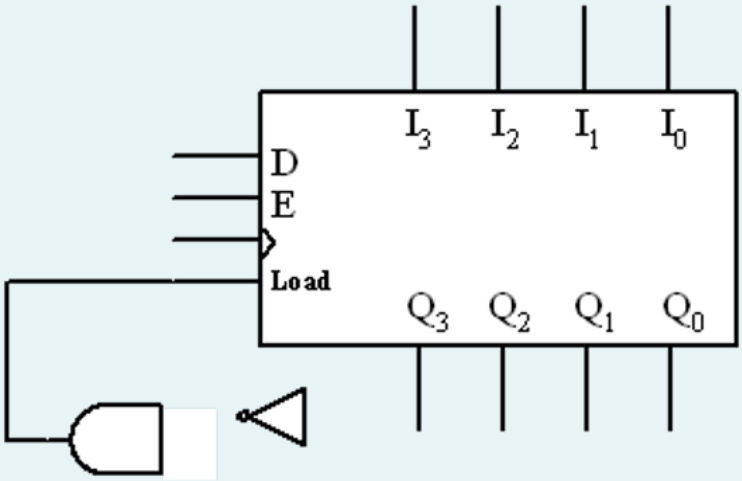
Question **10**

Correct

3.00 points out of 3.00

You are given the following 4-bit binary counter with input load capability through input pins I_3 to I_0. Note that E (Enable) and D (Disable) are control signals, and there is a clock input connected to the counter. You need to connect the counter and gates given in the figure without additional gates to count in the following sequence:

0, 1, 2, 3, 5, 6, 7, 13, 14, 15, 0, 1, 2, 3, 5, 6, 7, 13, 14, 15, 0...



(Hint: In binary it should count as: 0000-0001-0010-0011-0101-0110-0111-1101-1110-1111-0000-...)

What is the expression for Load input?

- a. Q3Q2'Q0
- b. Q3'Q1Q0 ✔
- c. Q2'Q1Q0
- d. Q3Q1Q0'

Your answer is correct.

The correct answer is:
Q3'Q1Q0

Question **11**

Incorrect

0.00 points out of 3.00

A register is defined as

- a. the group of latches suitable for storing 1 bit of information.
- b. the group of flip-flops suitable for storing 1 bit of information.
- c. the group of flip-flops suitable for storing binary information.
- d. the group of latches suitable for storing binary information. ✖

Your answer is incorrect.

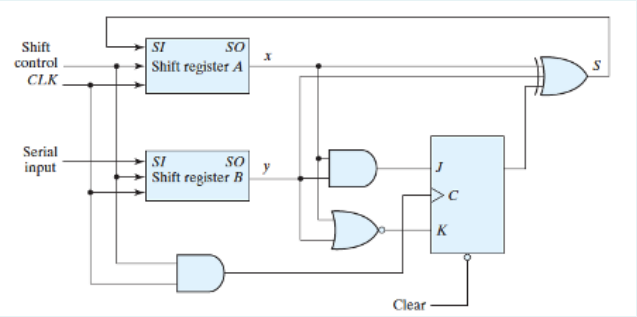
The correct answer is:
the group of flip-flops suitable for storing binary information.

Question **12**

Correct

3.00 points out of 3.00

The serial adder below uses two four-bit registers. Register A holds the binary number 0101 and register B holds 0111. The carry flip-flop is initially reset to 0. What are the binary values in register A and carry flip-flop after each shift?



- a. *A* = 0101, 0001,1000,1100 Carry = 1, 1, 1, 0
- b. *A* = 0010, 0001,1000,1100 Carry = 1, 0, 1, 0
- c. *A* = 0101, 0010, 0001,1000 Carry = 1, 0, 1, 0
- d. A = 0010, 0001,1000,1100 Carry = 1, 1, 1, 0 ✔

Your answer is correct.

The correct answer is:

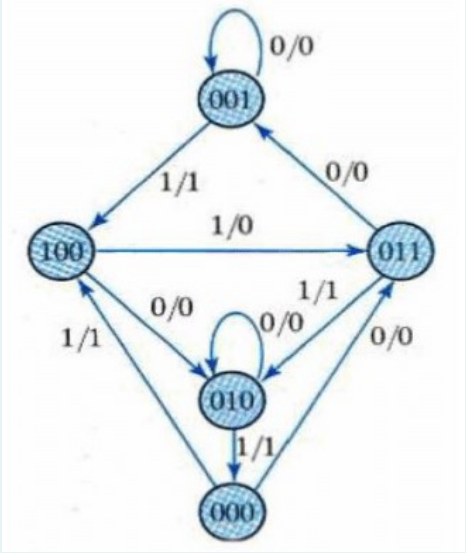
A = 0010, 0001,1000,1100 Carry = 1, 1, 1, 0

Question **13**

Correct

4.00 points out of 4.00

A sequential circuit has three D flip-flops *A, B,* and *C,* one input *x* and one output *y*. The state diagram is shown below. The circuit is designed by treating the unused states as don't care conditions. What are the next-state and output equations?



a. $D_A = A'B'x$
$D_B = A + BCx + C'x'$
$D_C = Ax' + A'B'x' + Cx'$
$Y = A$

b. $D_A = A'B'x$
$D_B = A + BCx + C'x'$
$D_C = Ax + A'B'x' + Cx'$
$Y = A'x$

c. $D_A = A'B'x$
$D_B = A + C'x + BCx$
$D_C = Ax + Cx'$
$Y = x$

d. $D_A = A'Bx$
$D_B = A + BCx + C'x'$
$D_C = Ax + A'B'x'$
$Y = A'$

Your answer is correct.

The correct answer is:
$D_A = A'B'x$
$D_B = A + BCx + C'x'$
$D_C = Ax + A'B'x' + Cx'$
$Y = A'x$

Question **14**

Correct

3.00 points out of 3.00

A DRAM chip uses two dimensional address multiplexing. The row address pins are 1 bit longer than the 15-bit column addresses. What is the capacity of the memory if it uses 1 byte words?

- a. 2 MB
- b. 2 GB ✔
- c. 64 KB
- d. 32 KB

Your answer is correct.

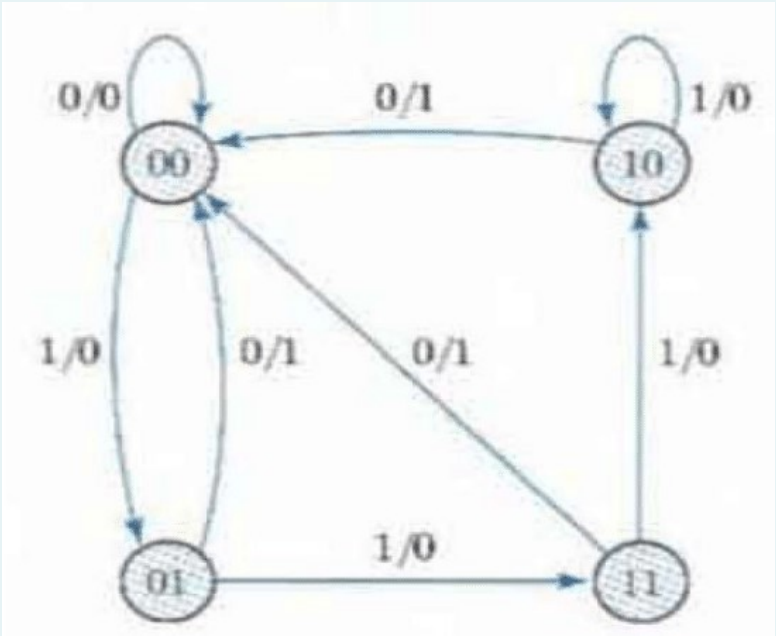
The correct answer is:
2 GB

Question **15**

Correct

4.00 points out of 4.00

Starting from state 00 in the state diagram below, what is the output sequence that will be generated when an input sequence of 11101100 is applied?



a. input: 1 1 1 0 1 1 0 0
output: 0 0 1 1 0 0 1 0

b. input: 1 1 1 0 1 1 0 0
output: 0 0 0 1 0 0 1 0 ✔

c. input: 1 1 1 0 1 1 0 0
output: 0 1 0 1 0 0 1 0

d. input: 1 1 1 0 1 1 0 0
output: 0 0 0 1 0 0 1 1

Your answer is correct.

The correct answer is:
input: 1 1 1 0 1 1 0 0
output: 0 0 0 1 0 0 1 0

Question **16**

Incorrect

0.00 points out of 3.00

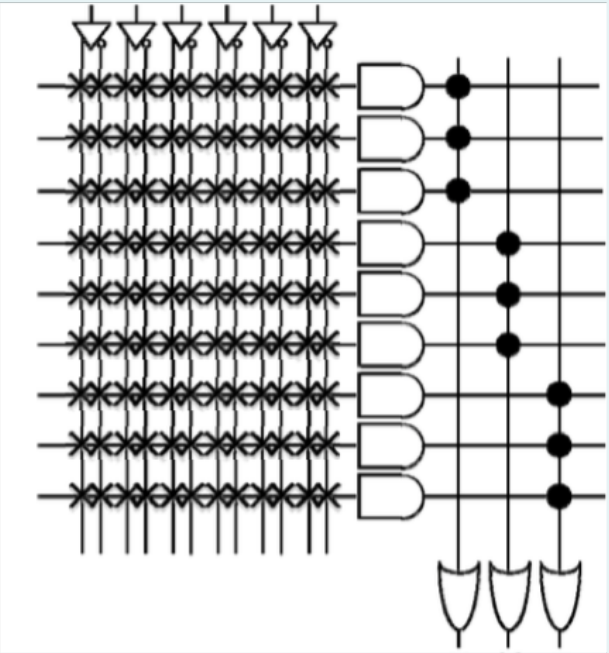
Given the following K-maps for two logic functions X and Y respectively. How would you program the function with the given PAL device below.

CD \ AB	00	01	11	10
00	0	0	1	0
01	0	0	0	1
11	1	0	0	0
10	0	1	0	0

X

CD \ AB	00	01	11	10
00	0	0	1	1
01	0	0	0	1
11	1	0	0	0
10	1	1	0	0

Y



a. X = AB'C'D + A'B'CD + Z
Y = AB'C' + A'B'C + Z
Z = ABC'D' + A'BCD'

b. X = ABC'D' + A'B'CD + A'BCD' + AB'C'D
Y = AC'D' + AB'C' + A'B'C + A'CD'

c. It can not be done with the given device

d. X = ABC'D' + A'BCD' + Z
Y = AB'C' + A'B'C + Z
Z = AB'C'D + A'B'CD

Your answer is incorrect.

The correct answer is:
X = AB'C'D + A'B'CD + Z

Y = AB'C' + A'B'C + Z

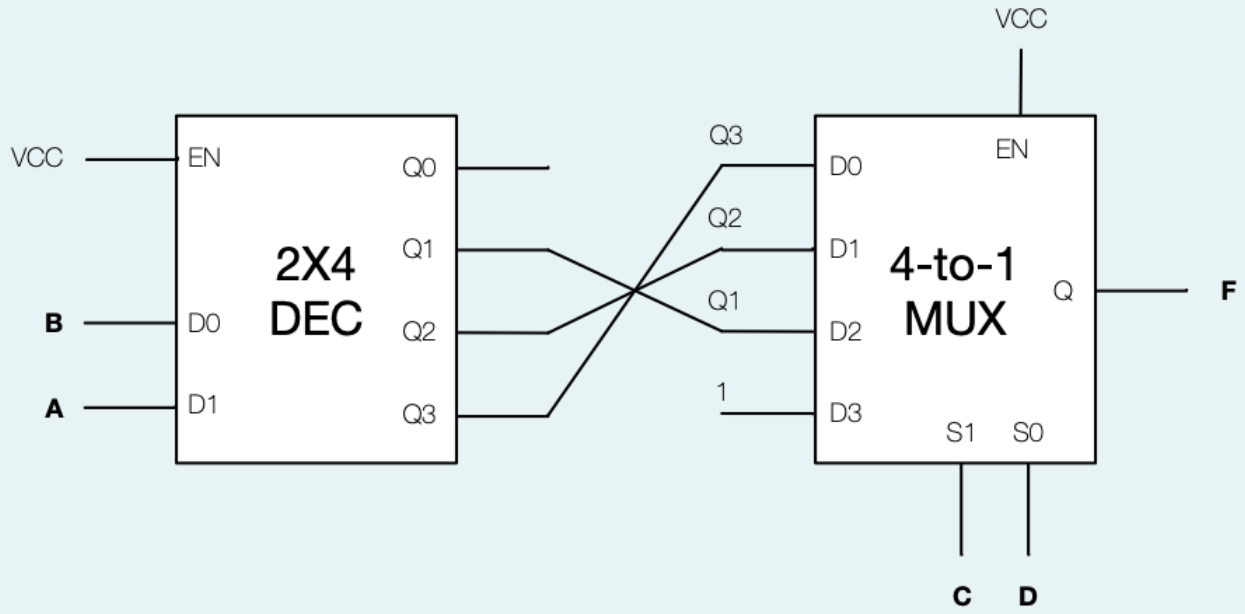
Z = ABC'D' + A'BCD'

Question **17**

Incorrect

0.00 points out of 3.00

Consider the following circuit with four inputs F(A,B,C,D) and a single output F. (Note that the cables do not touch where they cross.)



Assume that you will implement the given function using a ROM. There are _____ AND Gates in the smallest ROM that implements this function. Now, assume that you will implement the given function using a PAL instead of a ROM. The smallest number of AND Gates needed by a PLA implementation of this function is _____.

Choose the option to complete the given sentence in a correct way.

- a. 8 - 4
- b. 8 - 3 ✖
- c. 16 - 4
- d. 16 - 8

Your answer is incorrect.

The correct answer is:
16 - 4

Question **18**

Correct

3.00 points out of 3.00

When a HIGH is applied to the S and LOW input applied to the R input of an **SR latch**, then

a. Both Q and Q' outputs go HIGH.

b. Q' output goes HIGH.

c. Q output goes LOW.

d. Q output goes HIGH. ✔

Your answer is correct.

The correct answer is:
Q output goes HIGH.

Question **19**

Correct

3.00 points out of 3.00

An asynchronous counter differs from a synchronous counter in

a. the number of states in its sequence

b. the method of clocking ✔

c. the use of self correction mechanism

d. the type of flip-flops used

Your answer is correct.

The correct answer is:
the method of clocking

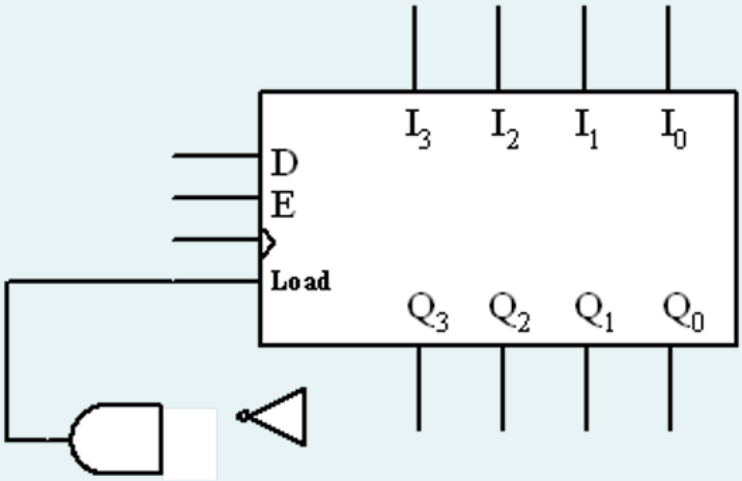
Question **20**

Correct

3.00 points out of 3.00

You are given the following 4-bit binary counter with input load capability through input pins I_3 to I_0. Note that E (Enable) and D (Disable) are control signals, and there is a clock input connected to the counter. You need to connect the counter and gates given in the figure without additional gates to count in the following sequence:

0, 1, 2, 3, 5, 6, 7, 13, 14, 15, 0, 1, 2, 3, 5, 6, 7, 13, 14, 15, 0...



(Hint: In binary it should count as: 0000-0001-0010-0011-0101-0110-0111-1101-1110-1111-0000-...)

What is the expression for I_3 input?

- a. Q0
- b. Q2 ✔
- c. Q1
- d. Q3

Your answer is correct.

The correct answer is:
Q2

Question **21**

Correct

3.00 points out of 3.00

The logic circuits whose outputs at any instant of time depends not only on the present input but also on the past outputs are called

- a. combinational circuits.
- b. sequential circuits. ✔
- c. short circuits.
- d. series circuits.

Your answer is correct.

The correct answer is:
sequential circuits.

Question **22**

Correct

4.00 points out of 4.00

Consider the design of a simple elevator controller. The building has two floors, an UP button on the first floor, a DOWN button on the second floor, and two buttons (FIRST and SECOND) inside the elevator indicating the floor to go to. While you can make assumptions, the behavior of the system has to be reasonable. For example, pressing the "SECOND" button with the elevator on the second floor causes the elevator to remain there with its door OPEN. Assume no buttons can be pressed simultaneously.

Show the state diagram of this problem, labeling all state transitions. Use the input / output representational conventions when labeling the state transitions.

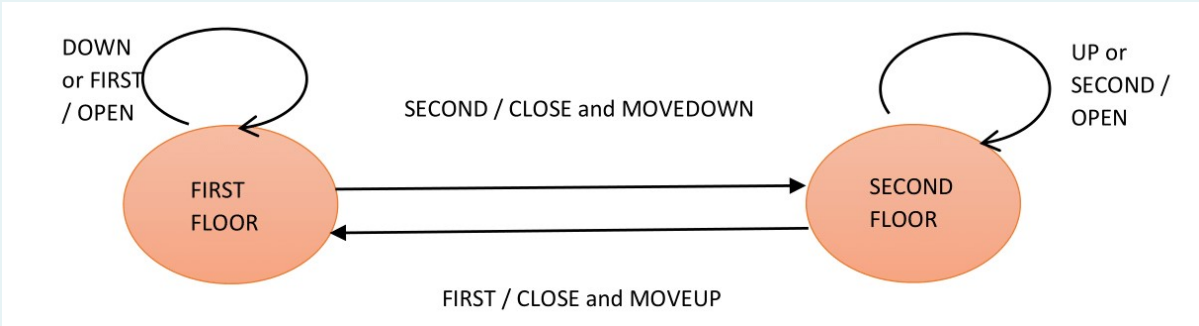
INPUTS: UP, DOWN, FIRST, SECOND

OUTPUTS: MOVEDOWN, MOVEUP, OPEN, CLOSE

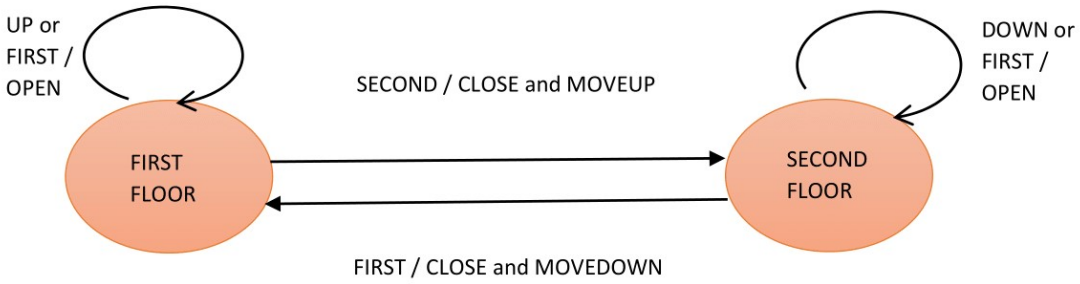
STATES: FIRST FLOOR

SECOND FLOOR

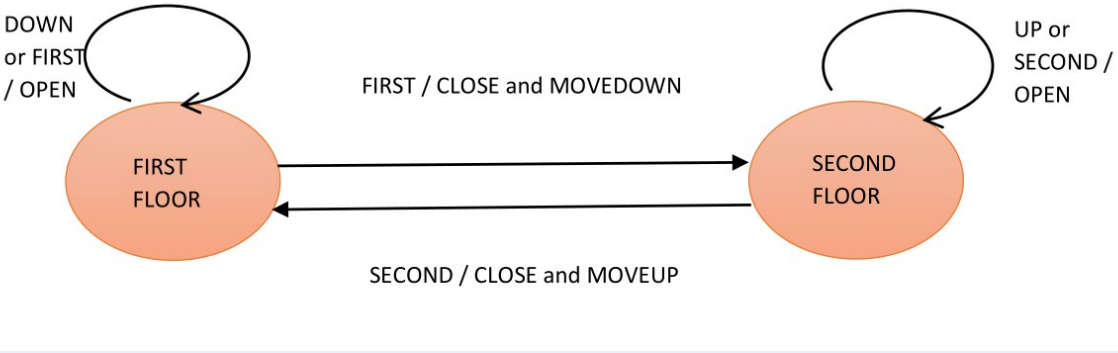
- a.



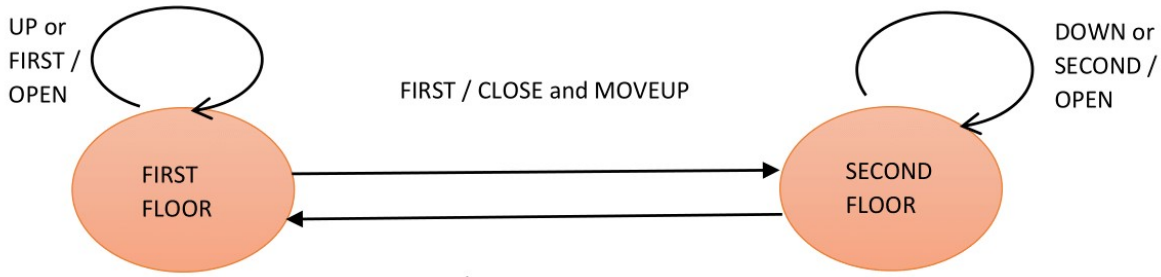
b.



c.

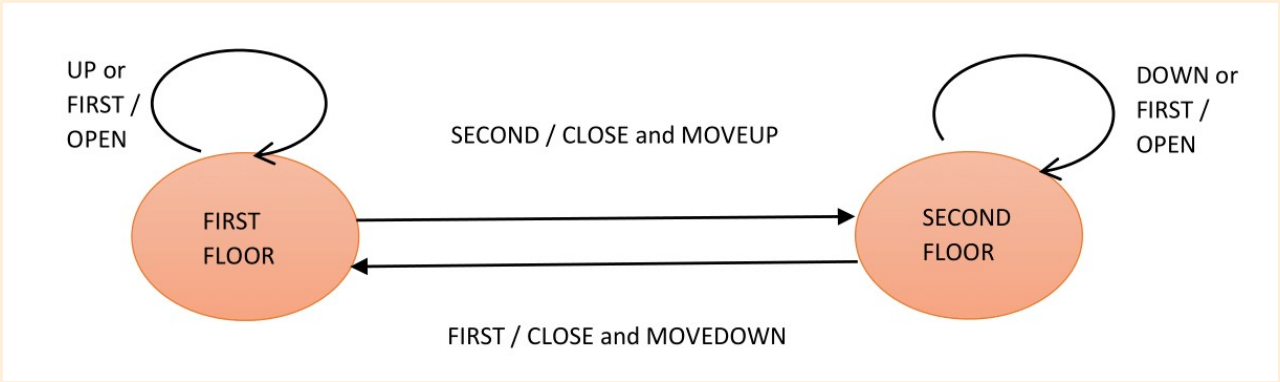


d.



Your answer is correct.

The correct answers are:



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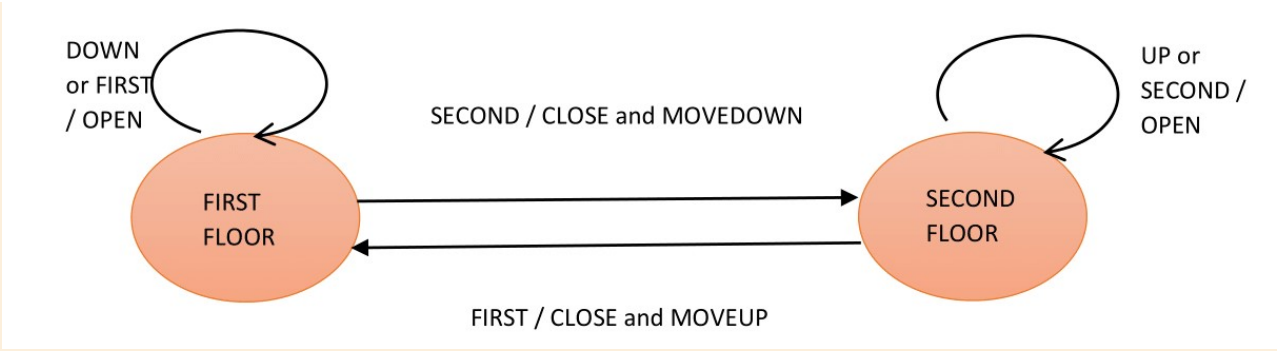
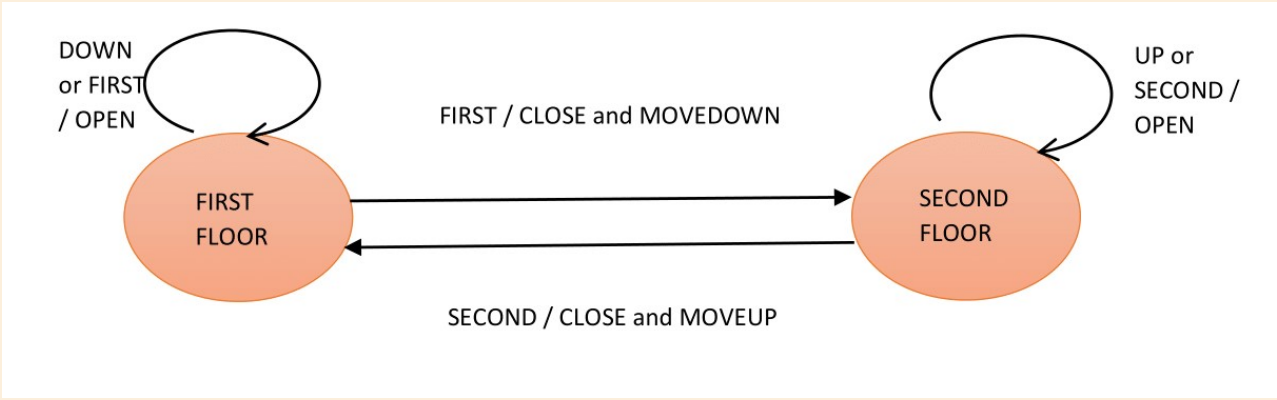
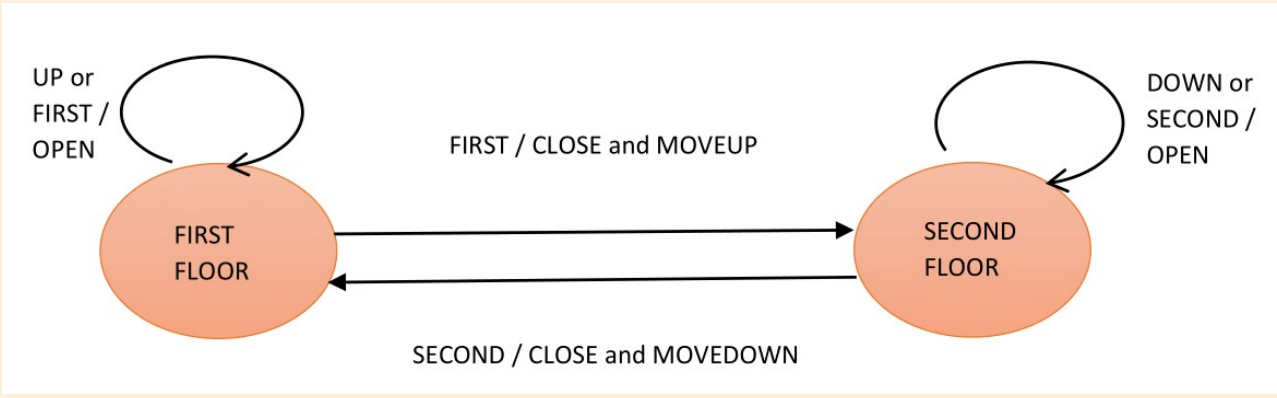






Question **23**

Correct

3.00 points out of 3.00

The register is a type of

- a. sequential circuit. ✔
- b. central processing unit (CPU).
- c. combinational circuit.
- d. latches.

Your answer is correct.

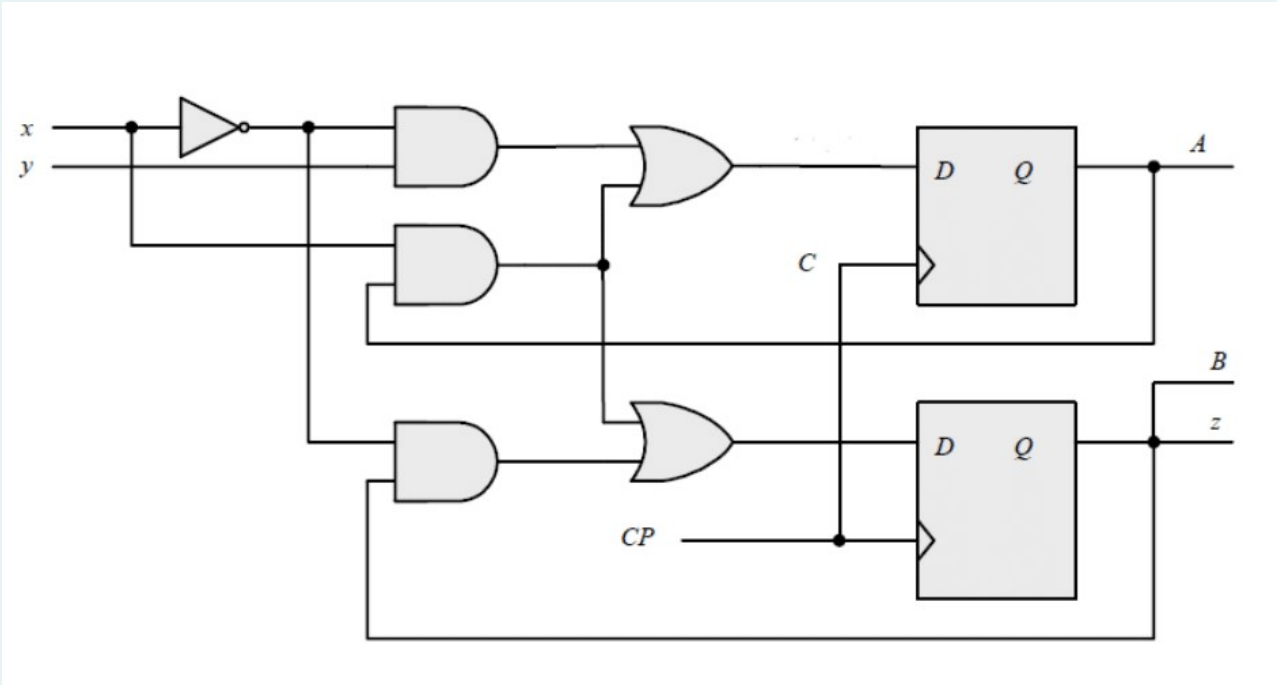
The correct answer is:
sequential circuit.

Question **24**

Correct

4.00 points out of 4.00

Given the circuit diagram below, what are the next-state and output equations ?



a. A(t+1) = x′y + xB
B(t+1) = x′A + xB
Z = B

b. A(t+1) = x′y + xA
B(t+1) = x′A + x′B
Z = A

c. A(t+1) = x′y + xA
B(t+1) = xA + x′B
Z = B ✔

d. A(t+1) = x y + xB
B(t+1) = x′A + xB
Z = A

Your answer is correct.

The correct answer is:
A(t+1) = x′y + xA
B(t+1) = xA + x′B
Z = B

Question **25**

Correct

3.00 points out of 3.00

The main difference between a register and a counter is:

- a. a register has no specific sequence of states. ✔
- b. a counter has no specific sequence of states.
- c. a register has capability to store 1 bit of information, but counter can store n-bits.
- d. a register counts data.

Your answer is correct.

The correct answer is: a register has no specific sequence of states.

Question **26**

Incorrect

0.00 points out of 3.00

In order to build a RAM with 64-byte total storage capacity and a word size of 8 bits using 32x4 RAMs and decoders, we need _____ bit address lines, we need _____ 32x4 RAM chips together with _____ decoder(s) to build the RAM.

- a. 6 – 4 – 1
- b. 8 – 2 – 1 ✖
- c. 8 – 2 – 0
- d. 6 – 4 – 0

Your answer is incorrect.

The correct answer is:
6 – 4 – 0

Question **27**

Correct

3.00 points out of 3.00

The difference between a flip-flop and a latch is:

- a. both are the same.
- b. a flip-flop consists of an extra output.
- c. a latch is a level sensitive device while a flip-flops is an edge sensitive device. ✔
- d. a latch has two inputs but a flip-flop has one input.

Your answer is correct.

The correct answer is:
a latch is a level sensitive device while a flip-flops is an edge sensitive device.

Question **28**

Correct

3.00 points out of 3.00

Which of the following statements is correct about memory?

- a. ROM is a random output memory
- b. Stored data is lost if power is removed from a static RAM ✔
- c. A memory cell can store a byte of data
- d. The read operation erases the data byte

Your answer is correct.

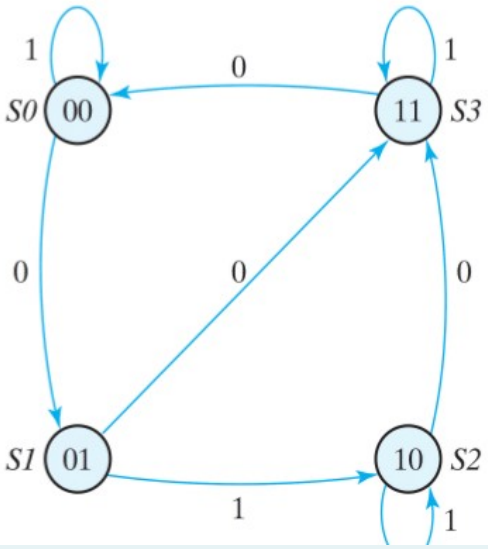
The correct answer is:
Stored data is lost if power is removed from a static RAM

Question **29**

Correct

4.00 points out of 4.00

Given the state diagram below, what are the next state equations if we use T-FFs in the circuit?



Q(t)	Q(t = 1)	T
0	0	0
0	1	1
1	0	1
1	1	0

(b) T

a. $T_A = A'B + Bx'$
$T_B = A'x + Bx' + A'Bx$

b. $T_A = AB + Bx'$
$T_B = A'x + Bx' + A'Bx$

c. $T_A = A'B + Bx'$
$T_B = Ax' + Bx' + A'Bx$

d. $T_A = AB' + Bx'$
$T_B = B'x' + Ax' + AB'x$

Your answer is correct.

The correct answer is:

$T_A = A'B + Bx'$
$T_B = Ax' + Bx' + A'Bx$

Question **30**

Incorrect

0.00 points out of 3.00

A J-K flip-flop with J = 1 and K = 1 has a 20 kHz clock input. The Q output is

a. constantly LOW.

b. a 10 kHz square wave.

c. constantly HIGH.

d. a 20 kHz square wave. ✖

Your answer is incorrect.

The correct answer is: a 10 kHz square wave.

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232-Lecture-9-Algorithmic-State-Machines-v2.0 ►