CENG 232 - Introduction to Labs

Middle East Technical University

Department of Computer Engineering

Introduction

Logic Design Labs

Logic Programming Labs

Grading Policy

Cheating Policy

INTRODUCTION

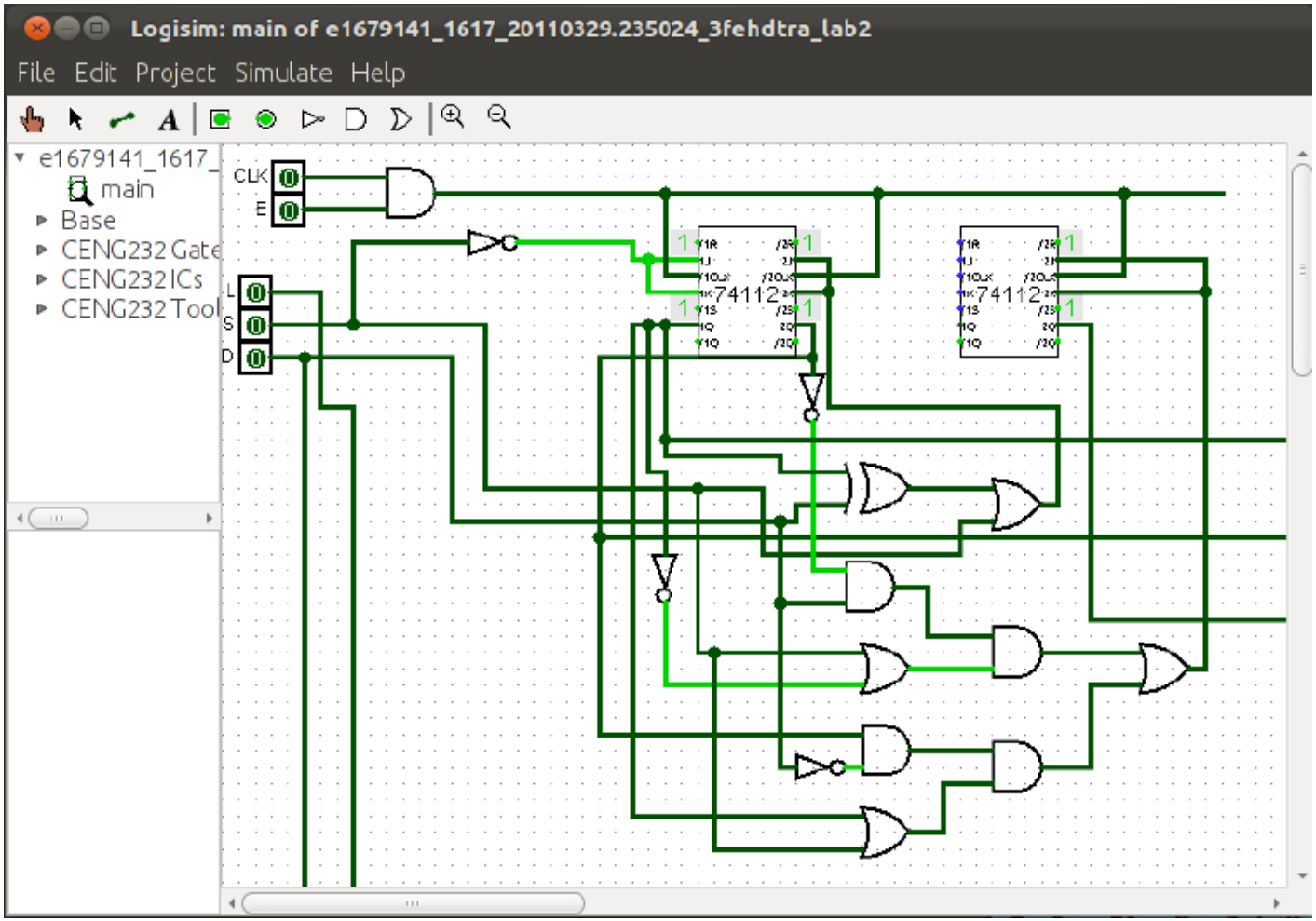
- **4 labs**
  - 2 labs: Logic Design & Hardware Implementation
  - 2 labs: Logic Programming & FPGA
- **Logic Design & Hardware Implementation:**
  - 1 free session.
  - 1 demo session.
  - At hardware lab (Computer center building, second floor).
- **Logic Programming & FPGA:**
  - 2 parts.
  - From computer, no attendance.
  - First part, individual (verilog).
  - Second part, individual (verilog + FPGA).
    - Demo, if needed.

Logic Design Labs (1)

- First 2 labs.
- Each lab has: preliminary work, and lab implementation consisting of 1 free session and 1 demo session.
- **Preliminary work:**
  - Design your circuits on paper.
  - Draw them with Logisim.
  - Try to find minimal circuits since you will have to implement them in hardware. (You will implement your own circuit in demo.)
  - If you don't post the preliminary work, you can only attend the quiz at the beginning of the demo session. You will not be allowed to attend the rest of the demo session.

LOGIC DESIGN LABS (2)

- Preliminary Work (Logisim):



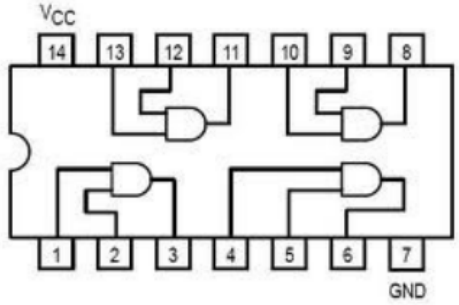
Logic Design Labs (3)

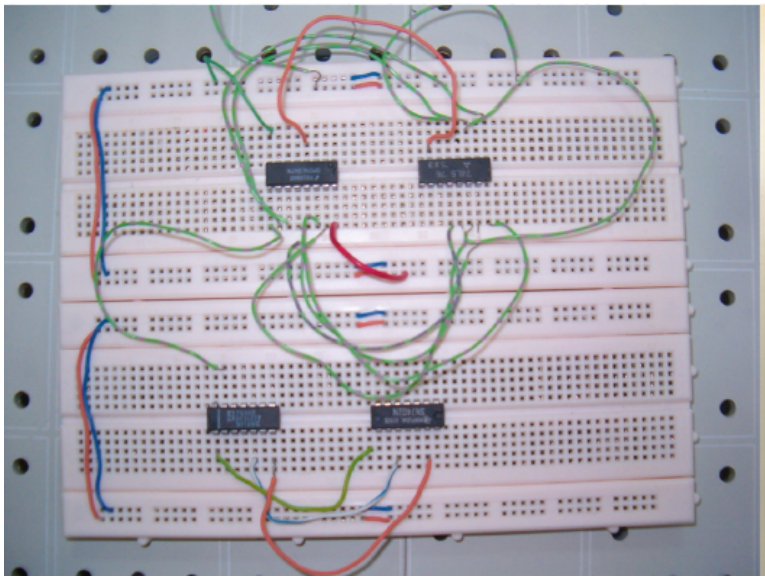
- **Lab implementation:**
  - You have two weeks: one free session and one demo session.
  - Done in hardware lab. (Computer center building, second floor.)
  - With cadets, breadboards, integrated circuits, cables.
  - Two students share a cadet for testing.
  - But this is an individual task, everyone implements their own circuit individually.

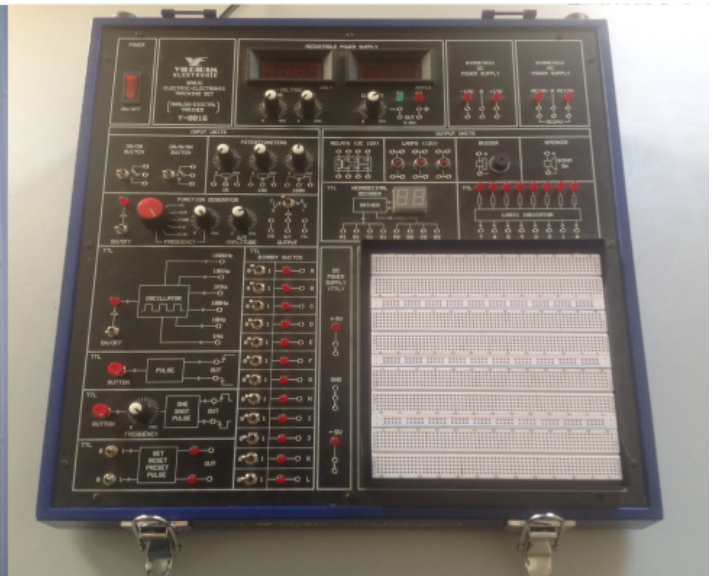
Logic Design Labs (4)

- **Free Session (1 Week):**
  - You will have 2 hours in Hardware Lab, attendance is not mandatory (but strongly recommended).
  - Assistants explain the circuit elements and show how they work.
  - You can familiarize yourself with the circuit elements.
  - Try to build your circuit. (That you will build in the demo!)
  - Find out practical problems. Learn how to debug & fix them.
- **Demo Session (1 Week):**
  - You will have 2 hours, attendance is mandatory.
  - It is graded, you have a quiz in the first 10, 15 minutes.
  - Preliminary work and quiz attendance are mandatory to attend the demo sessions.
  - You will build the same circuit in 2 hours and get graded.

Logic Design Labs (5)








CABLES
CABLES EVERYWHERE
Meme creator.org

Logic Programming & FPGAs (1)

- Last 2 assignments.
- Moving our focus from combinational logic circuits to sequential logic circuits.
- Design larger projects with Verilog language.
- Simulate & test them on your computers.
- Compile and deploy on an FPGA board (which will be provided to you).
  - FPGA: Field Programmable Gate Array
- FPGA boards are integrated circuits that can be configured (programmed).
- Usually hardware description languages are used to do this configuration.

LOGIC PROGRAMMING & FPGAS (2)

- **Preliminary Work (2 Weeks):**
  - The assignments will have two parts.
  - **First Part:**
    - Individually design your project with Verilog.
    - Simulate and test it with Xilinx tool.
  - **Second Part:**
    - Design your project with Verilog and simulate with Xilinx.
    - Deploy it to FPGA and physically test it.

Grading Policy

- **Logic Design Labs:**
  - Preliminary work is graded **black-box** with grader.
  - Demo lab quiz.
  - Demo circuits are graded **black-box** according to output.
  - Non-logical circuits won't take grade (always producing 0 or 1 etc.).
  - Percentages of these will be announced later.
- **Logic Programming Labs:**
  - For the first part, simulation results will be tested with test benches.
  - Second part will be physically tested.
  - Percentages of these will be announced later.
- For all of the labs and homeworks, obey the specifications and double check before sending.

Cheating Policy

- **Logisim work and their labs:**
  - Completely individual.
  - Design your own circuit.
  - Share cadet in lab but build your own circuit.
- **Verilog** & **FPGA work:**
  - Both parts should be implemented individually.
- Taking any sources directly from internet or from a friend/group (a part of it or as a whole) is strictly forbidden.
- According to university rules disciplinary action will be applied in any case of cheating.
- If you need help, do not hesitate to ask questions to your assistants instead of cheating.