Lecture 5-Sequential Circuit Design Examples

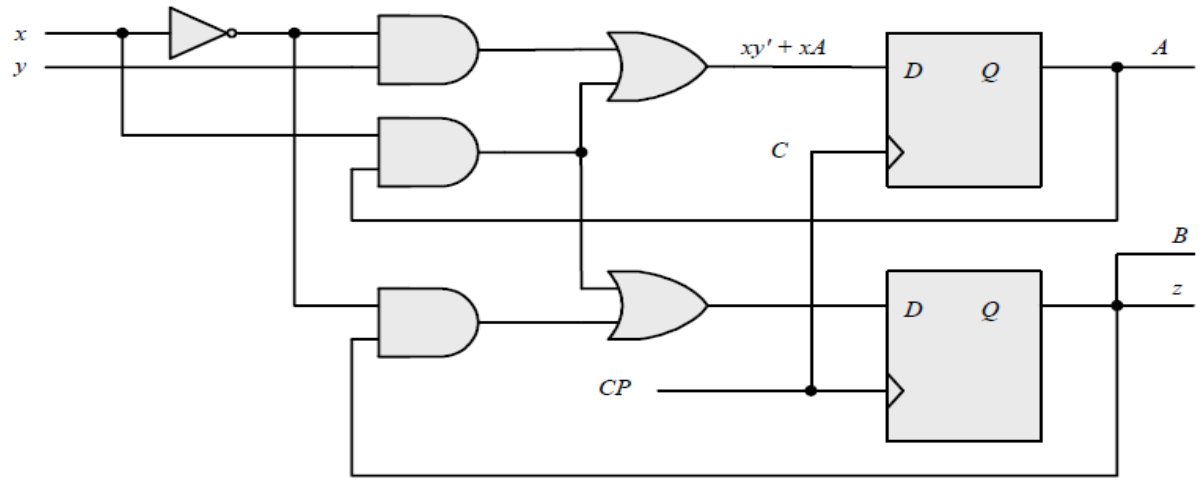
FNA

Ex 1. A sequential circuit with two *D* flip-flops A and B, two inputs x and y, and one output z is specified by the following next-state and output equations

$$A(t+1) = x'y + xA$$
$$B(t+1) = x'B + xA$$
$$Z = A$$

(a) Draw the logic diagram of the circuit.
(b) List the state table for the sequential circuit.
(c) Draw the corresponding state diagram.

(a)

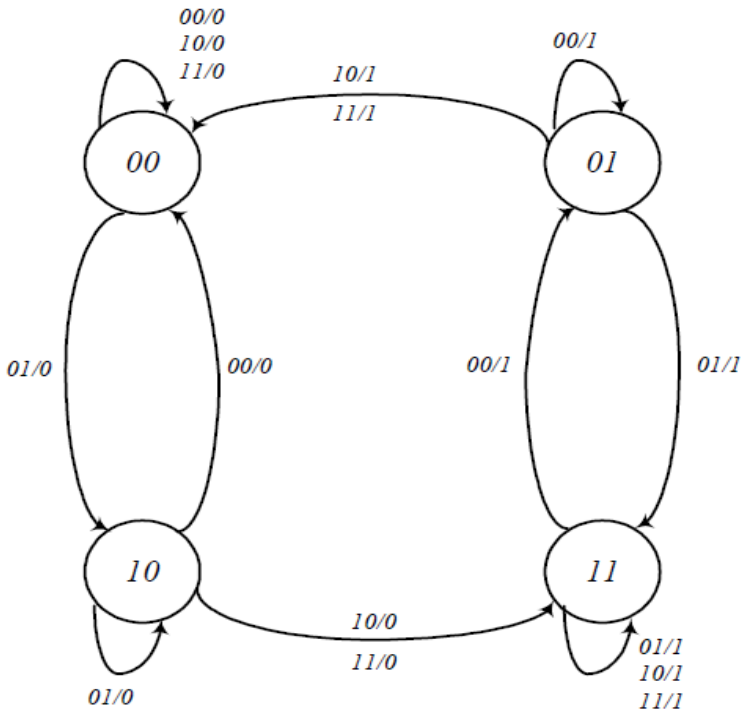


$$A(t+1) = x'y + xA$$
$$B(t+1) = x'A + xA$$
$$Z = A$$

(b)

Present state		Inputs		Next state		Output
A	B	x	y	A	B	z
0	0	0	0	0	0	0
0	0	0	1	1	0	0
0	0	1	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	1	1
0	1	0	1	1	1	1
0	1	1	0	0	0	1
0	1	1	1	0	0	1
1	0	0	0	0	0	0
1	0	0	1	1	0	0
1	0	1	0	1	1	0
1	0	1	1	1	1	0
1	1	0	0	0	1	1
1	1	0	1	1	1	1
1	1	1	0	1	1	1
1	1	1	1	1	1	1

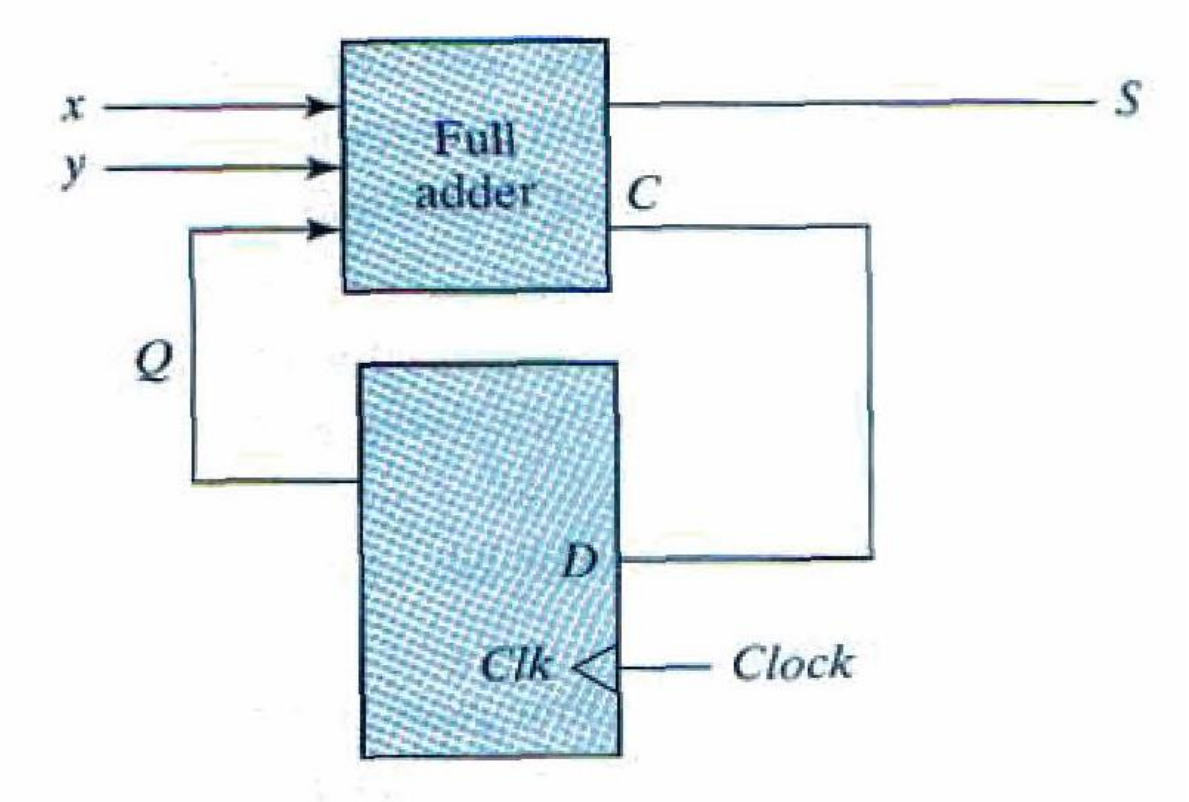
(c)



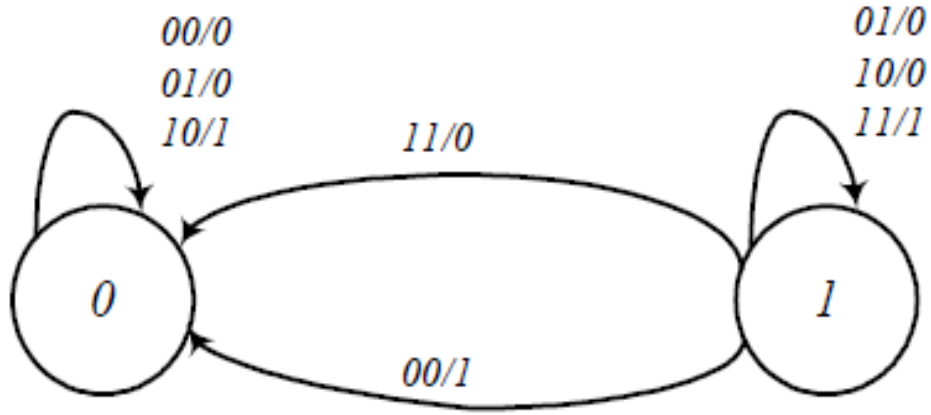
D Flip-Flop

D	Q(t + 1)	
0	0	Reset
1	1	Set

Ex 2. A sequential circuit has one flip-flop Q, two inputs x and y, and one output S. It consists of a full-adder circuit connected to a *D* flip-flop, as shown in the figure below. Derive the state table and state diagram of the sequential circuit.



Present state	Inputs		Next state	Output
Q	x	y	Q	S
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



$$S = x \oplus y \oplus Q$$

$$Q(t+1) = xy + xQ + yQ$$

D Flip-Flop

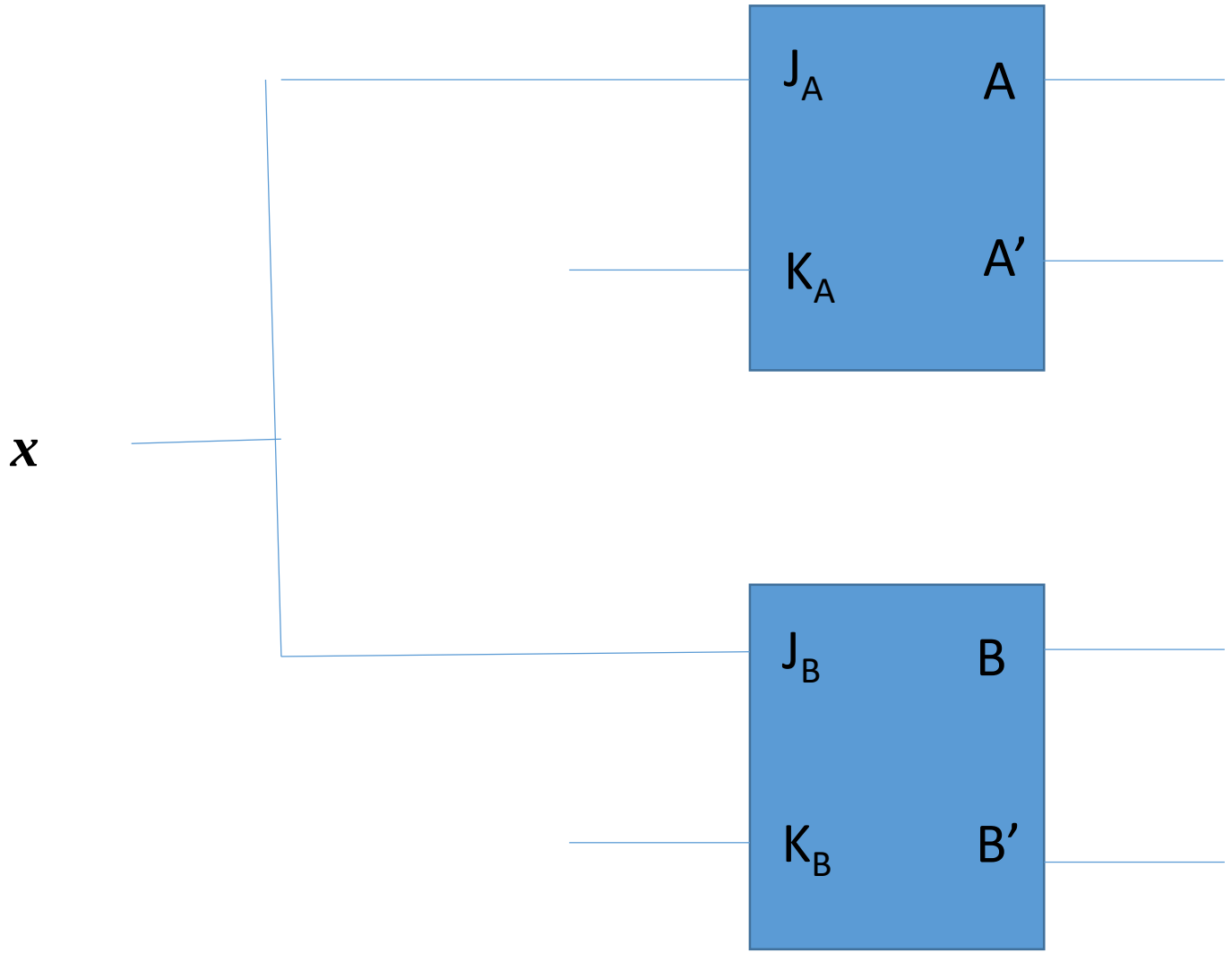
D	Q(t + 1)	
0	0	Reset
1	1	Set

Ex 3. A sequential circuit has two *JK flip-flops* A and B and one input x. The circuit is described by the following flip-flop input equations:

$$J_A = x \quad K_A = B'$$
$$J_B = x \quad K_B = A$$

(a) Derive the state equations A(t+1) and B(t+1) by substituting the input equations for the variables J and K.
(b) Derive the state diagram of the circuit.

$$J_A = x \quad K_A = B'$$
$$J_B = x \quad K_B = A$$



Characteristic Equations

- We can also write characteristic equations, where the next state Q(t+1) is defined in terms of the current state Q(t) and inputs.

D	Q(t+1)	Operation
0	0	Reset
1	1	Set

$$Q(t+1) = D$$

J	K	Q(t+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Q'(t)	Complement

$$Q(t+1) = K'.Q(t) + J.Q'(t)$$

T	Q(t+1)	Operation
0	Q(t)	No change
1	Q'(t)	Complement

$$Q(t+1) = T'.Q(t) + T.Q'(t)$$
$$= T \oplus Q(t)$$

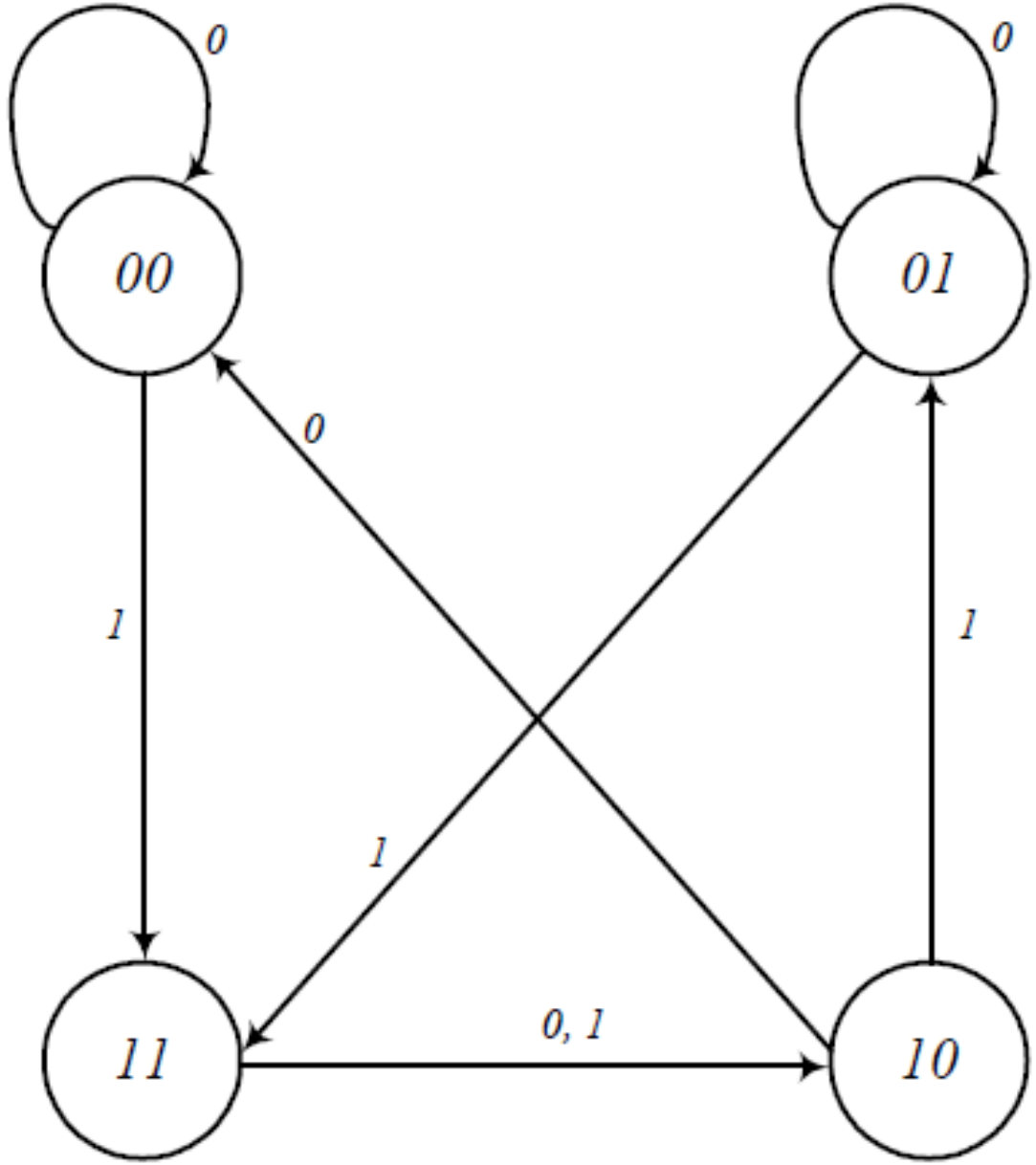
A	B	x	J_A	K_A	J_B	K_B	A	B
0	0	0	0	1	0	0	0	0
0	0	1	1	1	1	0	1	1
0	1	0	0	0	0	0	0	1
0	1	1	1	0	1	0	1	1
1	0	0	0	1	0	1	0	0
1	0	1	1	1	1	1	0	1
1	1	0	0	0	0	1	1	0
1	1	1	1	0	1	1	1	0

$$J_A = x \quad K_A = B'$$
$$J_B = x \quad K_B = A$$

$$A(t+1) = J_A A' + K'A = xA' + BA$$
$$B(t+1) = J_B B' + K'_B B = xB' + A'B$$

JK Flip-Flop

J	K	Q(t + 1)
0	0	$Q(t)$
0	1	0
1	0	1
1	1	$Q'(t)$



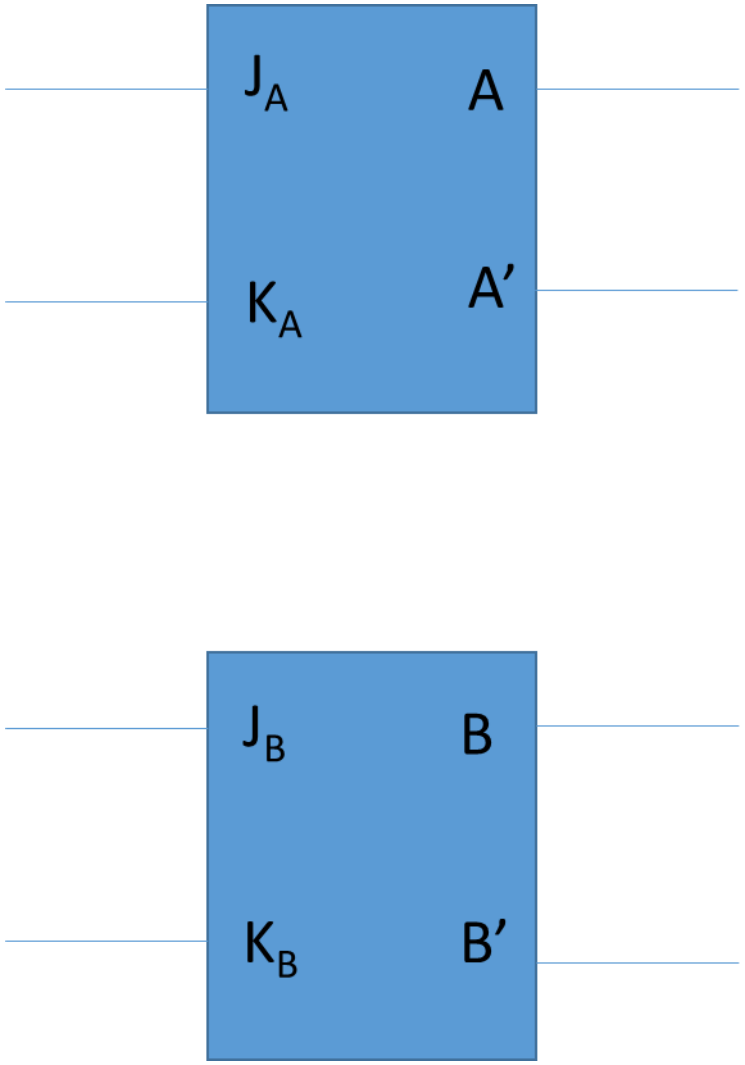
Ex 4. A sequential circuit has two *JK flip-flops* A and B, two inputs x and y, and one output z. The flip-flop input equations and the circuit output equation are:

$$J_A = Bx + B'y' \qquad K_A = B'xy'$$
$$J_B = A'x \qquad K_B = A + xy'$$
$$z = Ax'y' + Bx'y'$$

(a) Draw the logic diagram of the circuit.
(b) Tabulate the state table.
(c) Derive the state equations for A and B.

(a) $J_A = Bx + B'y'$ $J_B = A'x$

$K_A = B'xy'$ $K_B = A + xy'$ $z = Axy + Bx'y'$



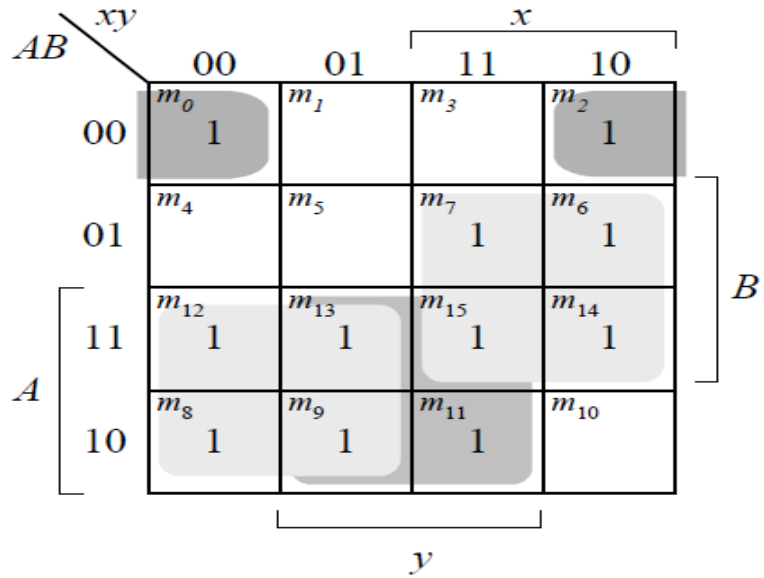
(a) $J_A = Bx + B'y'$ $\quad J_B = A'x$

$K_A = B'xy'$ $\quad K_B = A + xy'$ $\quad z = Axy + Bx'y'$

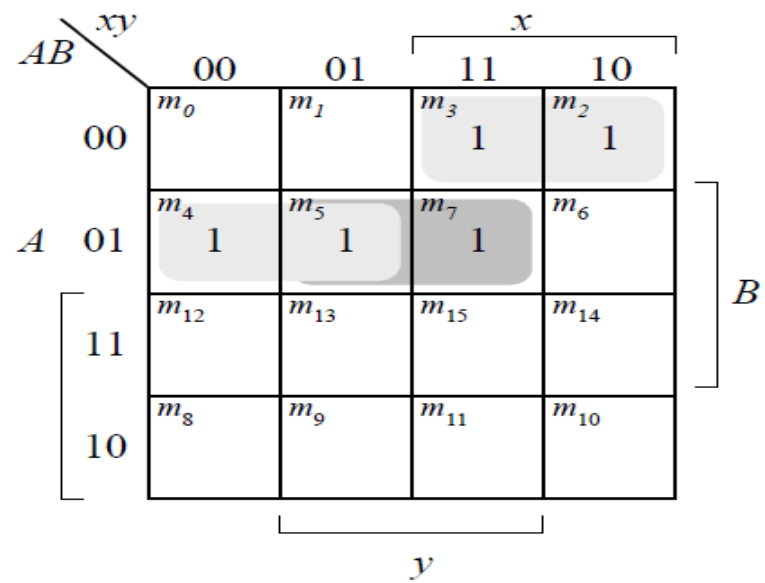
(b)

Present state		Inputs		Next state		Output	FF Outputs			
A	B	x	y	A	B	z	J_A	K_A	J_A	J_B
0	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	0	0	0	0	0	0
0	0	1	0	1	1	0	1	1	1	1
0	0	1	1	0	1	0	0	0	1	0
0	1	0	0	0	1	1	0	0	0	0
0	1	0	1	0	1	0	0	0	0	0
0	1	1	0	1	0	0	1	0	1	0
0	1	1	1	1	1	0	1	0	1	0
1	0	0	0	1	0	0	1	0	0	1
1	0	0	1	1	0	0	0	0	0	1
1	0	1	0	0	0	0	1	1	0	1
1	0	1	1	1	0	0	0	0	0	1
1	1	0	0	1	0	1	0	0	0	1
1	1	0	1	1	0	0	0	0	0	1
1	1	1	0	1	0	0	1	0	0	1
1	1	1	1	1	0	1	1	0	0	1

(c)

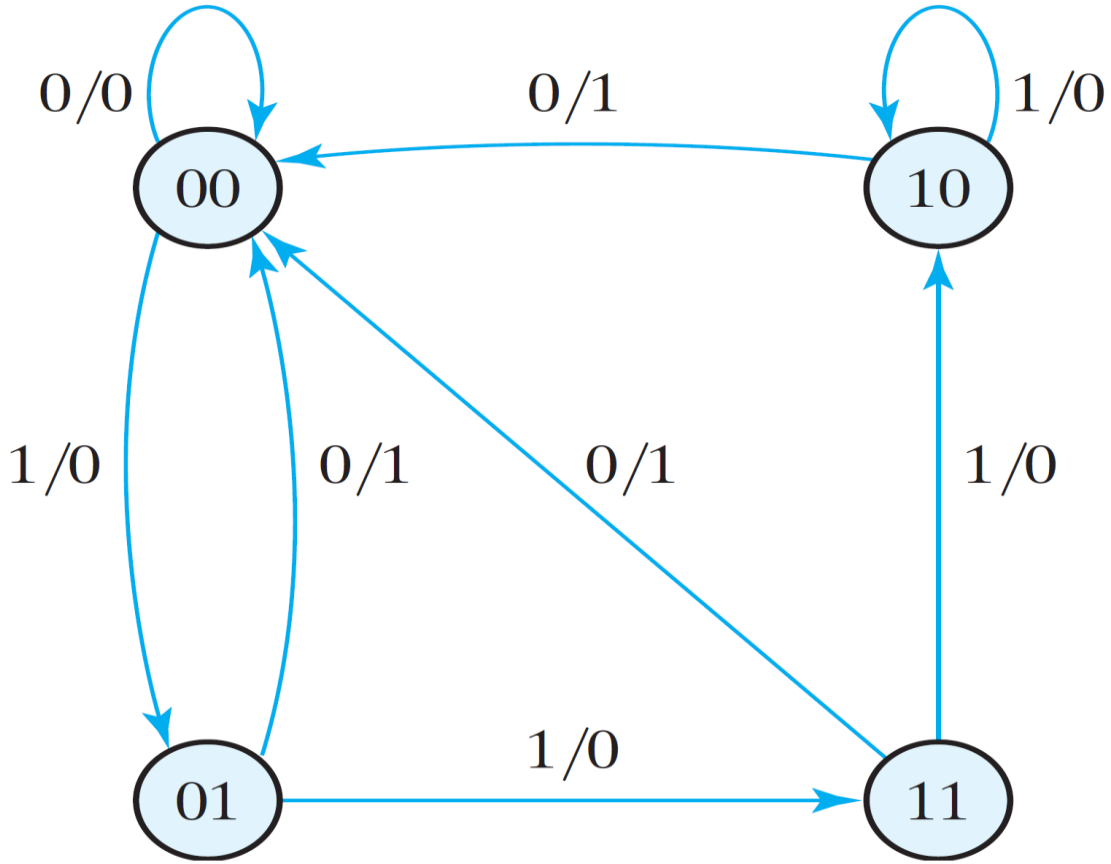


$A(t+1) = Ax' + Bx + Ay + A'B'y'$



$B(t+1) = A'B'x + A'B'(x' + y)$

Ex 5. Starting from state 00 in the state diagram below, determine the state transitions and output sequence that will be generated when an input sequence of 0101 101 1101 1110 is applied.



Work …

- Design a sequential circuit that detects 01 patterns coming through an input line X. The circuit's output Z should be set 1 when a 01 pattern occurs and to 0 otherwise.

X	0111001000010
Z	0100000100010

- Draw the state diagram of the circuit
- Derive the state table
- Implement using D-FF's
  - Extend the state table for D-FF inputs
  - Derive the expressions for D-FF inputs
  - Draw the full circuit