ElecEng 2CF3

ASSIGNMENT 1

Basic Circuits with Idealized Op-amp Model

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Instructions and Objective

- Perform all exercises.
- For each exercise, there are instructions on what to include in a short report about your observations. The report also must contain the answers to the posed questions.
- For each exercise, you are required to submit: (i) your final *LTspice* (`*.asc`) file and (ii) your short report (`*.pdf`) file. Submit to the respective Dropbox on A2L by the respective deadline. Do not include intermediate `*.asc` files. Failure to submit either in the correct file format will be penalized.
- Each exercise report (the PDF) must include (at the top of the first page) a suitable short title, your full name as it appears on Avenue to Learn, your student ID number, and your MacID login name.

The objective of this assignment is to introduce the students to the simulation of two basic op-amp circuits using a circuit simulator (*LTspice XVII*). To get familiar with *LTspice*, refer to the Quick Guide,

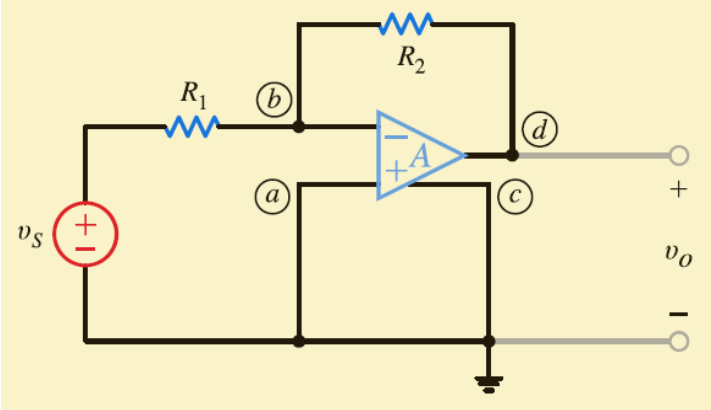
`LTSPICE_QuickStartGuide.pdf`

available for download from the Content folder in the A2L course shell.

The two op-amp circuits studied here are: 1) the inverting op-amp circuit, and 2) the non-inverting op-amp circuit. Three fundamental limitations of the op-amp circuit are examined: (i) the limitation of the DC power supply voltages V_{CC} and V_{EE} on the range of the output voltage V_o, (ii) the limitation on the output current I_o, and (iii) the impact of a finite-gain value A_o on the op-amp circuit output. Remember that the ideal op-amp model assumes that $A_o \to \infty$.

EXERCISE #1: *INVERTING OP-AMP CIRCUIT*

The inverting op-amp circuit is shown in Fig. 1 along with its voltage gain g assuming an ideal op-amp.



$$g = \frac{v_o}{v_S} = -\frac{R_2}{R_1}$$

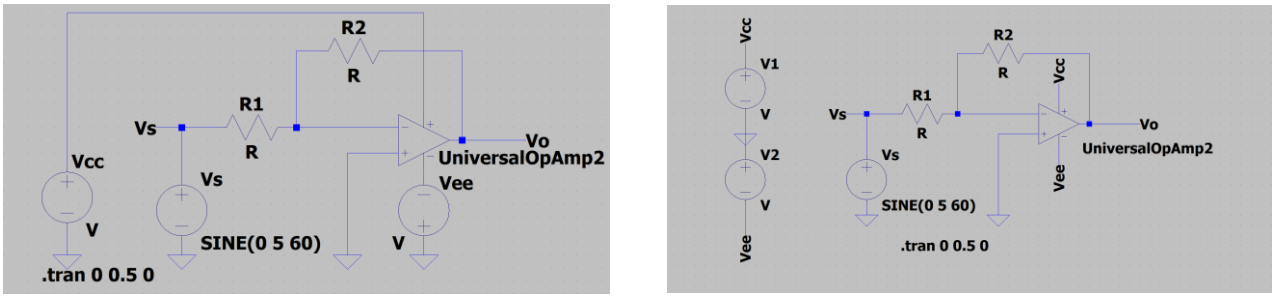
(a) (b)

Fig. 1. (a) The inverting op-amp circuit. (b) Its voltage gain assuming an ideal op-amp.

Perform the following tasks.

A. Create the LTspice Schematic

Example schematics are shown in Fig. 2a and Fig. 2b. Notice that the schematic in Fig. 2b avoids the need to draw wires from the DC voltage sources to the op-amp by making use of node labels – the labels at the V_{CC} and V_{EE} op-amp terminals are the same as those on the DC voltage sources.



(a) (b)

Fig. 2. The inverting op-amp circuit realized in *LTspice* schematics: (a) with direct wiring of the voltage DC supplies; (b) with indirect specification of the DC voltages using net labels.

The op-amp component is found through the `Component` tool  , then double-click `[OpAmps]`, and scroll right to select `UniversalOpamp2`.

The signal voltage source V_S is set as a sine source of magnitude 5 V and frequency 60 Hz. To set this source, hover the mouse over the voltage-source component until you see a pointing hand; then right click. A window pops up, where you can set up your source as shown in Fig. 3.

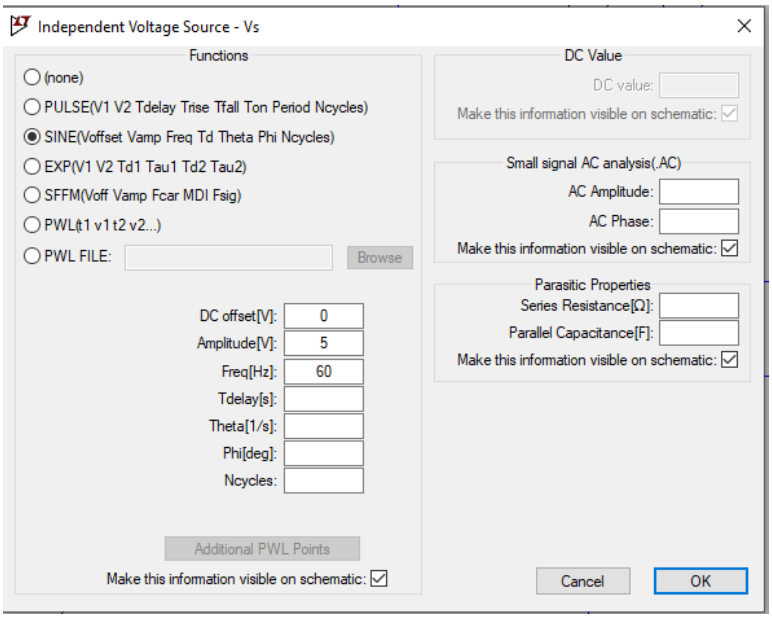


Fig. 3. Set up of the input-signal voltage source in *LTspice*.

You will notice that we have placed net (or wire) labels at the signal source terminal (`Vs`) and the circuit output terminal (`Vo`).

Set the value of the resistor `R1` to be equal to the sum of the last two digits of your student number in kΩ. For example, if the last two digits of your student ID are `63`, then set $R_1 = 9$ kΩ. To set this value, right-click on the label `R` under the `R1` resistor. A window will pop up, where you can enter the resistance

value. In our example, that would be `9k` or, equivalently, `9e3`.

Your circuit must exhibit a voltage-gain value of $g = -10$. Using the gain formula in Fig. 1b with the required gain, determine the value of the feedback resistor `R2` and set it up in the schematic.

For the report: Export an image of your schematic for your report. [You can use the *LTspice* bitmap export tool found under `Tools` in the main menu bar. The tool exports an image of the active window. To make a window active, click anywhere in the window.]
Copy and paste the complete netlist [`View→SPICE Netlist`] into your report. This serves as a textual summary of your circuit (and in later parts of the assignment, your simulation), and thus helps with assigning part marks to incorrect submissions.

B. Nonlinear Circuit Operation – Part I

Set $V_{CC} = 100$ V and $V_{EE} = 0$ V. To do this, place the mouse over the symbol `V` next to the desired DC voltage source and right-click. A window pops up where you can input the value; i.e., `100` for V_{CC} and `0` for V_{EE}. Run the simulation and observe V_o as a function of time. You can set up the simulation through `Simulate -> Edit Simulation Cmd`. Fig. 4 shows an example setup suitable for this task.

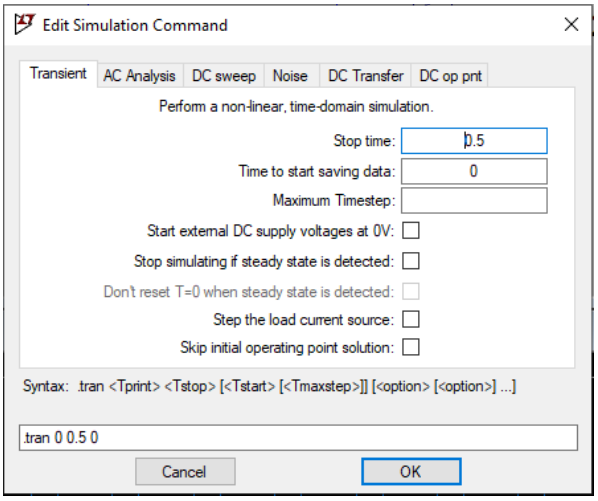


Fig. 4. Example simulation setup suitable for Exercise #1.

For the report: Export the plot of V_o as a function of time for your report. [To generate a plot of the voltage on a wire (net), point the mouse to the net until you see a probe symbol and click. If there are two or more curves already plotted and you want only one of them to remain, simply double-click on the net whose voltage you want to display by itself.]
Copy and paste the complete netlist [`View→SPICE Netlist`] into your report.
Answer the following question:

Q-E1B: Explain the behavior of V_o. Which half-periods of V_S (the positive or the negative) are amplified and transferred to the output and which are cut out?

C. Nonlinear Circuit Operation – Part II

Set $V_{CC} = 100$ V and $V_{EE} = 20$ V. Run the simulation and observe V_o as a function of time.

For the report: Export the plot of V_o as a function of time for your report.
Copy and paste the complete netlist [`View→SPICE Netlist`] into your report.
Answer the following question.
Q-E1C: Explain the behavior of V_o. Which values within the V_S waveform are amplified and transferred to the output and which are cut out?

D. Linear Circuit Operation

Set $V_{CC} = 100$ V and $V_{EE} = 100$ V. Run the simulation and plot both V_S and V_o as functions of time on the same plot.

For the report: Export the plot of V_S and V_o as functions of time for your report. [To change the colors of the plotted waveforms or the background of the plot, select `Tools → Color Preferences`. In the `Color Palette Editor` select the tab `WaveForm`.]
Copy and paste the complete netlist [`View→SPICE Netlist`] into your report.

E. Limit on Output Current

The DC supply voltages are still set as $V_{CC} = 100$ V and $V_{EE} = 100$ V. Inspect the op-amp parameters of the default component `UniversalOpamp2`. [Hover the mouse over the op-amp until you see the pointing hand, then right-click.] These are shown in Fig. 5. Therein, `Avol` is A_o, `Ilimit` is the maximum output current $I_{o,\max}$ that the device can supply, and `Rin` is the device input resistance R_i. We see that this op-amp model is not quite ideal since $A_o = 10^6$ is not infinite and neither is $R_i = 5 \cdot 10^8$ Ω. Note also that `Rail` has a value of 0. This means that this is a *rail-to-rail op-amp*, meaning that V_o can vary all the way from the negative voltage supply V_{EE} to the positive one V_{CC}.

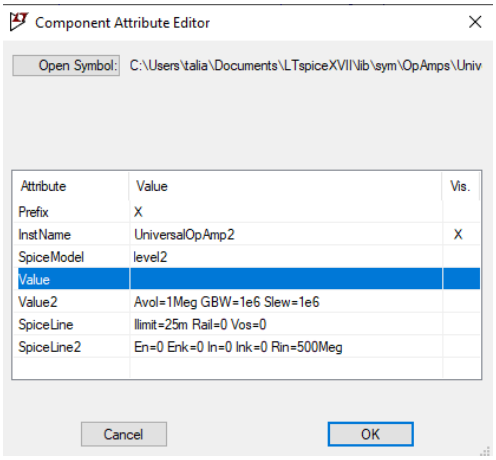


Fig. 5. Op-amp parameters of the default component `UniversalOpamp2`.

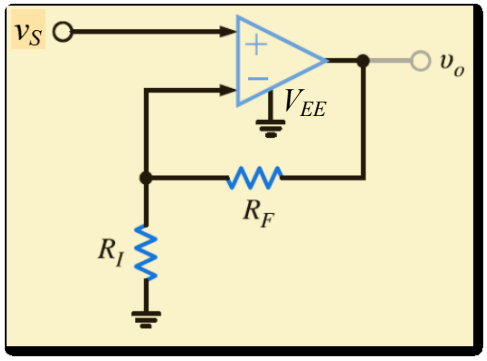
Here, we are concerned with $I_{o,\max} = 25$ mA. So far, the circuit output has been left open, i.e., $I_o = 0$ A. Now we will load it with a resistor R_L. Knowing the maximum voltage value that your circuit can output in a linear regime ($V_{o,\max} = |g| V_{S,\max}$) and the maximum current allowed, calculate the minimum load that you can employ, $R_{L,\min}$. Perform two simulations: with $R_L = 2R_{L,\min}$ and with $R_L = 0.5R_{L,\min}$. Observe the time waveforms of V_o and I_o (the current through R_L) in both cases.

For the report: Export the plot of V_S, V_o and I_o (all three waveforms in one plot) as functions of time in the case of: (a) $R_L = 2R_{L,min}$, and (b) $R_L = 0.5R_{L,min}$. [When plotting voltages and currents on the same plot, the voltage scale is on the left whereas the current one is on the right, or *vice versa*.]
Copy and paste the complete netlist [`View→SPICE Netlist`] into your report.
Answer the following questions:
Q-E1E1: What is the value of $R_{L,min}$?
Q-E1E2: What is the observed maximum value of V_o with $R_L = 2R_{L,min}$ and what is it with $R_L = 0.5R_{L,min}$? Is there a difference? Explain why you observe these values referring also to the observed maximum values of I_o in both cases.

Upload the final version of your *LTspice* schematic file `*.asc` along with the PDF of your Exercise #1 Report to the A2L Dropbox.

EXERCISE #2: *NONINVERTING OP-AMP CIRCUIT*

The noninverting op-amp circuit is shown in Fig. 6 along with its voltage gain assuming an ideal op-amp. Note that the implementation shown in Fig. 6 ($V_{EE} = 0$) is specifically designed to operate with positive signals, where $v_S \geq 0$ and, therefore $v_o \geq 0$ (this is a non-inverting amplifier circuit). The circuit, however, can work also with $v_S < 0$, in which case the negative voltage input results in a negative voltage output. In such regime, the negative voltage supply V_{EE} cannot be zero (as in Fig. 6). With a rail-to-rail op-amp, V_{EE} sets the negative-value limit of v_o.



(a)

$$\frac{v_o}{v_S} = 1 + \frac{R_F}{R_I}$$

(b)

Fig. 6. (a) The noninverting op-amp circuit. (b) Its voltage gain assuming an ideal op-amp.

Perform the following tasks.

A. Create the *LTspice* Schematic

Set the value of the resistor R_F to be equal to the sum of the last two digits of your student number in kΩ. For example, if the last two digits of your student ID are `63`, then set $R_I = 9$ kΩ.

Your circuit must exhibit a voltage-gain value of 10. Using the gain formula in Fig. 6b with the required gain, determine the value of the feedback resistor R_F. Build the schematic in *LTspice*, where the positive and negative supply voltages are set in exactly the same manner as in Exercise #1. You will assign their DC values later. The input-signal voltage V_S, too, is the same as in Exercise #1, i.e., it is a sine waveform with magnitude of 5 V and frequency of 60 Hz. The simulation setup is identical to that in Exercise #1 (see Fig. 4).

For the report: Export an image of your schematic for your report. Provide the complete netlist.

B. Nonlinear Operation of the Noninverting Op-amp Circuit

Set the DC supply voltages as follows: $V_{CC} = 100$ V and $V_{EE} = 0$ V. Simulate your circuit and observe the V_S and V_o waveforms on a common plot.

For the report: Export the plot of V_S and V_o for your report. Provide the complete netlist. Answer the following questions:
Q-E2B1: Has your circuit achieved the desired gain of 10?
Q-E2B2: Is it operating in a nonlinear regime? Justify your answer.

C. Linear Operation of the Noninverting Op-amp Circuit

Set the DC supply voltages as follows: $V_{CC} = 100$ V and $V_{EE} = 100$ V (negative DC bias). Simulate your circuit and observe the V_S and V_o waveforms on a common plot.

For the report: Export the plot of V_S and V_o for your report. Provide the complete netlist. Answer the following questions:
Q-E2C1: Has your circuit achieved the desired gain of 10?
Q-E2C2: Is it operating in a linear regime? Justify your answer.

D. Gain Error of the Noninverting Op-amp Circuit

Change the V_S to a DC source with value $V_S = 1$ V. Simulate and observe the plot of V_o. Export the plot for your report.

In Lecture 2, we found that a finite value of A_o leads to a voltage gain, which is smaller than the case when $A_o \to \infty$. To observe the effect, change the default value of A_o (10^6) to 100. [Right-click on the op-amp component to open the `Component Attribute Editor` for `UniversalOpamp2`; see Fig. 5. Double-click in the `Value` field for `Value2` and then click next to `Avol` to change its value to 100.] Simulate again and observe the plot of V_o. Export the plot for your report.

For the report:
1) Export the plot of V_o for the case when $A_o = 10^6$. Provide the complete netlist.
2) Export the plot of V_o for the case when $A_o = 100$. Provide the complete netlist.
Q-E2D1: What is the circuit gain in the case when $A_o = 100$?
Q-E2D2: What is the gain error in percentage compared to the ideal gain of 10?

Upload the final version of your *LTspice* schematic file `*.asc` along with the PDF of your Exercise #2 Report to the A2L Dropbox.