ElecEng 2CF3
ASSIGNMENT 2
Op-Amp Logic Gates

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Instructions and Objective

- Complete all four exercises.
- Submit one LTspice (`*.asc`) file per exercise. Name them suitably. Failure to submit the files in the correct file format will be penalized.
- Submit one report as a PDF (`*.pdf`) for all four exercises with appropriately labeled sections. Follow the Report Requirements for each exercise. You may use these requirements as a checklist. If you cannot complete a requirement, it is best to state this in your report explicitly. Failure to submit the report in the correct file format will be penalized.
- Submit to the respective Dropbox on Avenue to Learn before the deadline.
- The report must include a suitable title, your full name as it appears on Avenue to Learn, your student ID number and your MacID login name at the top of the first page.
- There are numerous ways to design circuits that meet the criteria for each section; however, the solutions for Exercises 1 and 2 should be similar and those for Exercises 3 and 4 should be similar. Consider solving the exercises in pairs.
- There is a requirement to include SPICE netlists in the report. Just copy-paste the netlist text from LTspice. Do not export or submit any netlist files.

Logic gates are used as building blocks in the design and implementation of digital circuitry for computers. A logic gate implements a Boolean function – a function that is performed on binary inputs and results in a binary output. These binary values can take on two states: logic low (0) and logic high (1).

In this assignment, you will use operational amplifiers (op-amps) in LTspice to implement the four basic logic gates in Figure 1. In your circuits, logic high (1) will be represented with 5 V, and logic low (0) will be represented with 0 V. Here, we only concern ourselves with the four gates in Figure 1: the (non-inverting) buffer, the NOT gate or inverting buffer[1], the (inclusive) OR gate and the AND gate. Generally speaking, there are others, but these four can all be made using a single op-amp.

Recall that an op-amp has two supply inputs with voltages $V_{CC} > V_{EE}$, a non-inverting input with voltage V_+, an inverting input with voltage V_- and an output with voltage V_{out} (Figure 2). If an ideal op-amp has no negative feedback loop, it functions as a comparator, i.e.,

$$V_{\text{out}} = \begin{cases} V_{EE}, & V_+ < V_- \\ V_{CC}, & V_+ > V_- \end{cases} \tag{1}$$

and thus its output is binary (either V_{CC} or V_{EE}). For this assignment, the behavior when $V_+ = V_-$ can be considered undefined; i.e., you will not be penalized for your circuit's behavior when $V_+ \approx V_-$ which will happen during certain transitions.

[1] We avoid the use of the term "inverter" as it can either refer to the inverting buffer/NOT gate studied in this assignment or the inverting amplifier studied in the previous assignment.

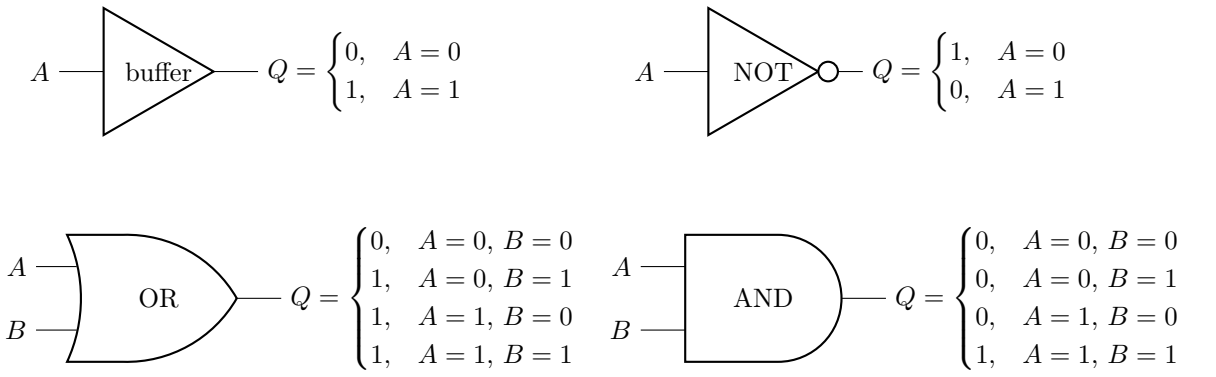

Figure 1: Schematic symbols and behavior of the buffer, NOT gate, OR gate and AND gate. The buffer's output Q is the same as its input A, the NOT gate's output Q is the opposite of its input A, the OR gate's output Q is low (0) only if both of its inputs A and B are low, and the AND gate's output Q is high (1) only if both of its inputs A and B are high.

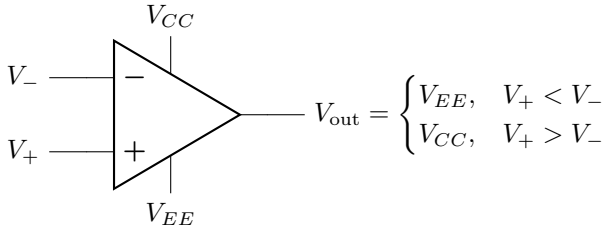

Figure 2: Ideal op-amp used as a comparator.

1 Simulate a Buffer in LTspice

In your circuit (see Figure 3), create a voltage source between ground (net `0`) and a net labeled `A`. Once you have placed the voltage source, right-click on it and click `Advanced` to access a menu to configure it as a square wave (`PULSE`) which varies between 0 V and 5 V with a 50% duty cycle. A suitable SPICE specification is given below, assuming the voltage source is named V_A or `VA`:

```
VA A 0 PULSE(0 5 0 0.001 0.001 0.25 0.5)
```

This is a pulse of period 0.5 s. Since its duty cycle must be 50%, the time during which its is ON (at 5 V) is 0.25 s. Its rise and fall times are both 1 ms. This source (net `A`) will be the input to the buffer circuit.

Next, add an op-amp (`UniversalOpamp2`) and label its output net `Q`. This will also be the output of the entire circuit.

Next, add a DC power supply such that the op-amp's supply voltages are $V_{CC} = 5\,\text{V}$ and $V_{EE} = 0\,\text{V}$ and thus $0\,\text{V} \leq V_{\text{out}} \leq 5\,\text{V}$. The supply voltages in your solution must not change (i.e., do not wire either to a varying voltage source).

Following the definition of the buffer from Figure 1, the circuit behavior should be

$$V_{\text{out}} = \begin{cases} 0\,\text{V}, & V_A = 0\,\text{V} \\ 5\,\text{V}, & V_A = 5\,\text{V}. \end{cases}$$

As this is an analog circuit, we consider its behavior for input values between 0 V and 5 V, too, so we modify the requirement as

$$V_{\text{out}} = \begin{cases} 0\,\text{V}, & V_A \lesssim 2.5\,\text{V} \\ 5\,\text{V}, & V_A \gtrsim 2.5\,\text{V}. \end{cases} \tag{2}$$

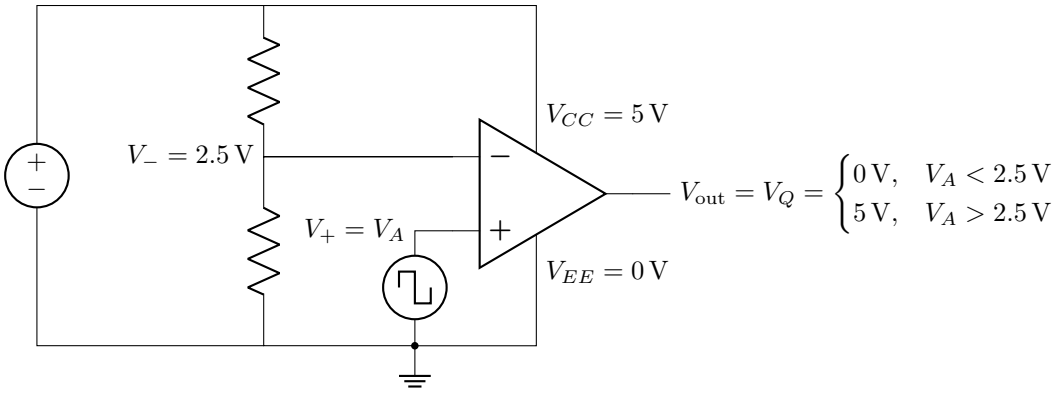

Figure 3: Template for the buffer circuit.

The exact behavior during transitions when $V_A \approx 2.5\,\text{V}$ is not important. Also, note that a unit-gain non-inverting amplifier that you studied in Lecture 1 cannot be used to perform the task specified by the requirement in Equation (2). The circuit in figure 3 is a digital logic buffer and it is different from the unit-gain amplifier.

Referring to Figure 3, your task to design a circuit that implements the non-inverting buffer described in Equation (2). The connections in the circuit are chosen by comparing Equation (2) to Equation (1); e.g., V_+ is wired to the square-wave source V_A and V_- is wired to the reference voltage of 2.5 V. You must choose appropriate values for the resistors.

Validate your design by carrying out transient analysis for at least one period of the square wave. Suitable simulation parameters which match the voltage source specification above are

```
.tran 0 1 0 0.01
```

After running the simulation, right-click in the existing plot pane and select `Add Plot Pane`. This will result in two vertically stacked panes. In the upper pane, add the trace `V(a)`, the voltage of the input net `A`. In the lower pane, add the trace `V(q)`, the voltage of the output net `Q`.

Report Requirements

1. Include the complete schematic (screenshot or image export).
2. Include the two waveforms resulting from the simulation, with the output voltage below the input voltage, as described above (screenshot or image export).
3. Include the complete netlist (`View`→`SPICE Netlist`).
4. Include the name of the LTspice (`*.asc`) file with the buffer circuit.
5. Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.
6. Explain how you derived the two resistors' values.
7. It was noted that a unit-gain amplifier is not suitable as a buffer because we would like the output to be either voltage high or low even if the input voltage is intermediate. Comment on why this behavior is desirable.

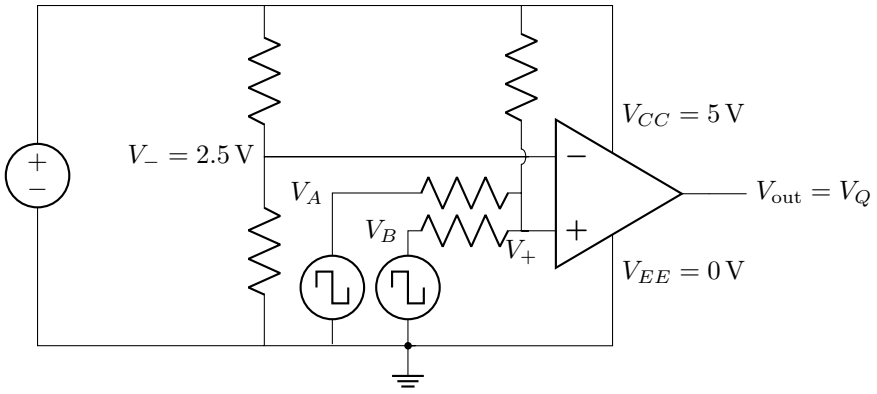

Figure 4: Template for the OR-gate circuit.

2 Simulate a NOT Gate in LTspice

To create a non-inverting buffer, we applied the input voltage (V_A) to the non-inverting input of the op-amp and applied a reference voltage (2.5 V) to the inverting input. For the inverting buffer (NOT gate), apply instead V_A to the inverting input and the reference voltage to the non-inverting input.

Derive an expression akin to Equation (2) that describes the comparator circuit for the NOT gate from Figure 1; i.e., complete the following output requirement:

$$V_{\mathrm{out}} = \begin{cases} ?, & V_A \lesssim 2.5\,\mathrm{V} \\ ?, & V_A \gtrsim 2.5\,\mathrm{V}. \end{cases}$$

Modify the buffer circuit to match this requirement and re-run the simulation.

Report Requirements

1. Include the complete schematic (screenshot or image export).
2. Include the two waveforms resulting from the simulation, with the output voltage below the input voltage, as described above (screenshot or image export).
3. Include the complete netlist (`View→SPICE Netlist`).
4. Include the name of the LTspice (`*.asc`) file with the NOT-gate circuit.
5. Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.
6. Explain why swapping the driving voltages of the inverting and non-inverting inputs turned the non-inverting buffer of Exercise 1 into an inverting buffer.
7. Include the output requirement for the NOT gate. It is not necessary to show its derivation.

3 Simulate an OR Gate in LTspice

In this exercise, you will simulate an OR gate by modifying the circuit from Exercise 1 to look like the circuit of Figure 4.

Two inputs are necessary for an OR gate, so add a second `PULSE` voltage source connected to a net labeled `B` with half the frequency of the first. The following are suitable:

```
VA A 0 PULSE(0 5 0 0.001 0.001 0.25 0.5)
VB B 0 PULSE(0 5 0 0.001 0.001 0.5 1)
```

To understand the circuit, note that we are using a comparator; therefore, we need a comparison expression that is equivalent to an OR gate. Consider that if the input voltages V_A and V_B are either 0 V or 5 V, then $V_A + V_B < 2.5\,\mathrm{V}$ only if $V_A = V_B = 0\,\mathrm{V}$, like an OR gate. However,

$$\max\left(V_A + V_B\right) = 10\,\mathrm{V} > V_{CC} = 5\,\mathrm{V},$$

so connecting the two sources in series is not a good solution. On the other hand, if $V_A + V_B < 2.5\,\mathrm{V}$, then $5\,\mathrm{V} + V_A + V_B < 7.5\,\mathrm{V}$. Therefore,

$$\frac{5\,\mathrm{V} + V_A + V_B}{3} \quad < \quad 2.5\,\mathrm{V}.$$

With $V_{CC} = 5\,\mathrm{V}$, this implies that

$$\bar{V} = \frac{V_{CC} + V_A + V_B}{3} < 2.5\,\mathrm{V}. \tag{3}$$

Both the mean $\bar{V}$ of V_{CC}, V_A and V_B on the left side and 2.5 V on the right side are within the interval $[V_{EE}, V_{CC}] = [0\,\mathrm{V}, 5\,\mathrm{V}]$. Show that if you set all three resistors leading to the non-inverting input in Figure 4 to the same value, its voltage will be $V_+ = \bar{V}$.

Also, write the mathematical expression that describes the circuit's behavior in terms of $\bar{V}$. It should look like

$$V_{\text{out}} = \begin{cases} ?, & \bar{V} \lesssim 2.5\,\mathrm{V} \\ ?, & \bar{V} \gtrsim 2.5\,\mathrm{V}. \end{cases}$$

Repeat the simulation again for at least one period of the input of the lowest frequency. Once again, suitable parameters are

```
.tran 0 1 0 0.01
```

This time, create three plot panes, one per trace. Plot `V(a)` and `V(b)` above `V(q)`.

Report Requirements

1. Include the complete schematic (screenshot or image export).
2. Include the three waveforms resulting from the simulation, with the output voltage below the input voltages, as described above (screenshot or image export).
3. Include the complete netlist (`View`→`SPICE Netlist`).
4. Include the name of the LTspice (`*.asc`) file with the OR-gate circuit.
5. Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.
6. Analyze the node at the non-inverting input of the op-amp to prove that

   $$V_+ = \bar{V} = \frac{V_{CC} + V_A + V_B}{3}$$

   if all three resistors branching from it have the same value R.
7. Include the output requirement for the OR gate.

4 Simulate an AND Gate in LTspice

In this exercise, you will implement the AND gate of Figure 1.

We are using a comparator. Therefore, we need a comparison expression that is equivalent to an AND gate. The AND gate's output must be high only if $V_A = V_B = 5\,\mathrm{V}$. In our analog circuit, this requirement is modified as

$$V_A + V_B > 7.5\,\mathrm{V}.$$

We cannot work with voltages greater than V_{CC}, but if $V_A + V_B > 7.5\,\mathrm{V}$, then

$$\bar{V} = \frac{0\,\mathrm{V} + V_A + V_B}{3} > 2.5\,\mathrm{V}.$$

Thus, we need to apply the mean of three voltages at the non-inverting input as in the case of an OR gate. However, now one of the voltages is 0 V which is equal to V_{EE}. Modify the circuit from Exercise 3 accordingly.

Report Requirements

1. Include the complete schematic (screenshot or image export).
2. Include the three waveforms resulting from the simulation, with the output voltage below the input voltages, as described above (screenshot or image export).
3. Include the complete netlist (`View→SPICE Netlist`).
4. Include the name of the LTspice (`*.asc`) file with the AND-gate circuit.
5. Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.
6. A NAND gate is an AND gate with its output inverted. Of course, it can be made by cascading an AND gate and a NOT gate, but suggest how it might instead be designed with a single op-amp.