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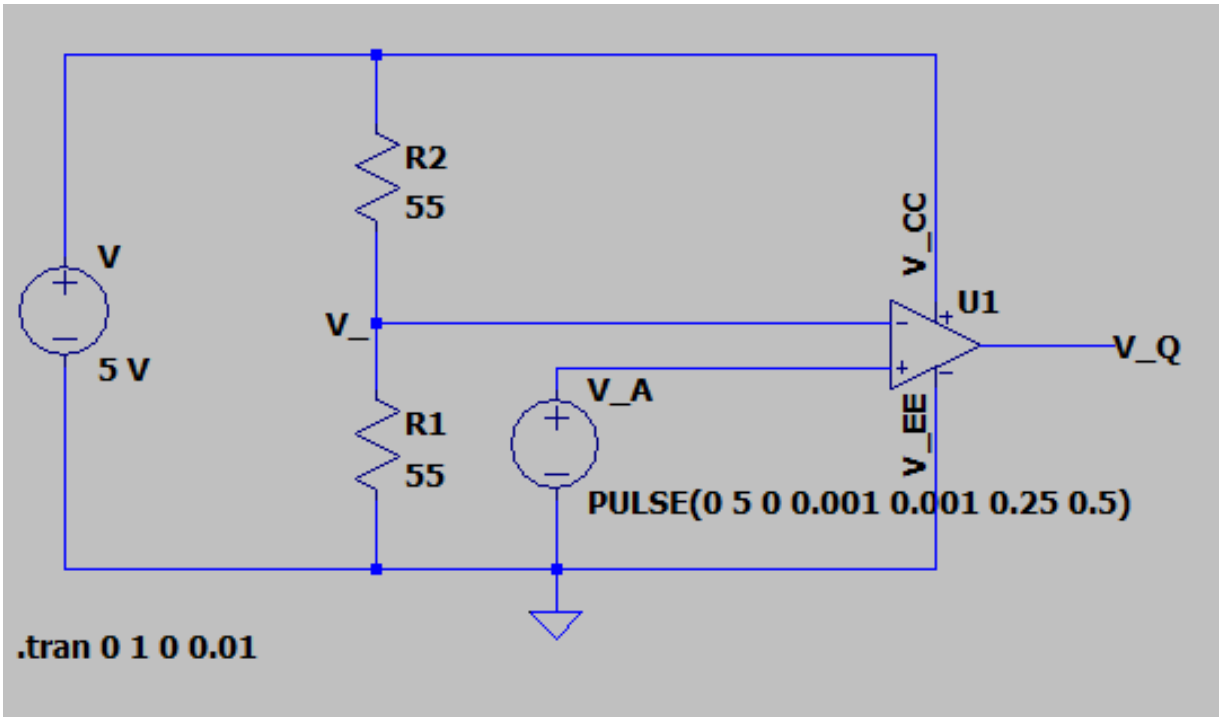
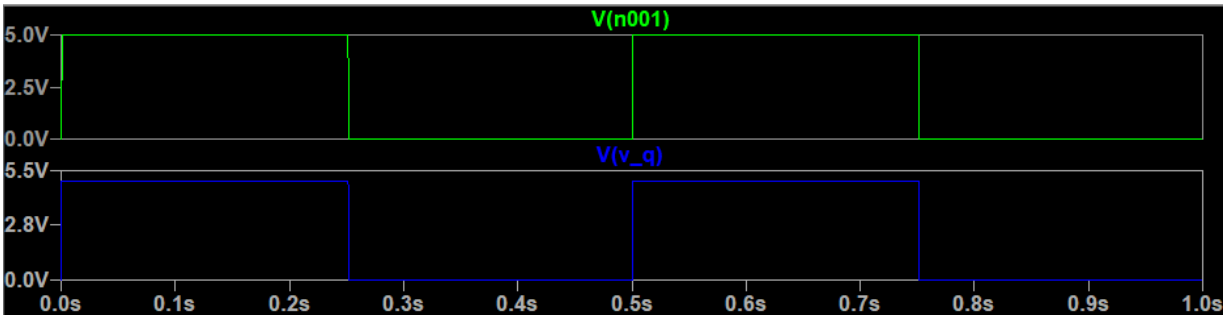
# Assignment 2: Op-amp Logic Gates

## Exercise 1

**Schematic:**




**Waveforms:**




**Netlist:**

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\eleceng 2cf3 assignements\assignment 2\assig2_q1.asc
R1 V_ 0 55
R2 V_CC V_ 55
V V_CC 0 5 V
XU1 N001 V_ V_CC 0 V_Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m
```

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```
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
V_A N001 0 PULSE(0 5 0 0.001 0.001 0.25 0.5)
.tran 0 1 0 0.01
.lib UniversalOpAmp2.lib
.backanno
.end
```

**Name of file:** assig2_q1.asc

**Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results**.

The simulation results do match the expected behavior because both V_A and V_Q produce the same result. They both drop and increase their voltages at the same time.

**Explain how you derived the two resistors' values.**

The 2 resistor values were determined using voltage division and it was discovered that it did not matter what the resistor values were, as long as they were of the same value. That is why I made my resistor values the last 2 numbers from my student ID.

**It was noted that a unit-gain amplifier is not suitable as a buffer because we would like the output to be either voltage high or low even if the input voltage is intermediate. Comment on why this behavior is desirable.**

When the input voltage was bigger than 2.5V, the unit gain amplifier was outputting a much higher level, and when the input was lower than 2.5V, the output was much lower. This was because logic gates can only have 0's and 1's as their output. Because of these on and off values provided, it is much easier to create more combinations in circuits to produce certain outputs we desire.

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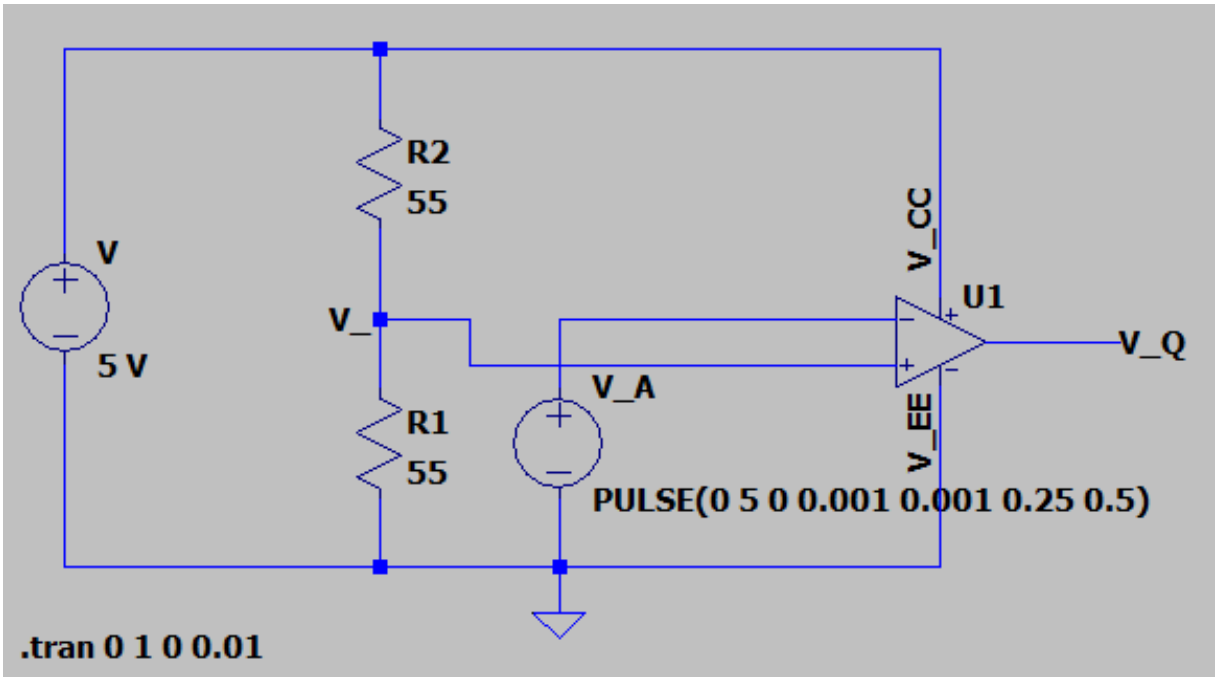
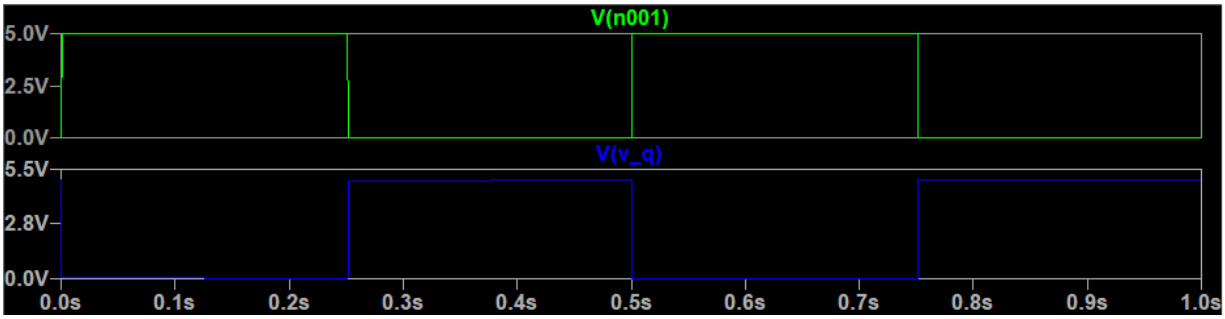
## Exercise 2

**Schematic:**




**Waveforms:**




**Netlist:**

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\eleceng 2cf3 assignements\assignment 2\assig2_q2.asc
R1 V_ 0 55
R2 V_CC V_ 55
V V_CC 0 5 V
XU1 V_ N001 V_CC 0 V_Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
V_A N001 0 PULSE(0 5 0 0.001 0.001 0.25 0.5)
.tran 0 1 0 0.01
.lib UniversalOpAmp2.lib
.backanno
```

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| |
|---|
| .end |
| **Name of file:** assig2_q2.asc |
| **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.**<br>The simulation results do match the expected behaviour because when V_A drops, V_Q increases, and vice-versa. This behaviour is the opposite from what is seen in exercise 1 because it functions as a NOT gate. |
| **Explain why swapping the driving voltages of the inverting and non-inverting inputs turned the non-inverting buffer of Exercise 1 into an inverting buffer.** |
| **Include the output requirement for the NOT gate. It is not necessary to show its derivation.**<br>For the NOT gate output, V_A would be 0V if it is bigger than 2.5V and would be 5V if it is less than 2.5V. |

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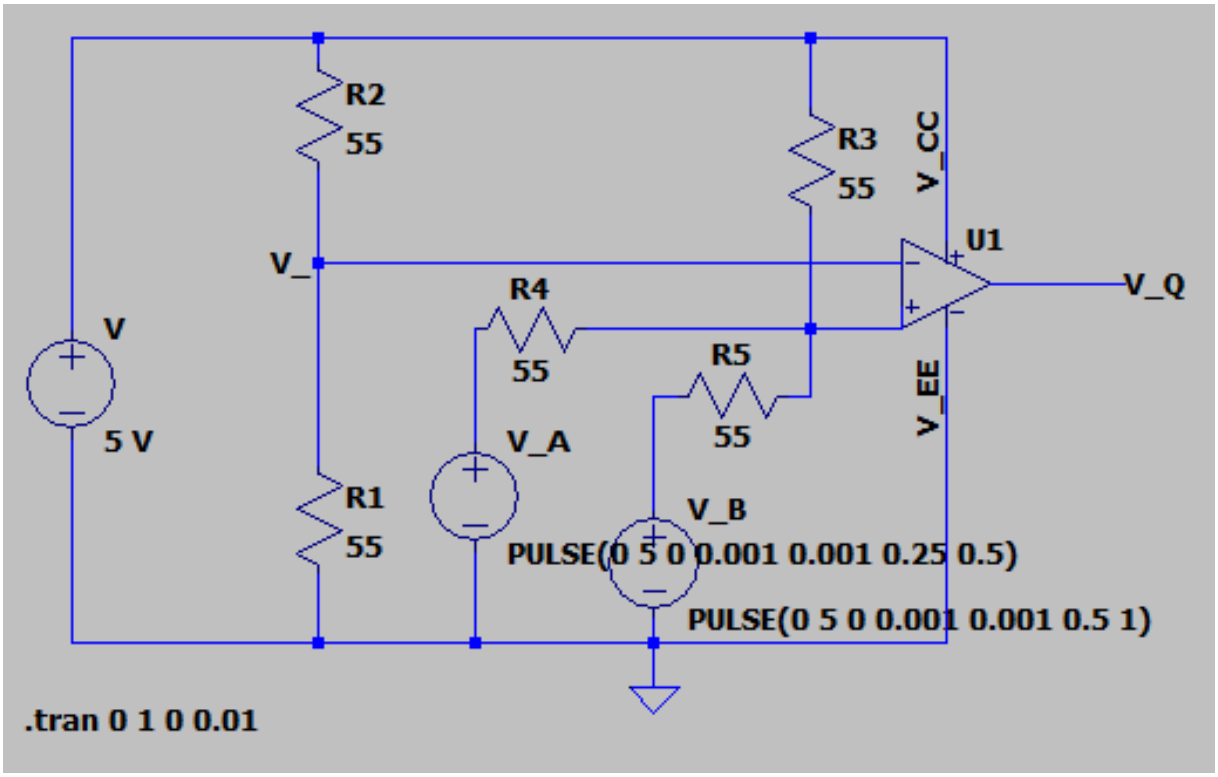
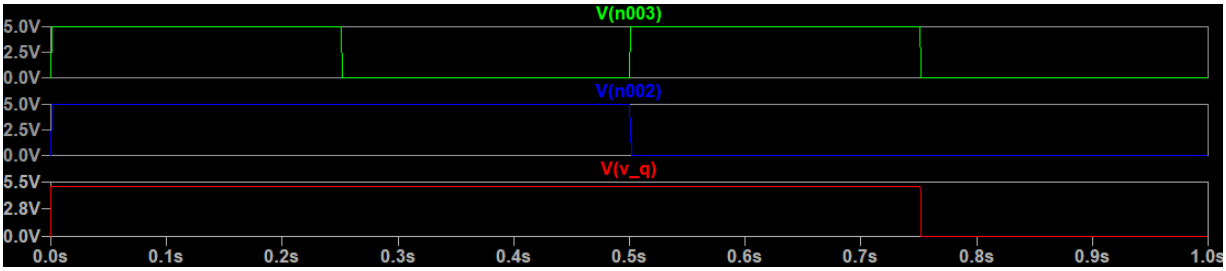
## Exercise 3

**Schematic:**




**Waveforms:**




**Netlist:**

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\eleceng 2cf3 assignements\assignment 2\assig2_q3.asc
R1 V_ 0 55
R2 V_CC V_ 55
V V_CC 0 5 V
XU1 N001 V_ V_CC 0 V_Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
V_B N002 0 PULSE(0 5 0 0.001 0.001 0.5 1)
R3 V_CC N001 55
R4 N001 N003 55
```

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```
R5 N001 N002 55
V_A N003 0 PULSE(0 5 0 0.001 0.001 0.25 0.5)
.tran 0 1 0 0.01
.lib UniversalOpAmp2.lib
.backanno
.end
```

**Name of file:** assig2_q3.asc

**Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.**

The simulation results match the expected behavior of an OR gate because if either V_A or V_B has a voltage, than the V_Q also has the same high voltage.

**Analyze the node at the non-inverting input of the op-amp to prove that $V_+ = V = \frac{V_{CC} + V_A + V_B}{3}$ if all three resistors branching from it have the same value R.**

Nodal analysis: $0 = \frac{V - V_A}{R} + \frac{V - V_A}{R} + \frac{V - 5}{R} = \frac{3V - V_B - V_A - 5}{R}$

Simplifies to: $V = \frac{-V_B - V_A - 5}{3}$ which is equal to $\frac{V_{CC} + V_A + V_B}{3}$ because V_CC = 5V.

**Include the output requirement for the OR gate.**

For the OR gate output, V_+ would be 0V if it is less than 2.5V and would be 5V if it is bigger than 2.5V.

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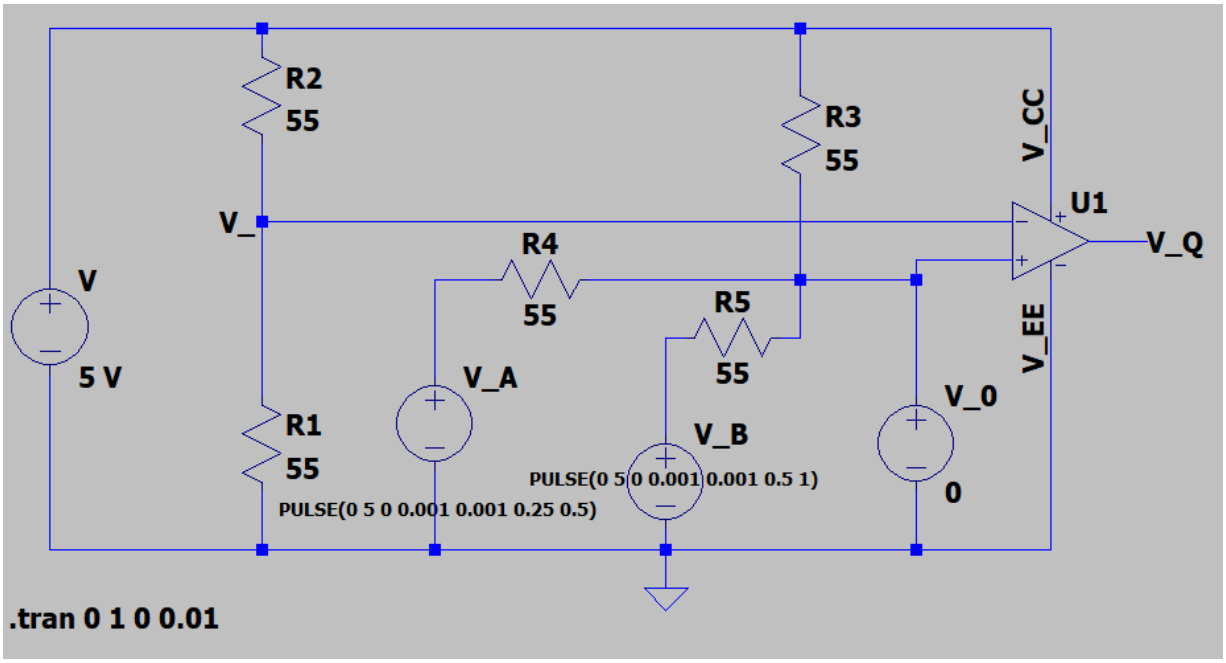
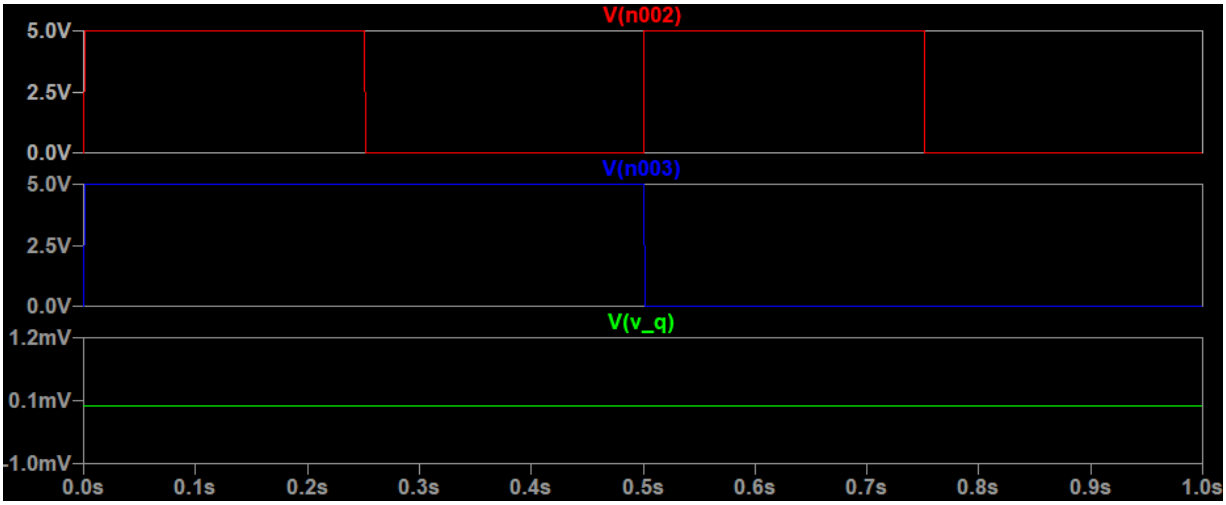
## Exercise 4

**Schematic:**




**Waveforms:**




**Netlist:**

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\eleceng 2cf3 assignements\assignment 2\assig2_q4.asc
R1 V_ 0 55
R2 V_CC V_ 55
V V_CC 0 5 V
XU1 N001 V_ V_CC 0 V_Q level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
```

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```
V_B N003 0 PULSE(0 5 0 0.001 0.001 0.5 1)
R3 V_CC N001 55
R4 N001 N002 55
R5 N001 N003 55
V_A N002 0 PULSE(0 5 0 0.001 0.001 0.25 0.5)
V_0 N001 0 0
.tran 0 1 0 0.01
.lib UniversalOpAmp2.lib
.backanno
.end
```

**Name of file:** assig2_q4.asc

**Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.**

The simulation results match the expected behavior of an AND gate because there is also a 0V input that is not being graphed. Since this input is off, it does not matter what the other inputs are, V_Q would be off.

**A NAND gate is an AND gate with its output inverted. Of course, it can be made by cascading an AND gate and a NOT gate, but suggest how it might instead be designed with a single op-amp.**

To design this using a simple op-amp instead of a NOT gate, simply switch the inverting and non-inverting inputs. This will make the outputs the opposite value of the inputs, as seen in exercises 1 and 2.