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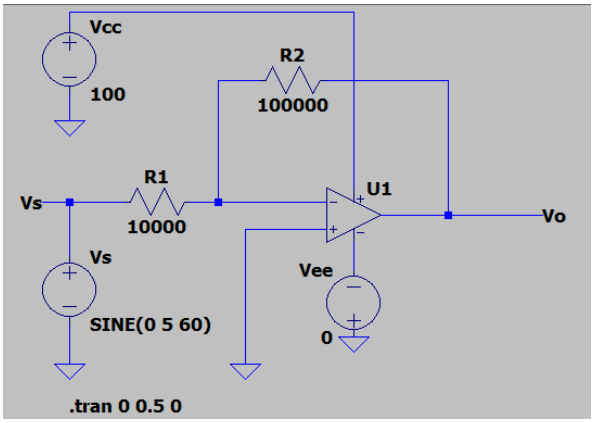
Assignment 1: Basic Circuits with Idealized Op-amp Model

Exercise 1

a.

Schematic:

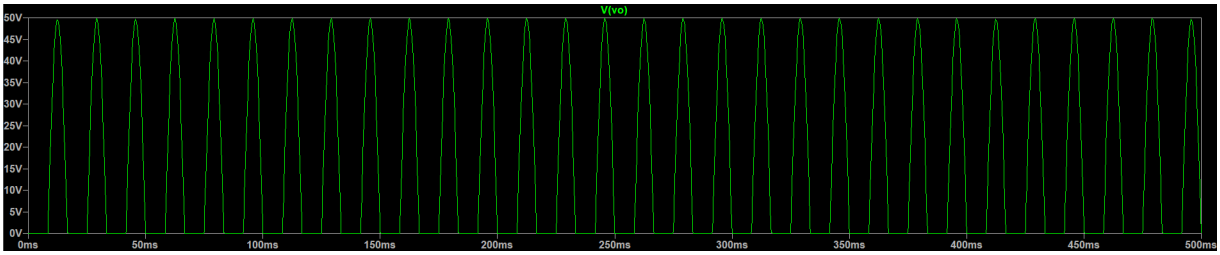


Netlist:

*C:\Users\gurle\OneDrive\Documents\LTspiceXVII\ElecEng 2CF3 assignments.asc
XU1 0 N002 N001 N003 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vs Vs 0 SINE(0 5 60)
Vee 0 N003 0
Vcc N001 0 100
R1 N002 Vs 10000
R2 Vo N002 100000
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end

b.

Plot:



Netlist:

*C:\Users\gurle\OneDrive\Documents\LTspiceXVII\ElecEng 2CF3 assignments.asc
XU1 0 N002 N001 N003 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vs Vs 0 SINE(0 5 60)
Vee 0 N003 0
Vcc N001 0 100
R1 N002 Vs 10000
R2 Vo N002 100000
.tran 0 0.5 0

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```
.lib UniversalOpAmp2.lib
.backanno
.end
```

Explain the behavior of V_0. Which half-periods of V_s (the positive or the negative) are amplified and transferred to the output and which are cut out?
V_0 has a maximum of about 50V and is constantly oscillating, but when it reaches 0V, it stays constant until the voltage is bigger than 0V again. The negative half-periods of V_s are amplified and transferred to the output and the positive half-periods of V_s are cut out because the inverting op-amp is being used.

c.

Plot:

Netlist:

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\ElecEng 2CF3 assignments.asc
XU1 0 N002 N001 N003 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vs Vs 0 SINE(0 5 60)
Vee 0 N003 20
Vcc N001 0 100
R1 N002 Vs 10000
R2 Vo N002 100000
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

Explain the behavior of V_0. Which values within the V_s waveform are amplified and transferred to the output and which are cut out?
V_0 has a maximum of about 50V and is constantly oscillating, but when it reaches -21V, it stays constant until the voltage is bigger than -21V again. Values above -21V are amplified and transferred out, while values below -21V are cut out.

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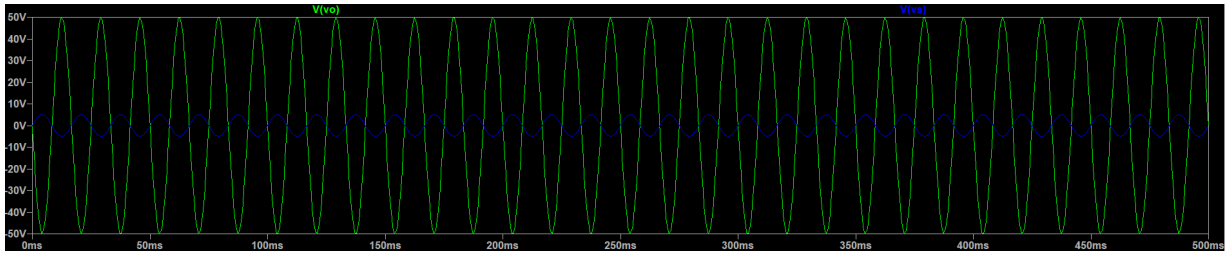
d.

Plot:

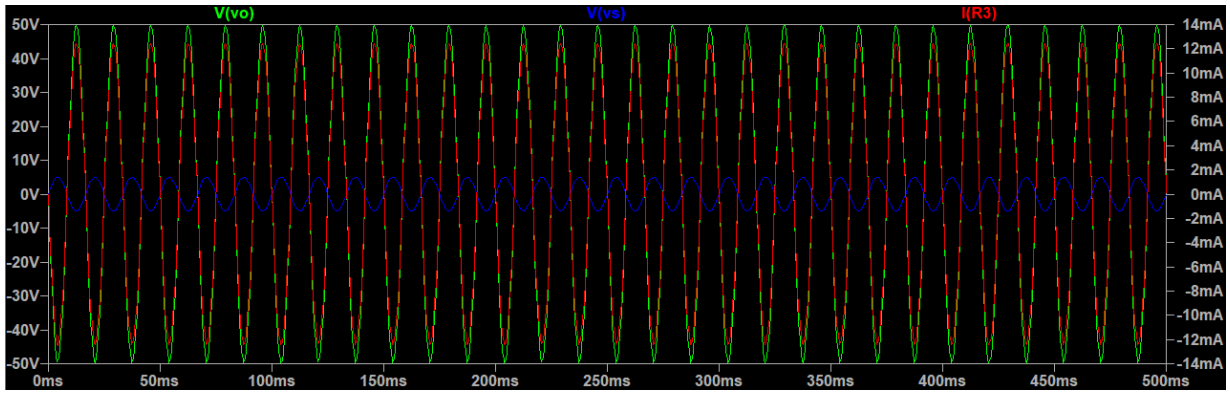


Netlist:

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\ElecEng 2CF3 assignments.asc
XU1 0 N002 N001 N003 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vs Vs 0 SINE(0 5 60)
Vee 0 N003 100
Vcc N001 0 100
R1 N002 Vs 10000
R2 Vo N002 100000
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

e.

Plot 1:



Plot 2:

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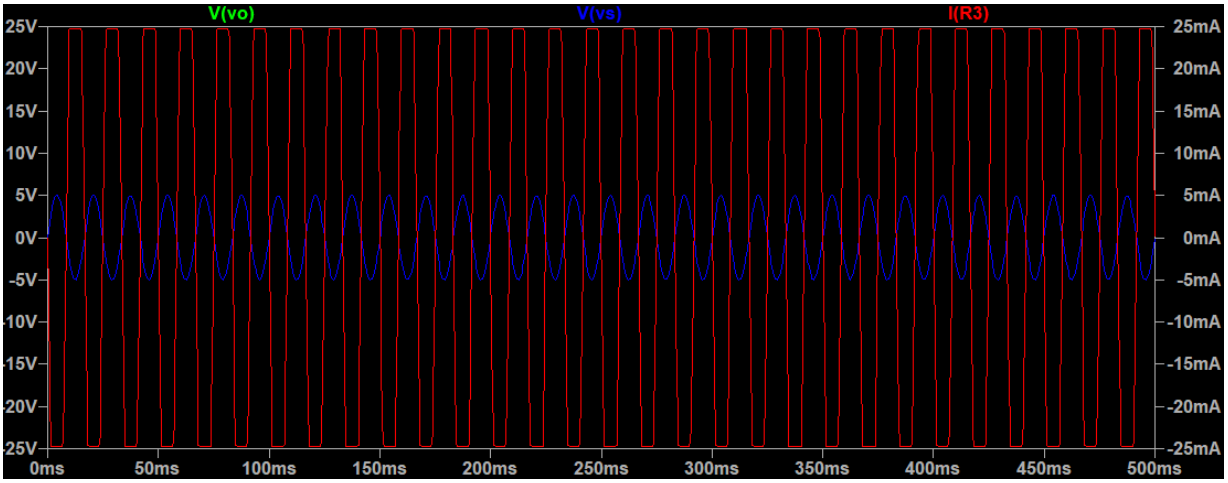

Netlist:

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\ElecEng 2CF3 assignments.asc
XU1 0 N002 N001 N003 Vo level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
Vs Vs 0 SINE(0 5 60)
Vee 0 N003 100
Vcc N001 0 100
R1 N002 Vs 10000
R2 Vo N002 100000
R3 Vo 0 1000
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

What is the value of R_L,min? $R_{L,min} = V_{0,max}/I_{0,max} = 2000\Omega$

What is the observed maximum value of V_0 with R_L = 2 R_L,min and what is it with R_L = 0.5R_L,min? Is there a difference? Explain why you observe these values referring also to the observed maximum values of I_0 in both cases.

The observed maximum value of V_0 with both R_Ls are both 100V.

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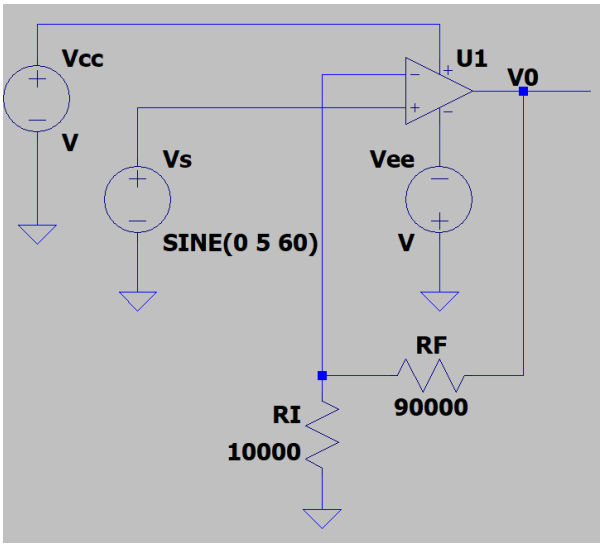
Exercise 2

a. *assuming R_I = sum of last 2 digits of student #*

Schematic:

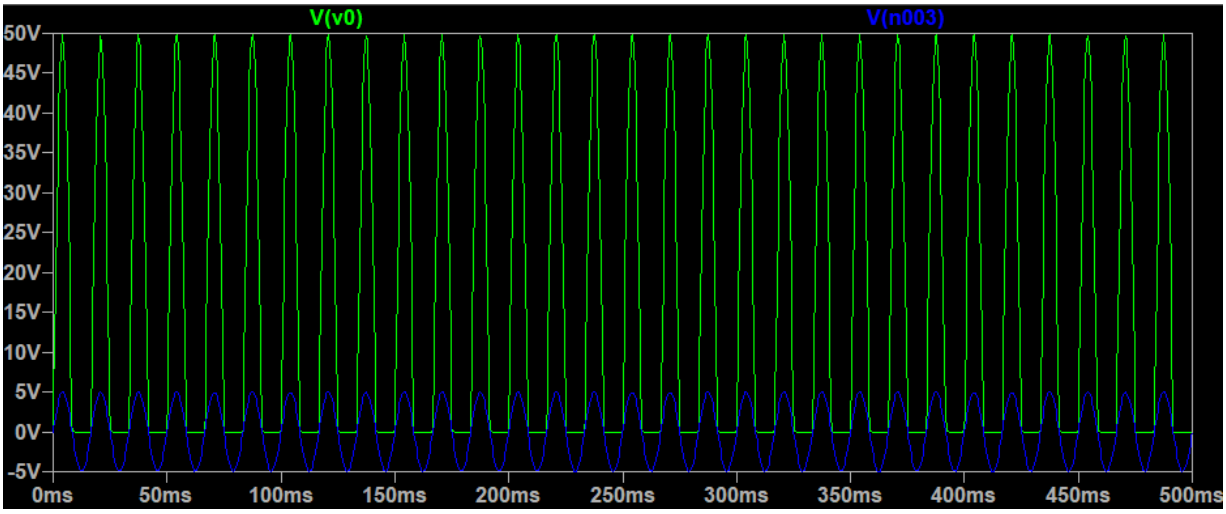


Netlist:

*C:\Users\gurle\OneDrive\Documents\LTspiceXVII\eleceng 2cf3 assignements\assig1_q2.asc
RI 0 N002 10000
RF N002 V0 90000
Vcc N001 0 V
Vee 0 N004 V
Vs N003 0 SINE(0 5 60)
XU1 N003 N002 N001 N004 V0 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.lib UniversalOpAmp2.lib
.backanno
.end

b.

Plot:



Netlist:

* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\eleceng 2cf3 assignements\assig1_q2.asc
RI 0 N002 10000
RF N002 V0 90000
Vcc N001 0 100
Vee 0 N004 0
Vs N003 0 SINE(0 5 60)

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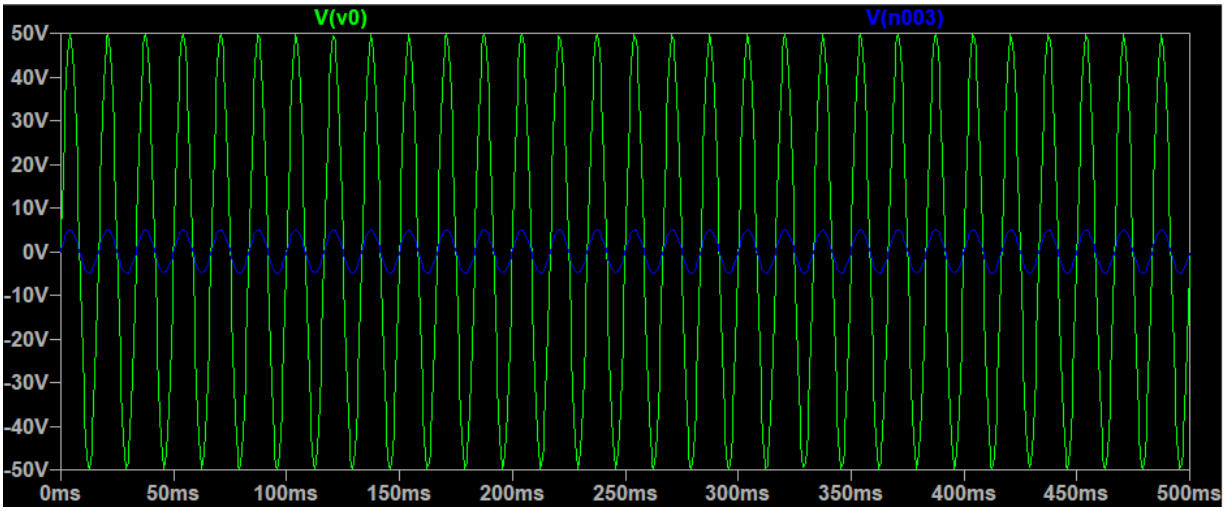
```
XU1 N003 N002 N001 N004 V0 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

Has your circuit achieved the desired gain of 10?
The desired gain has been achieved because the V_0 output has a peak 10x larger than the peak of V_s.

Is it operating in a non linear regime? Justify your answer.
It is not operating in a non-linear regime because the V_0 value is within the V_ee and V_cc values.

c.

Plot:



Netlist:

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\eleceng 2cf3 assignements\assig1_q2.asc
RI 0 N002 10000
RF N002 V0 90000
Vcc N001 0 100
Vee 0 N004 100
Vs N003 0 SINE(0 5 60)
XU1 N003 N002 N001 N004 V0 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
```

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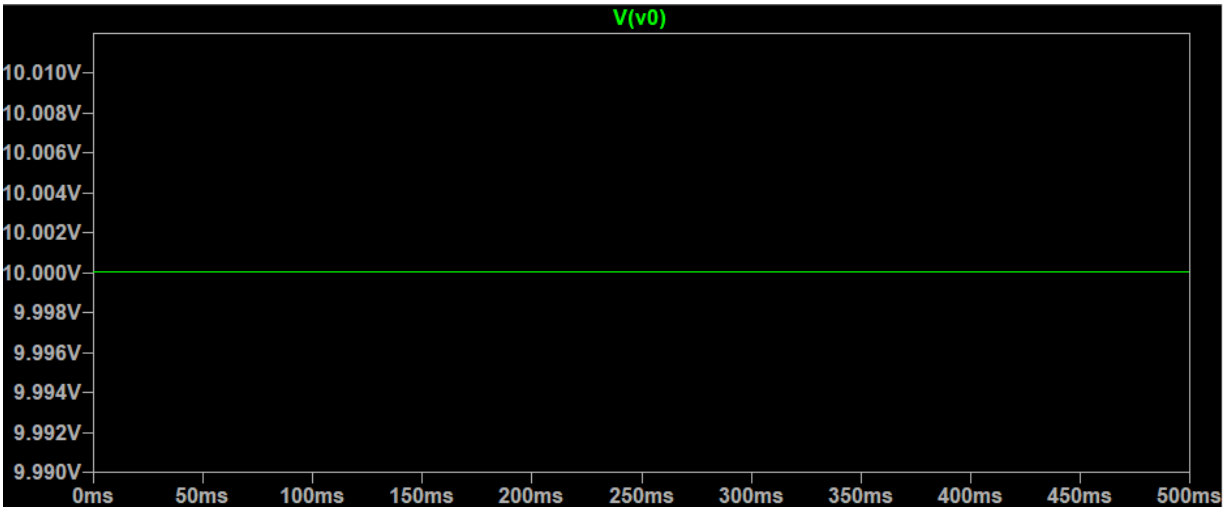
.end

Has your circuit achieved the desired gain of 10?
The desired gain has been achieved because the V_0 output has a peak 10x larger than the peak of V_s.

Is it operating in a linear regime? Justify your answer.
It is operating in a linear regime because the V_0 value is within the V_ee and V_cc values.

d.

Plot 1:



Netlist 1:

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\eleceng 2cf3 assignements\assig1_q2.asc
RI 0 N002 10000
RF N002 V0 90000
Vcc N001 0 100
Vee 0 N004 100
Vs N003 0 1
XU1 N003 N002 N001 N004 V0 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

Plot 2:

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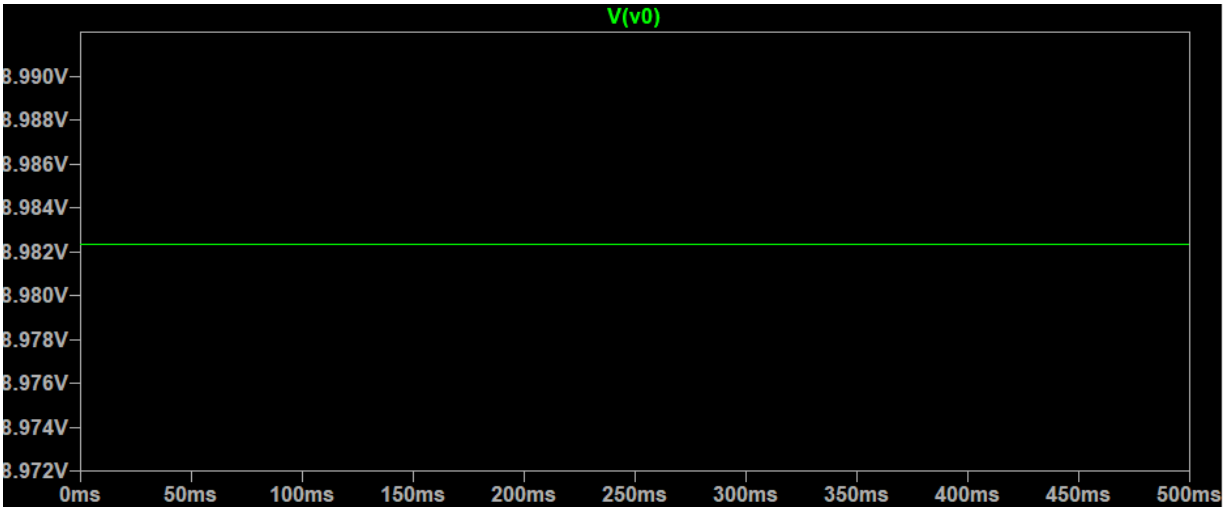

Netlist 2:

```
* C:\Users\gurle\OneDrive\Documents\LTspiceXVII\eleceng 2cf3 assignements\assig1_q2.asc
RI 0 N002 10000
RF N002 V0 90000
Vcc N001 0 100
Vee 0 N004 100
Vs N003 0 1
XU1 N003 N002 N001 N004 V0 level2 Avol=100 GBW=10Meg Slew=10Meg Ilimit=25m
Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.tran 0 0.5 0
.lib UniversalOpAmp2.lib
.backanno
.end
```

What is the circuit gain in the case when A_0 = 100? ~8.982V

What is the gain error in percentage compared to the ideal gain of 10?

$gain\ error\ =\ 100\%\ *\ (actual\ -\ ideal)/ideal\ =\ -\ 10.18\%$