
Design Project 4

ELECENG 2EI4

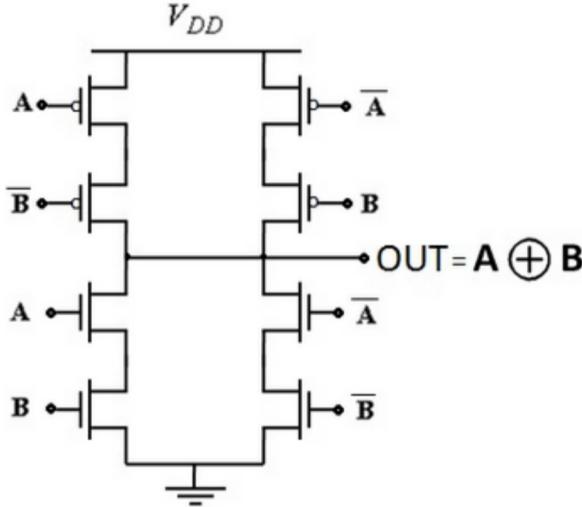
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Circuit Schematic



To create an XOR gate, we can use AND and OR gates. To do this, we can have A and B go into an AND gate and have A' and B go into another AND gate. These 2 inputs will then be put through an OR gate to create an output that matches the output of an XOR gate. The equation of this circuit would be AB' + A'B.

If we want to use negative gates like NAND or NOR, we can only use one to create an output equal to the XOR gate. For the NAND gate, the equation would be written as $(A(AB))(B(AB))$. For the NOR gate, the equation would be written as

$$\overline{(A + (\overline{A} + B))} + \overline{(B + (\overline{A} + B))} + \overline{(A + (\overline{A} + B))} + \overline{(B + (\overline{A} + B))} .$$

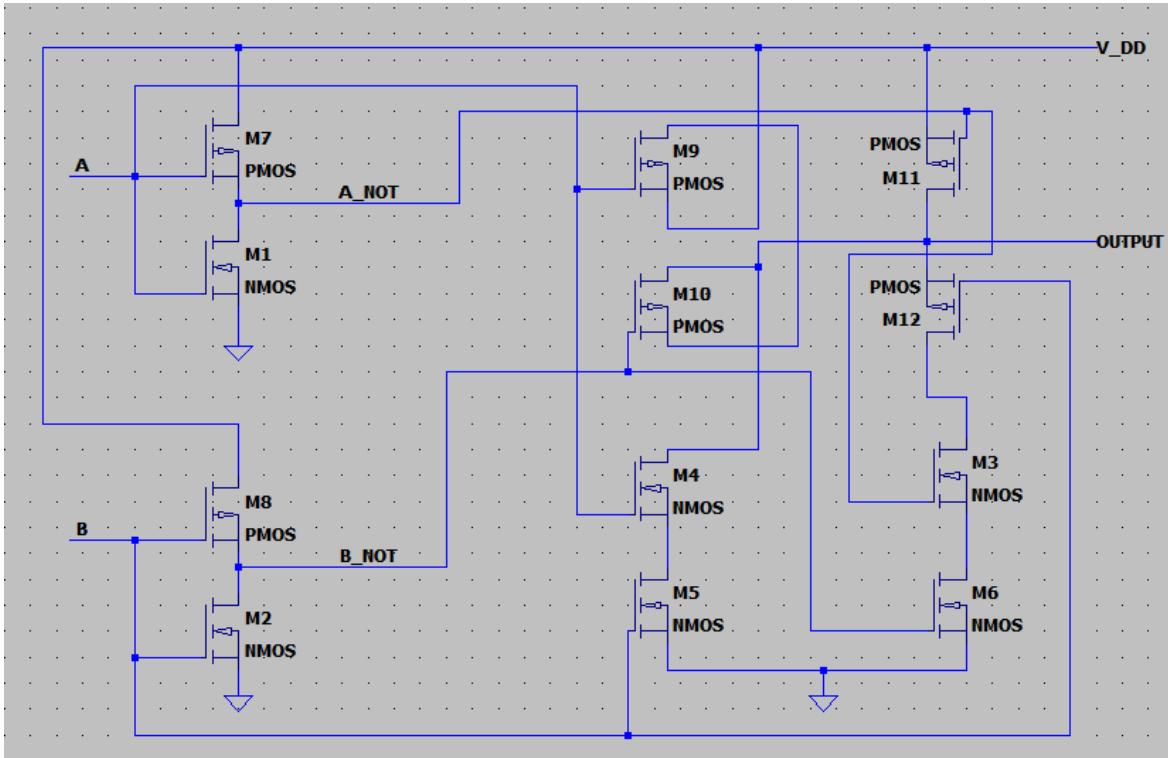


Figure 1: Schematic of XOR gate design

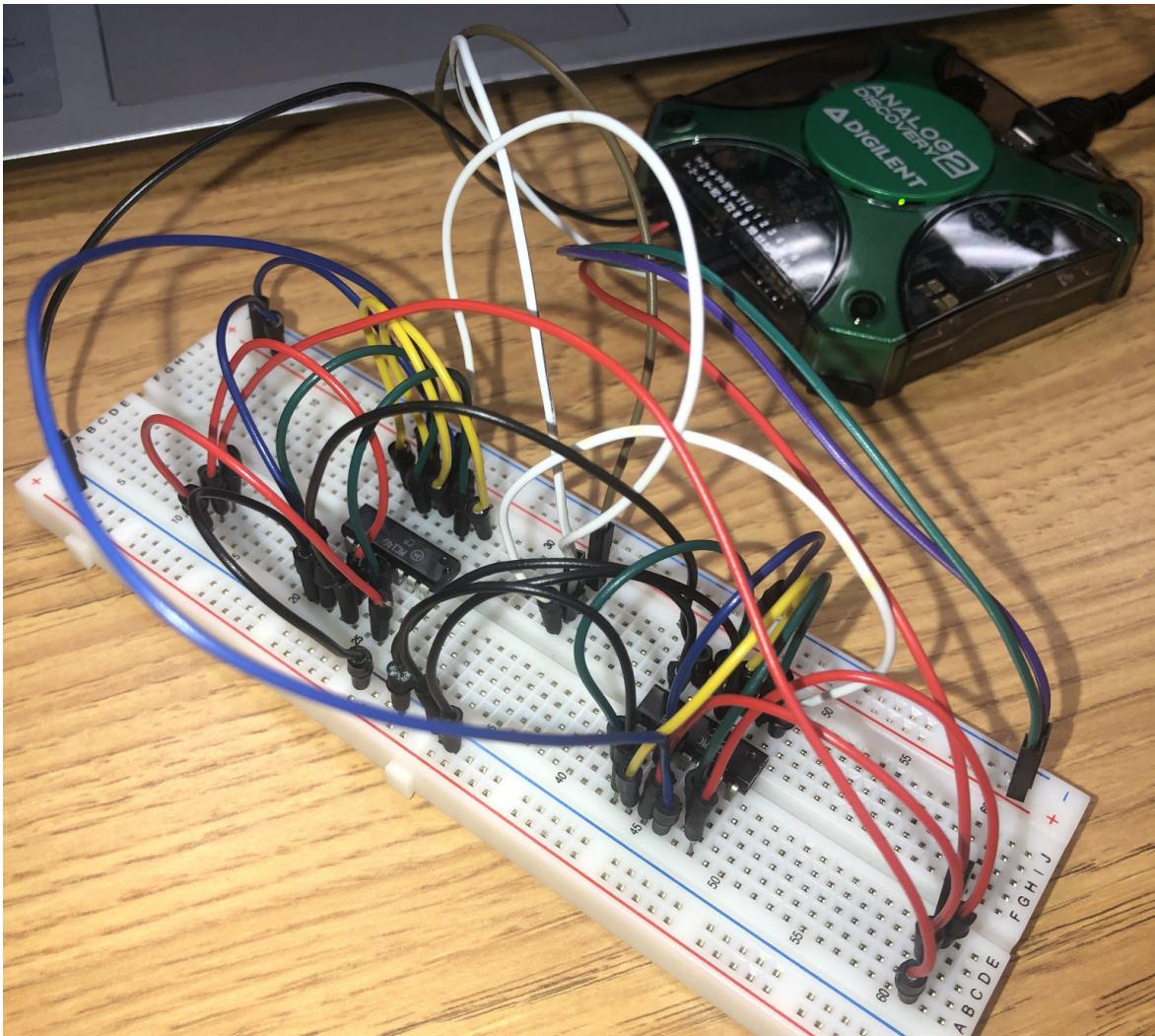


Figure 2: Circuit of XOR gate design

Ideal Sizing

The ideal ratio between the PMOS and the NMOS would be a 1 to 1 ratio, as there would be the same amount of PMOS and NMOS. This is because they act as switches and can switch between on and off so that we can create the truth table to the XOR gate using the multiple combinations of inputs. Overall, there will be 6 NMOS and 6 PMOS used. In the design, there will be four 2Ns and four 2Ps as well as one 2N and once 2P.

This circuit design can be implemented into the hardware design if the MC14007UB is used, as it gives us the option to utilize 12 transistors, half of which are NMOS and the other half PMOS.

Functional Testing

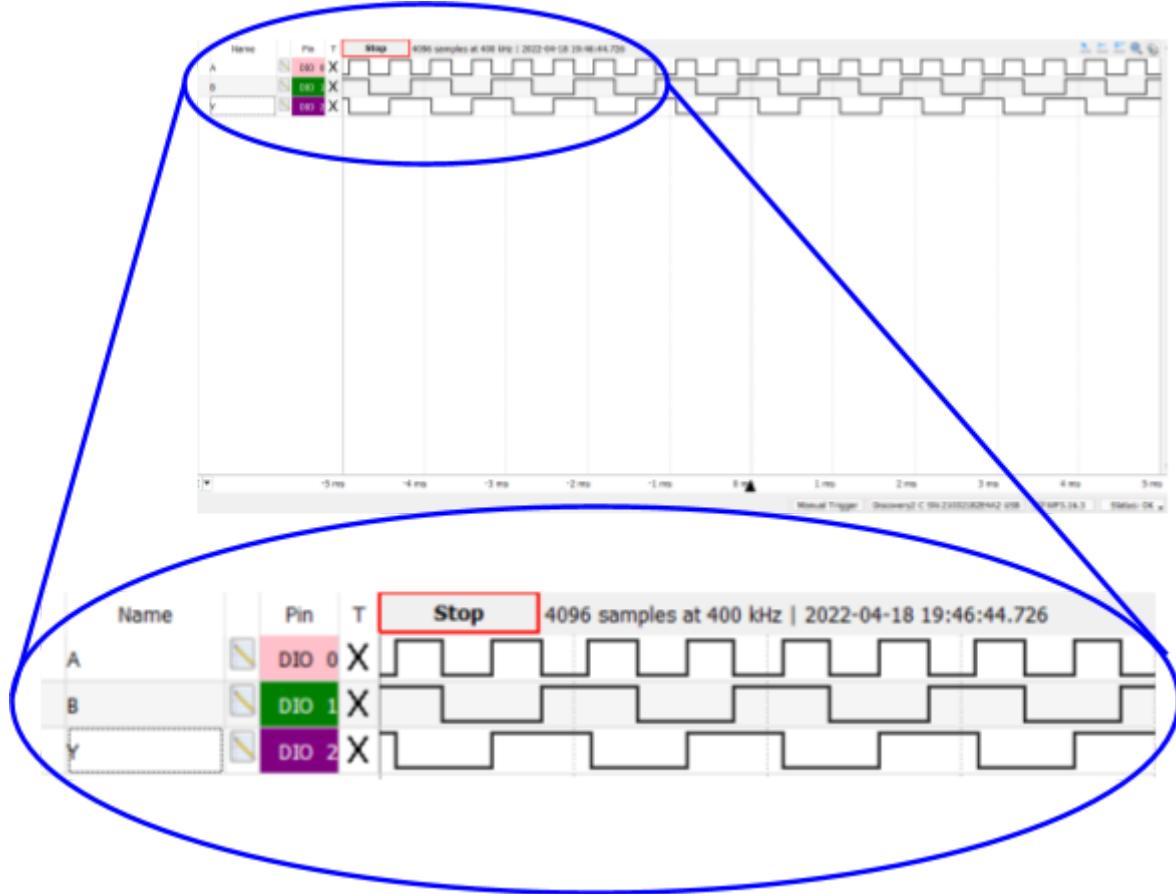


Figure 3: Logic result for XOR gate design from Waveforms

Static Level Testing

In our first test, we were to use a 5V constant for 1 wavegen, and a square wavegen for the second, which must also operate between 0V to 5V. From figure 4, it is visible that V_{IH} is equal to about 5V and V_{IL} is equal to about 0V. When the A and B switch their input voltages, the outputting oscilloscope remains the same.

For the second part of the testing, we were to use a similar wavegen to our first testing, except lower the amplitude until the logic failed. From figure 5, it is visible that V_{IH} is equal to about 3.19V and V_{IL} is equal to about 1.96V.

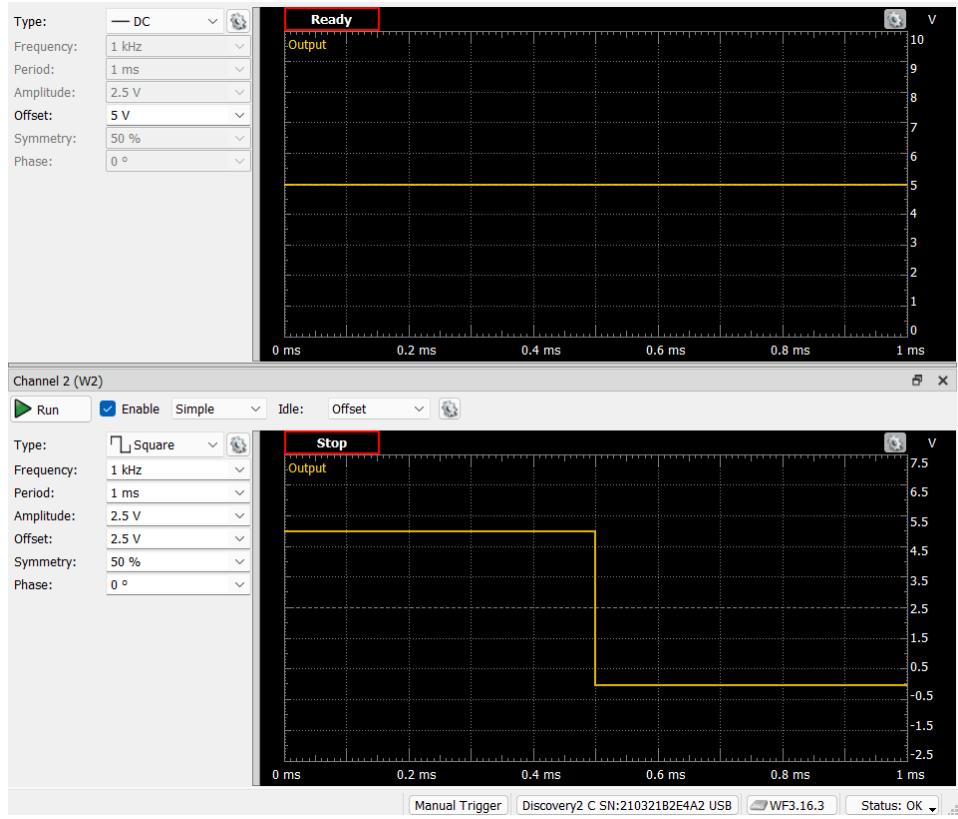


Figure 4: waveform inputs for the first testing

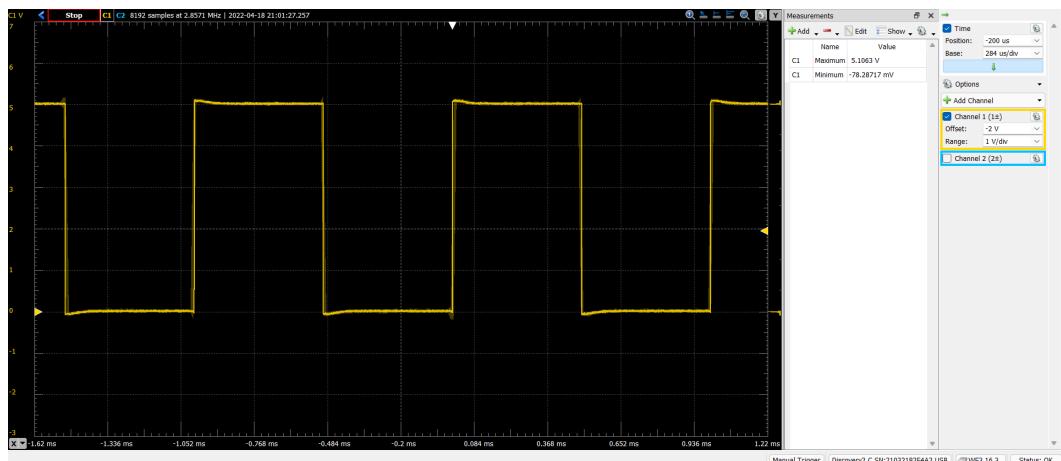


Figure 5: Oscilloscope graph output when one input is +5V and the other input is a square wave between 0 and +5V.

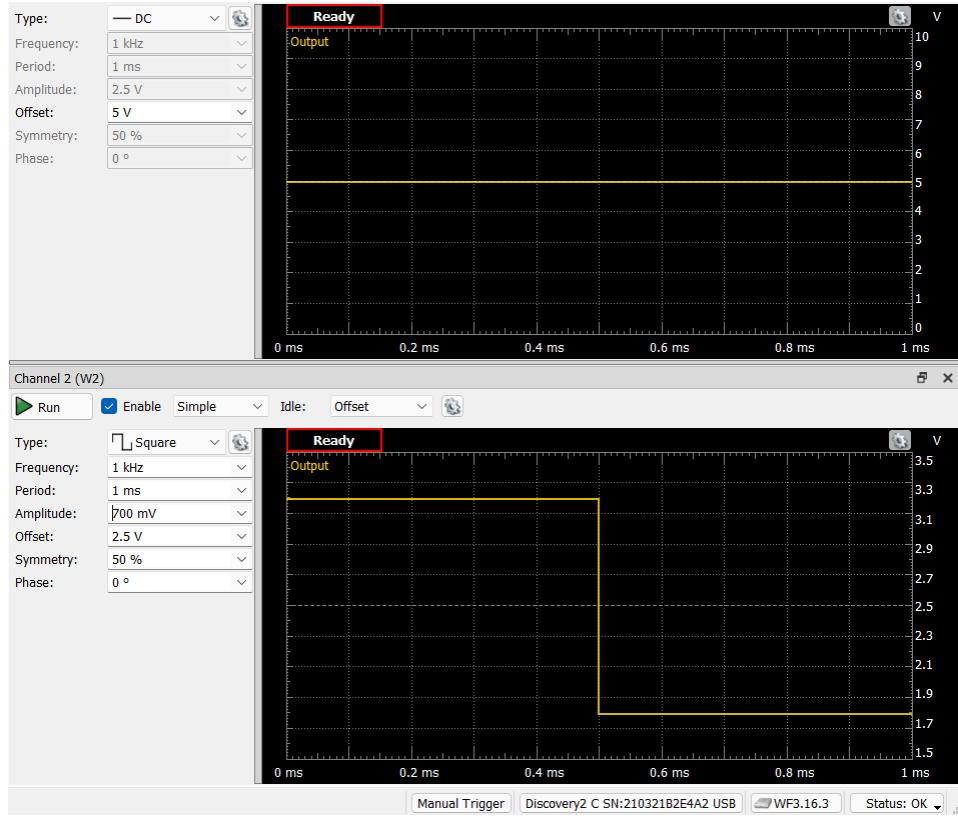


Figure 6: waveform inputs for the second testing

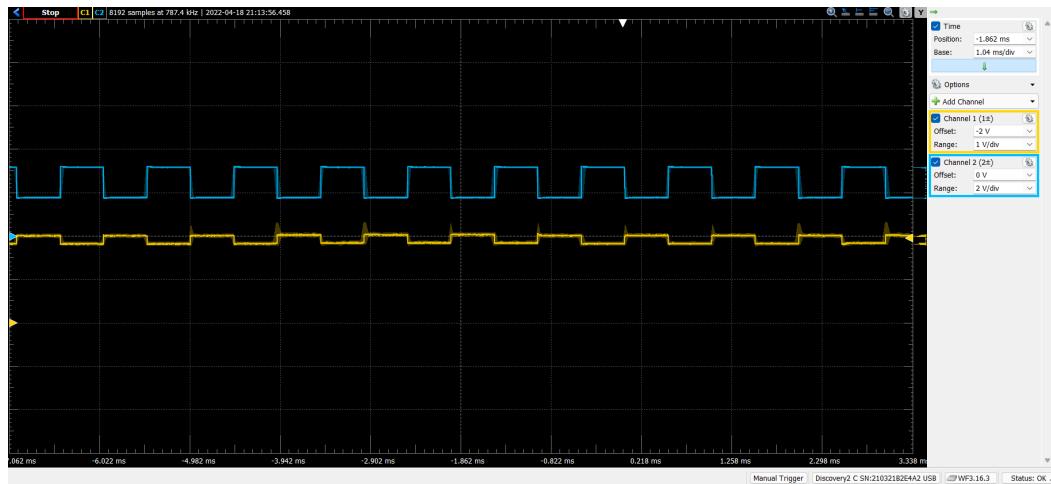


Figure 7: Oscilloscope graph output when one input is +5V and the other input is a square wave with an offset of 2.5V.

Timing

For the timing test, we were to use a 5V constant for 1 wavegen, and a square wavegen for the second, which must also operate between 0V to 5V. We must also connect a 100nF capacitor to the output. To calculate the rise and fall time, we can read the values from figure 8 and determine that the peak was about 4.8V. We were also able to determine our τ_{PLH} is equal to about 103us, τ_{PHL} is equal to about 110us, and τ_P is equal the summation of τ_{PHL} and τ_{PLH} divided by 2, which is equal to about 106.5us.

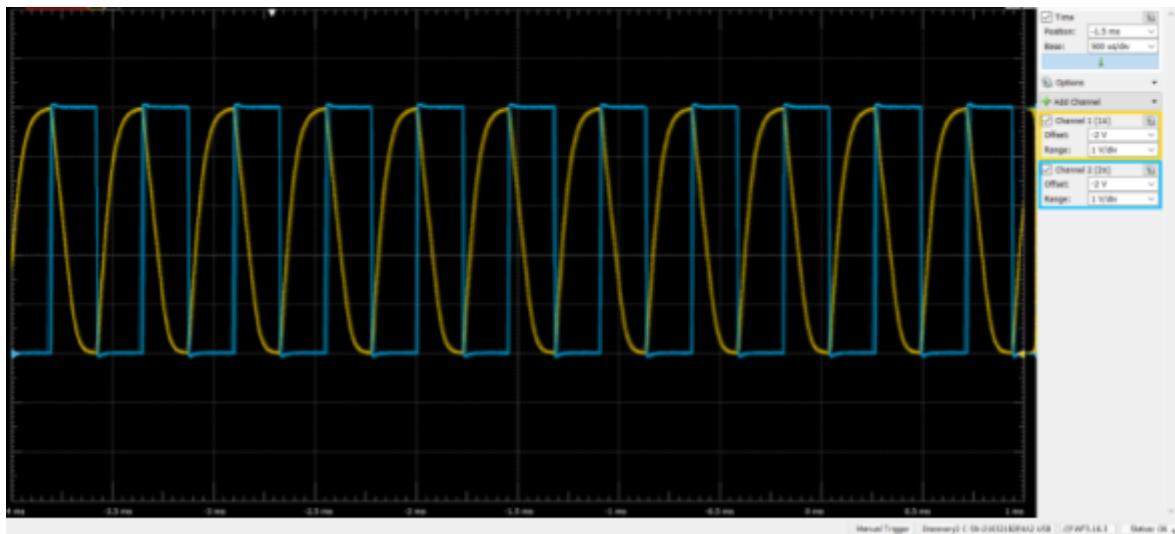


Figure 8: Oscilloscope for the timing test