ELECENG 2EI4: Electronic Devices and Circuits 1

Design Project 4

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Design Schematic

1. **Circuit Schematic**

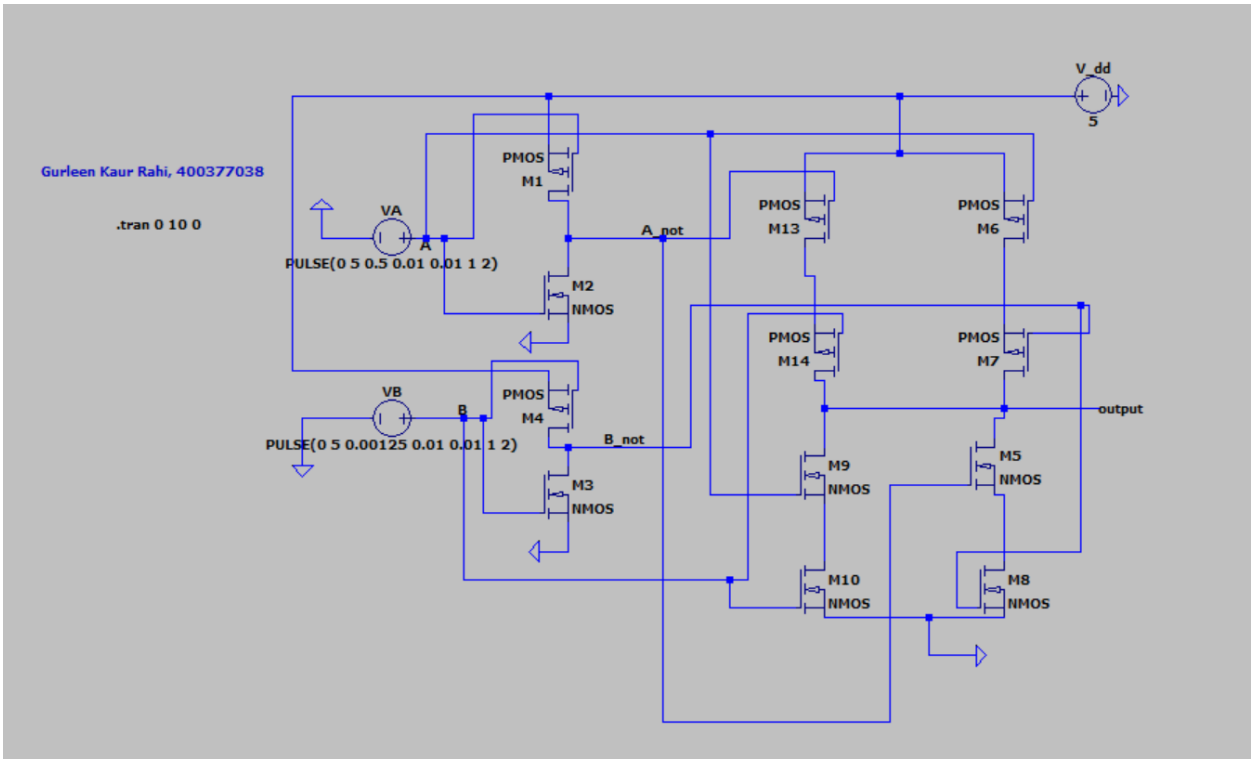

Figure 1: Circuit schematic of XOR gate

The figure above shows the schematic of the XOR gate. This schematic involves 12 mosfets in total, 6 of them are P-Mosfets and the other 6 are N-Mosfets. It also has two input voltage supplies, one V_dd of 5V, and a node for the output.

2. **Ideal Sizing. Explain the perfect ratio between PMOS and NMOS sizes for the design.**

For our 12-mosfet XOR gate design, the appropriate ratio between P-Mosfet and N-Mosfet sizes depends on a number of variables, including the process technology employed, the supply voltage, and the desired performance criteria.

The proportion of P-Mosfet to N-Mosfet transistor sizes is essential for attaining the best performance in mosfet designs, particularly in Xor gate design. Based on the difference between electron and hole density, this ratio is frequently selected. To be more precise, electron mobility is frequently higher than hole mobility, leading to faster switching speeds for N-Mosfet devices than P-Mosfet devices. The width of P-Mosfet transistors is often made to be wider than that of

N-Mosfet transistors in order to address this disparity. As a result, both types of transistors drive similar currents and have comparable rise and fall times. To ensure the performance of the circuit, **the ratio of 5:1 and of 5:2**. Another consideration is that because mosfets function like switches and can turn on or off, a truth table can be produced utilizing a variety of different input configurations. Six P-Mosfets and six N-Mosfets are used, balancing out the overall architecture.

3. **Explain whether you can implement the ideal sizing in your hardware design. If not, explain why not, and qualitatively explain the impact on circuit performance.**

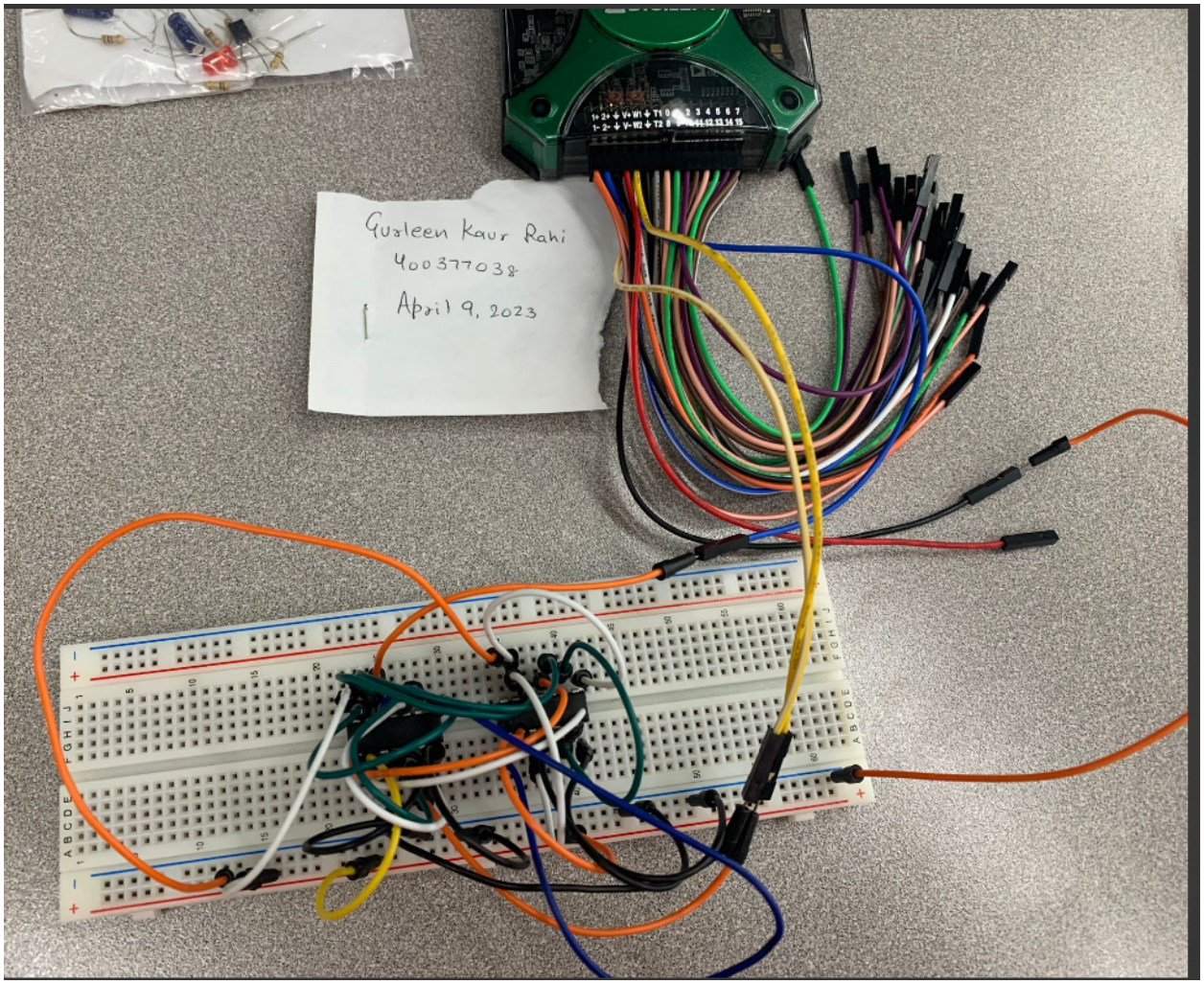

Figure 2: Picture of the physical circuit

As shown in the circuit above, the ideal sizing is available in the hardware design. However, to improve the performance of the circuit, sometimes we have to replace some of the elements with the one with similar properties to achieve to make the circuit work effectively and efficiently.

Speaking about the qualitative impact on the performance of the circuit, there are various ways by which the performance of the circuit can be affected. To illustrate, if the P-Mosfets are very tiny in comparison to the N-Mosfets, the output signal's rise and fall timings may be slower, leading to a greater propagation delay and a slower circuit speed. The circuit may use more power and have a long delay for the complementary signal if the PMOS transistors are too large, on the other hand. In either situation, it's critical to optimize the size ratio depending on the particular needs and limitations of the design in order to achieve the desired circuit performance.

Testing

1. **Functional Testing: Use the digital IO pins on the AD2 to demonstrate that the circuit implements the XOR function.**

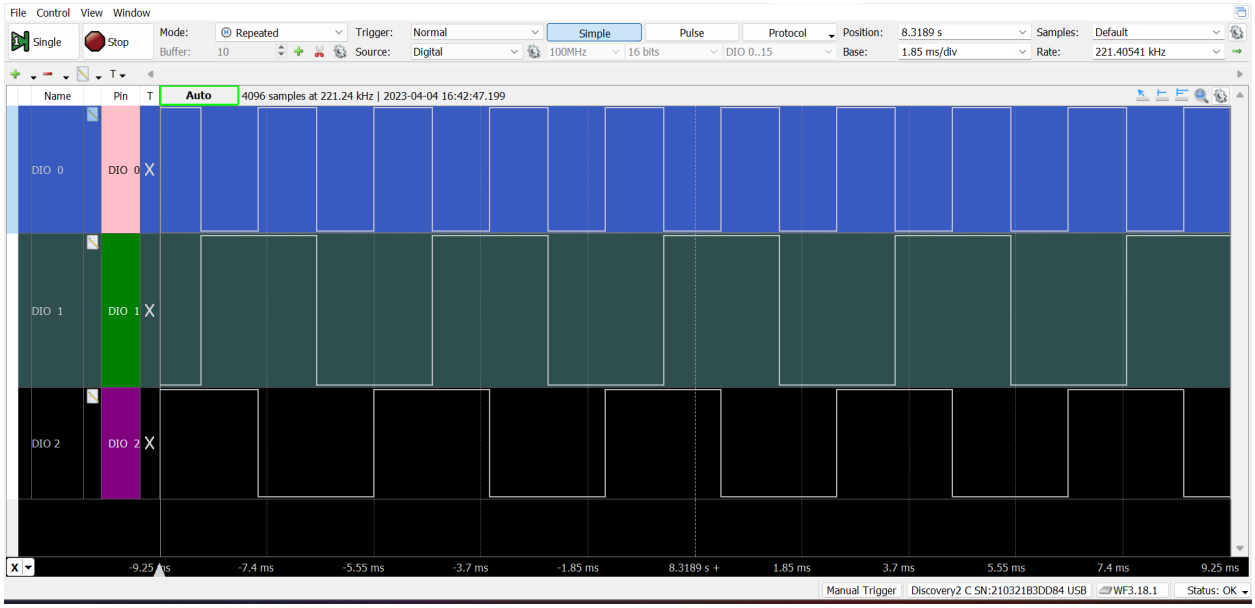

Figure 3: Functional Testing Results

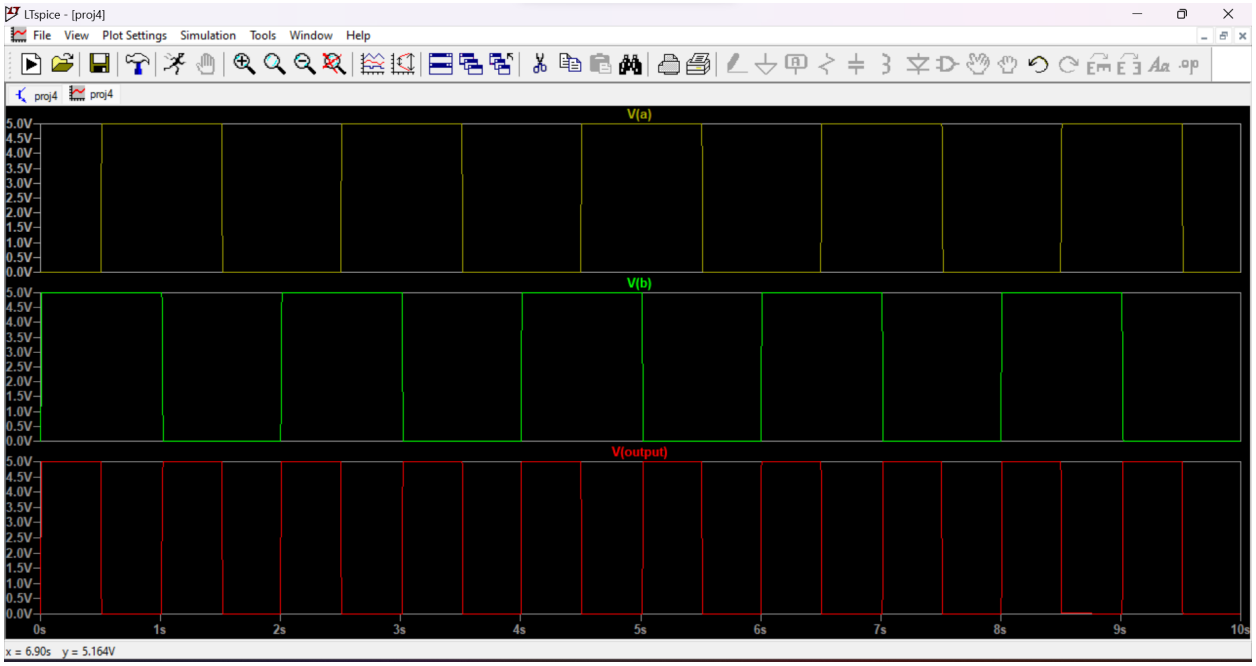

Figure 4: Simulation Results

We can see that the graphs in Figures 2 and 3 are very similar to each other. The graphs above show how the circuit implements the XOR function with the relatively input supplies V(a) and V(b) and the output voltage V(Output). The results of both graphs match the truth table of the XOR gate. For example, in the functional testing graph, from -7.4 ms to -6.0 ms (approx), the state combination is 1 1 0 for the output, first and second input respectively. This is true with respect to the truth table for the XOR gate. For the simulation results, at 4s, the combination is 0 1 1 for the first input, a second input, and output respectively. Therefore, both graphs are valid and do match each other.

2. **Static level Testing: Set one of the inputs to logic -1 (+5V). Set the 2nd input as a square wave between 0 and 5V. Measure the output on the oscilloscope. Determine V_H and V_L. Switch the two inputs and determine V_H and V_L change.**

First test

Figure 5: Wavegen settings for both inputs (Test 1)

The functional testing is done by connecting the Digital IO pins from AD2 to the hardware design of the circuit. Figure 5 shows the wavegen settings for both inputs. By running the scope, we will get the waveform for the output. This is shown in Figure 6 below.

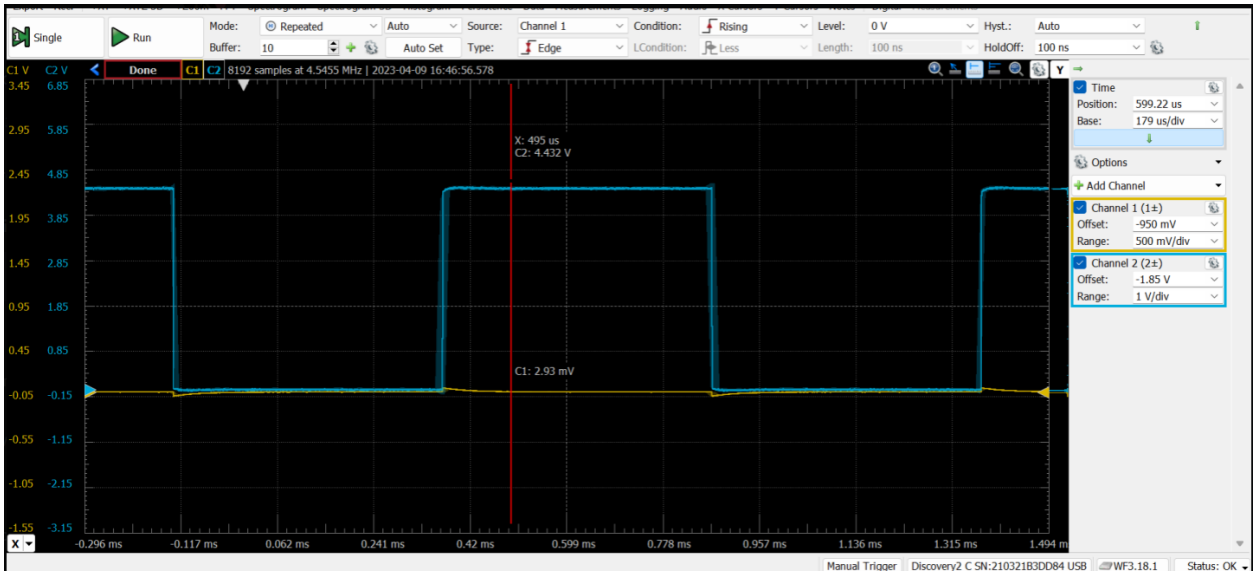

Figure 6: Output waveform on the oscilloscope

From the picture above we can see the logic high value is around 4.80 V and the logic low value is around 0 V. Any vertical translations in the graph could be due to any systematic errors. This is due to the fact that during static level testing, the output of the gate is measured while one input is held constant at a logic high level and the other input is a square wave that alternates between 0V and 5V. This indicates that the switched input has no impact on the voltage levels that the state is altered in the output.

The internal architecture of the gate and the thresholds of the transistors employed in the gate determine the voltage levels (V(high) and V(low)) at which the output changes state. These thresholds are established by the fabrication process of the gate and are independent of the particular input values. Since the values of V(high) and V(low) are defined by the internal architecture of the gate and not by the specific input values, switching the inputs should not change these values.

3. **Set one of the inputs to logic-1 (+5V). Set the 2nd input as a square wave with a 2.5 V offset. Gradually decrease the amplitude of this 2nd input until the logic function fails. Determine V_{IH} and V_{IL}.**

Second Test

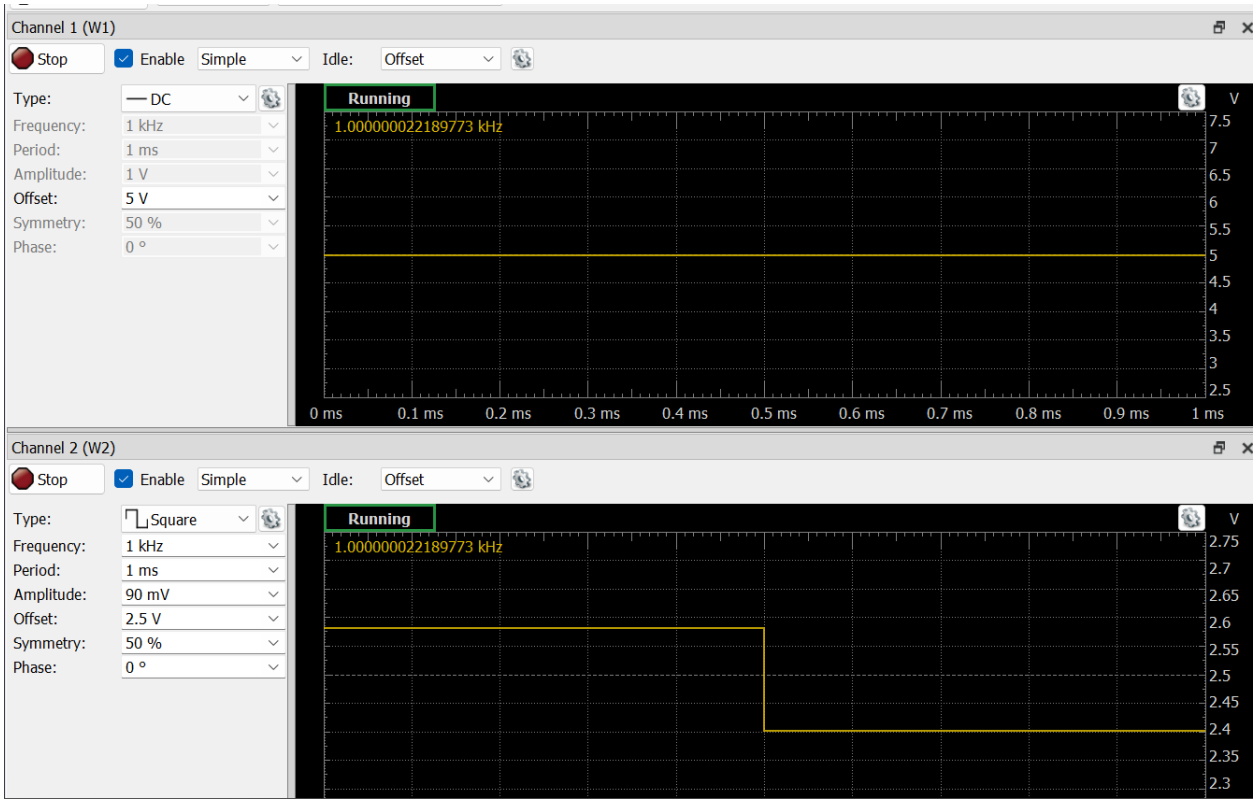

Figure 7: Wavegen settings for both inputs (Test 2)

Figure 7 describes the wavegen settings for both input supplies when doing the second test. For the second input (Channel 2), 90 mV amplitude produced a precise graph which is why I chose that value to produce the output graph. The output graph is shown in Figure 8. The interval between input signal transitions may be so brief at high frequencies and tiny input amplitudes that the response time of the XOR gate becomes a crucial influence. The gate may create a glitch output that does not accurately reflect the XOR function if its response time is longer than the interval between input signal changes. According to our graph,

The parasitic capacitances and inductances of the circuit can also become considerable at high frequencies, which can have an impact on how the XOR gate behaves. The transmission of a signal may be delayed by parasitic capacitances, whereas it may be distorted and attenuated by parasitic inductances. These effects can be reduced by designing XOR gates with quicker response times, fewer parasitic capacitances and inductances, and greater input signal amplitudes. In order to confirm that the XOR gate satisfies the required performance criteria, it can also be tested and characterized at the anticipated operating frequency and input amplitudes.

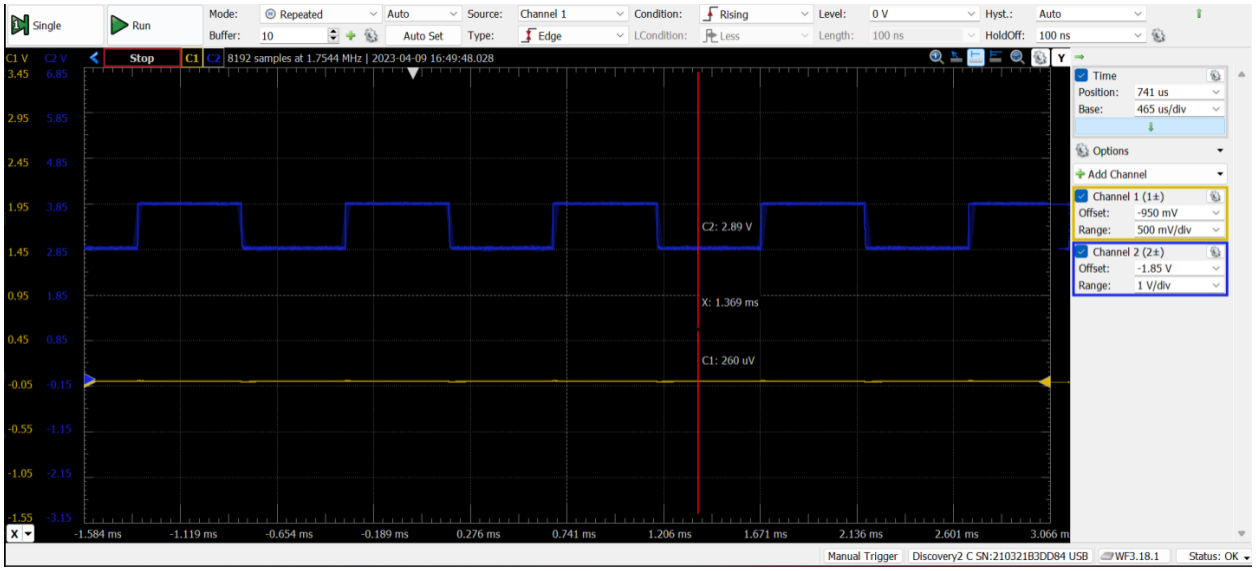

Figure 8: Output waveform from Oscilloscope

Timing

a. Set one of the inputs to logic-1 (+5V). Set the 2nd input as a square wave between 0 and 5V. Connect a 100 nF capacitor at the output to simulate a load.
    1) Determine the rise and fall times at the output waveform.

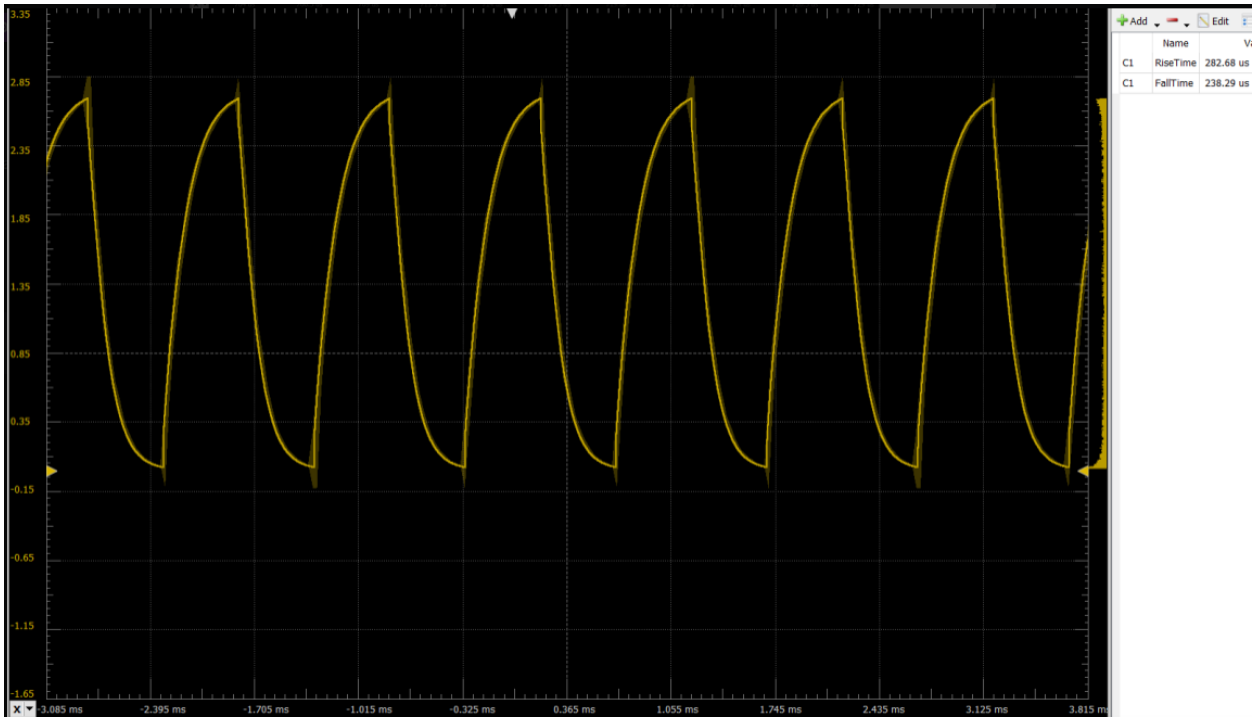

Figure 9: Output waveform demonstrating rise and fall times

As we can see from the graph above, the rise and fall time of the output waveform when a 100nF capacitor was used is approximately 283us and 238us respectively.

    2) Determine τ_{PLH}, τ_{PHL}, and τ_P.

For τ_{PLH}, τ_{PHL}, and τ_P, we were able to determine from our waveform that τ_{PLH} is equal to 102us, τ_{PHL} to 109us, and τ_P is the result of τ_{PHL} and τ_{PLH} added together and divided by two, which is equal to 105.5us.

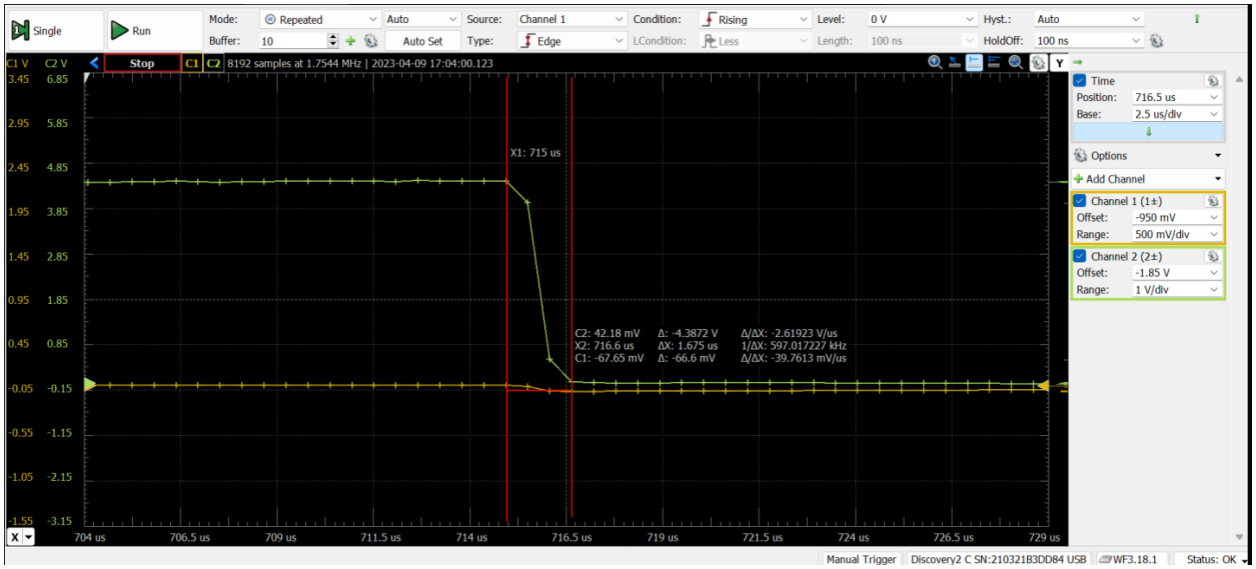

Figure 10: A closer view of the square waveform