# ELECENG 2CF3: Assignment 2

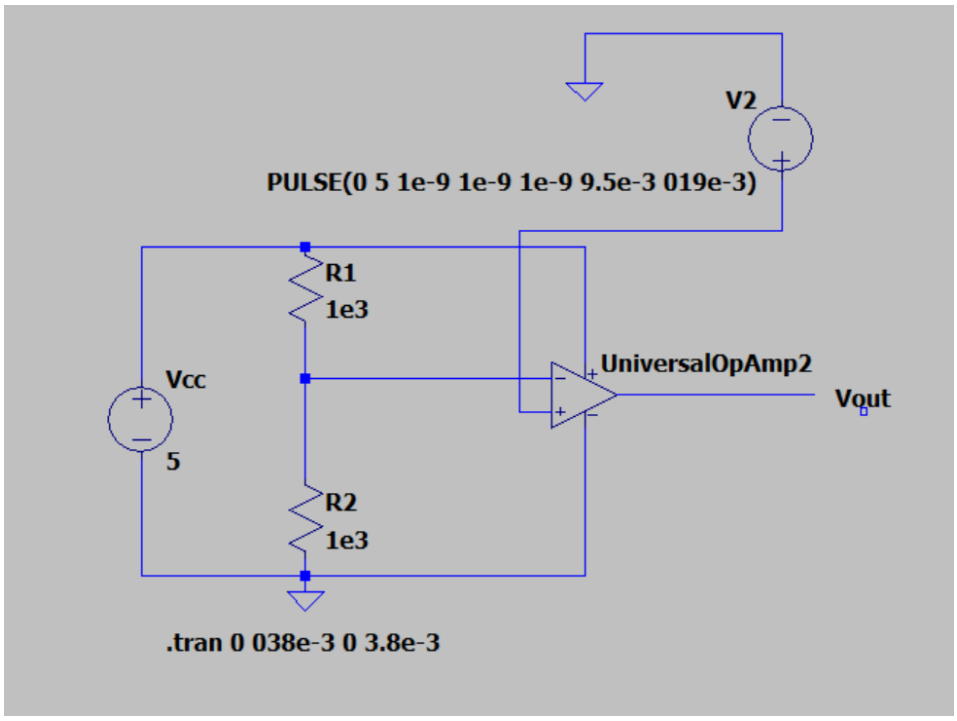
Name: Gurleen Kaur Rahi

Student ID: 400377038

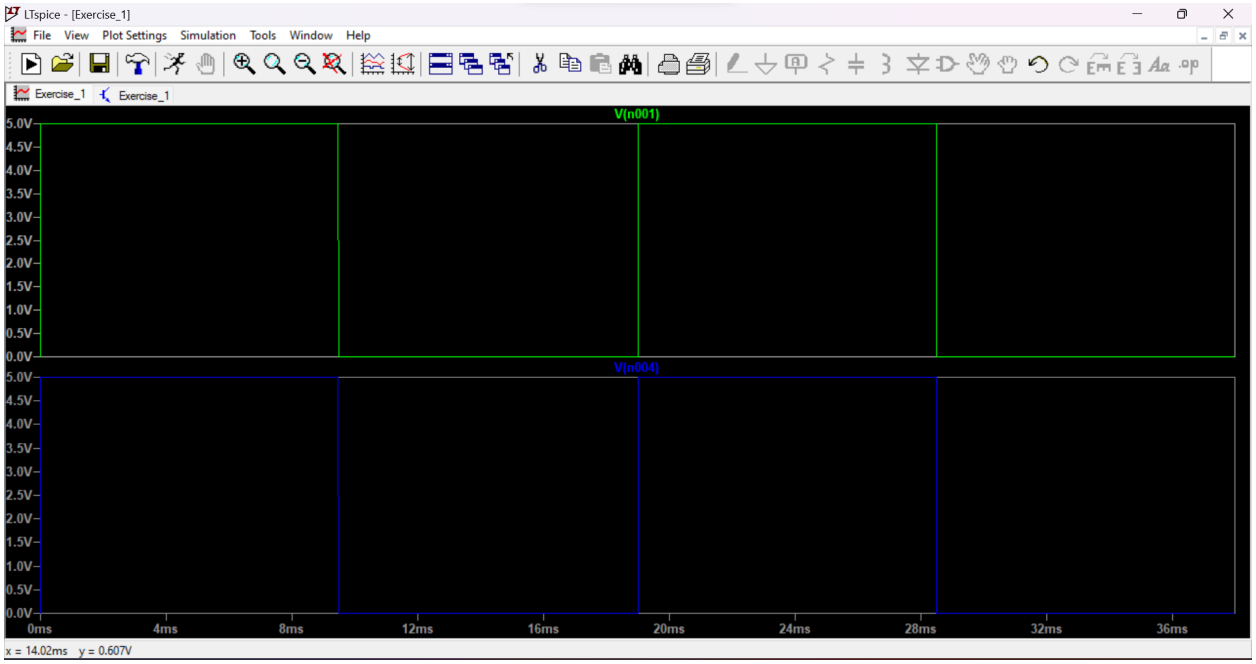
MacId: rahig

# Exercise #1: Simulate a Buffer in LTspice

1. **Include the complete schematic.**




2. **Include the two waveforms resulting from the simulation, with the output voltage below the input voltage as described above.**



3. **Include the complete netlist.**

```
Vcc N002 0 5
R1 N002 N003 1e3
R2 N003 0 1e3
XUniversalOpAmp2 N001 N003 N002 0 N004 level2 Avol=1Meg GBW=10Meg Slew=10Meg
Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
V2 N001 0 PULSE(0 5 1e-9 1e-9 1e-9 9.5e-3 019e-3)
.tran 0 038e-3 0 3.8e-3
.lib UniversalOpAmp2.lib
.backanno
.end
```

4. **Include the name of the LTspice with the buffer circuit.**

   Exercise_1.asc

5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.**

   Yes, the simulation results match the expected behavior. This is because the simulation's behavior was expected to have the same graph for Vin and Vout since we are using a digital logic buffer. The equation of the digital logic buffer proves that the value of Vin and Vout should be the same since their ratio is equal to 1. Therefore, their graphs should also be the same. This shows that our simulation results match the expected behavior.

6. **Explain how you derived the two resistors' values.**

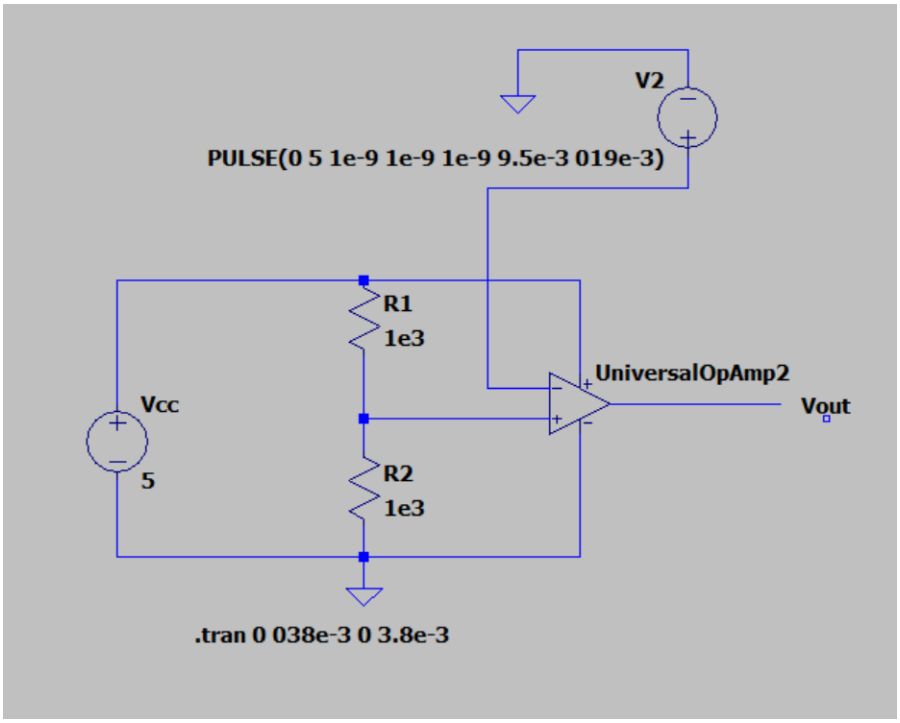
   The resistor values are derived using the rule of voltage division. Voltage division shows that we will get simulation not just for R=1k ohm for each resistor value, but for any value as long as both resistors have the same resistance value.

7. **It was noted that a unit-gain amplifier is not suitable as a buffer because we would like the output to be either voltage high or low even if the input voltage is intermediate. Comment on why this behavior is desirable.**

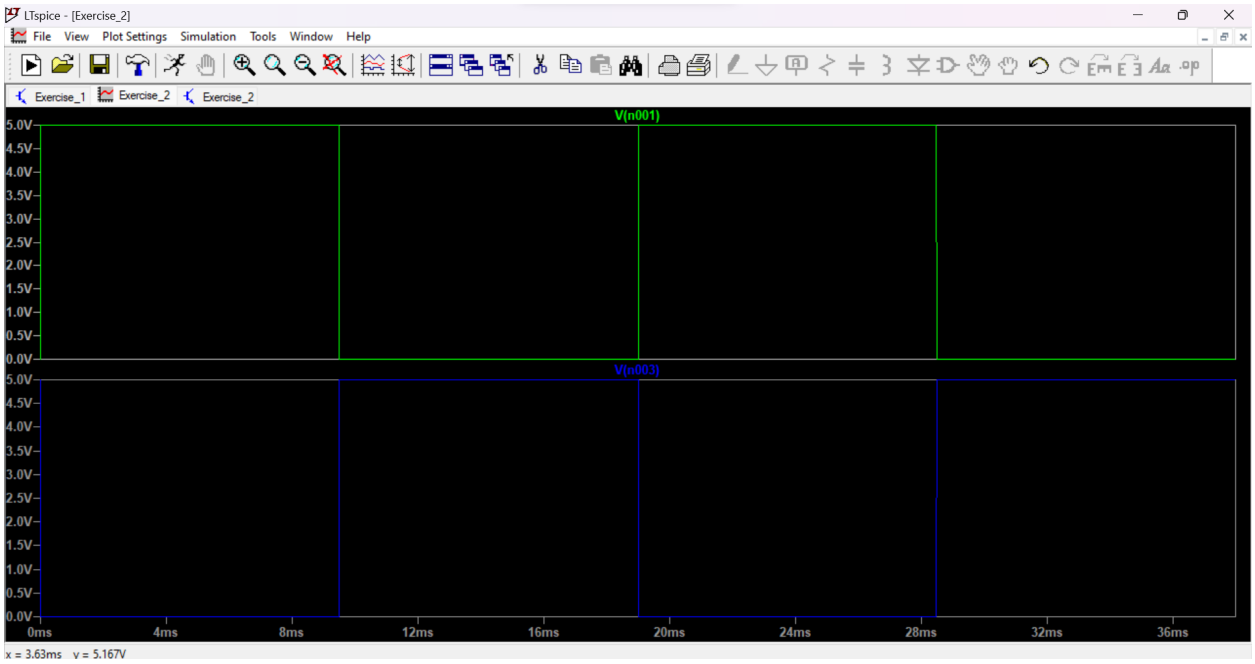
   Since digital communication uses binary numbers, circuit outputs are expected to be either be high or low. To satisfy this need, even with an intermediate input, a high or low voltage is preferred. The input and output are equal since the input is not amplified while using a unity-gain buffer. Unity gain buffers are inappropriate because an intermediate voltage output is undesirable.

## Exercise #2: Simulate a NOT gate in LTspice

1. **Include the complete schematic.**




2. **Include the two waveforms resulting from the simulation, with the output voltage below the input voltage, as described above.**



3. **Include the complete netlist.**

```
Vcc N002 0 5
V2 N001 0 PULSE(0 5 1e-9 1e-9 1e-9 9.5e-3 019e-3)
R1 N002 N004 1e3
R2 N004 0 1e3
XUniversalOpAmp2 N004 N001 N002 0 N003 level2 Avol=1Meg GBW=10Meg Slew=10Meg
Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
.tran 0 038e-3 0 3.8e-3
.lib UniversalOpAmp2.lib
.backanno
.end
```

4. **Include the name of the LTspice file with the NOT-gate circuit.**

   Exercise_2.asc

5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.**

   Yes, the simulation behavior matches with the expected behavior. Since by using the NOT gate and since VA is applied to the inverting input and the reference voltage is applied to the non-inverting input, we have swapped the terminals of the op-amp. Therefore, the simulation for the Vout is expected to behave opposite to that of the VA. The graph above shows that the simulation result matches with the expected behavior.

6. **Explain why swapping the driving voltages of the inverting and non-inverting inputs turned the non-inverting buffer of Exercise 1 into an inverting buffer.**

   This is because, in an inverting buffer, the input signal is connected to the inverting terminal of the op-amp, while the output signal is connected to the non-inverting terminal. This results in the gain of -R2/R1 as the output is the $180^{o}$ horizontal translation of the input signal. This is why by swapping the driving voltages from Exercise 1 turns the non-inverting buffer into an inverting buffer.

7. **Include the output requirement for the NOT gate. It is not necessary to show its derivation.**

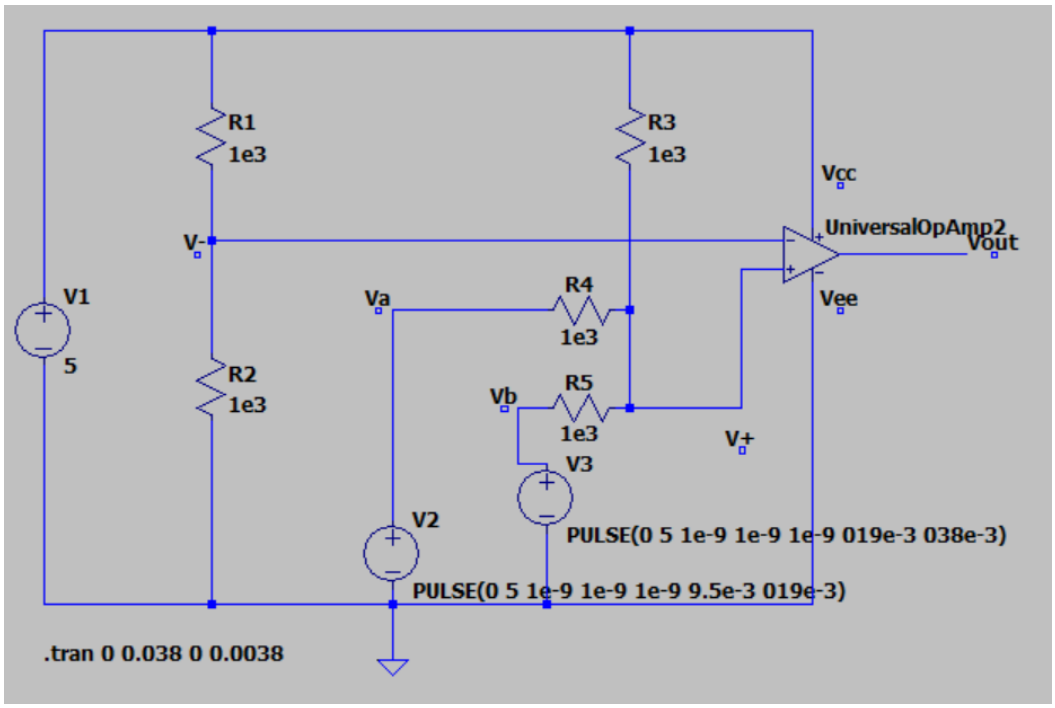
   The output requirement for the NOT gate is shown below.

   $V_{OUT}$ = 5V for VA < 2.5 V

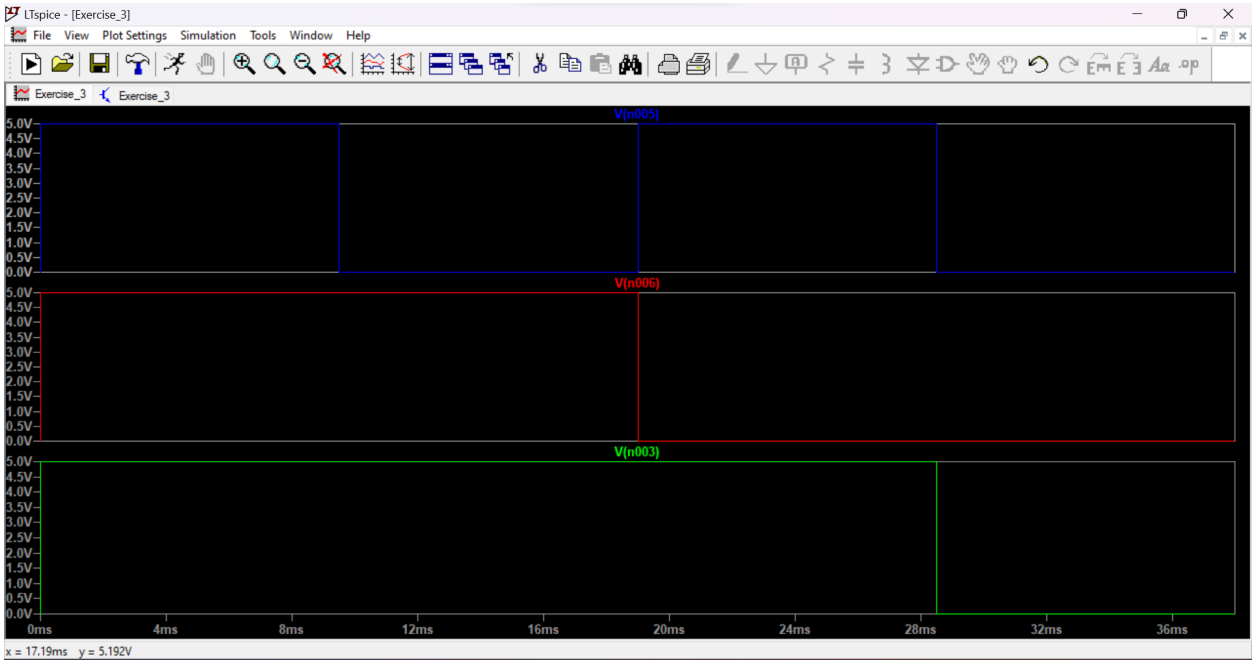
   $V_{OUT}$ = 0V for VA > 2.5 V

## Exercise #3: Simulate an OR gate in LTspice

1. **Include the complete schematic.**




2. **Include the three waveforms resulting from the simulation, with the output voltage below the input voltages as described above.**



3. **Include the complete netlist.**

```
V1 N001 0 5
R1 N001 N002 1e3
R2 N002 0 1e3
R3 N001 N004 1e3
R4 N004 N005 1e3
R5 N004 N006 1e3
V3 N006 0 PULSE(0 5 1e-9 1e-9 1e-9 019e-3 038e-3)
XUniversalOpAmp2 N004 N002 N001 0 N003 level2 Avol=1Meg GBW=10Meg Slew=10Meg
Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
V2 N005 0 PULSE(0 5 1e-9 1e-9 1e-9 9.5e-3 019e-3)
.tran 0 0.038 0 0.0038
.lib UniversalOpAmp2.lib
.backanno
.end
```

4. **Include the name of the LTspice file with the OR-gate circuit.**

   Exercise_3.asc

5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.**

   The simulation results match the expected behavior as this circuit is modified using an OR gate. That means if either of the inputs is greater than 2.5 V, the output is high. This is shown in the graph above.

6. **Analyze the node at the non-inverting input of the op-amp to prove that:**

$$V_+ = V = \frac{V_{CC} + V_A + V_B}{3}$$

   **If all three resistors branching from it have the same value R.**

KCL at node $V_+$

$$\frac{V_+ - V_B}{R_5} + \frac{V_+ - V_a}{R_4} + \frac{V_+ - V_{cc}}{R_3} = 0$$

Since $R_3 = R_4 = R_5 = R$

$$\frac{3V_+ - (V_a + V_b + V_{cc})}{R} = 0$$

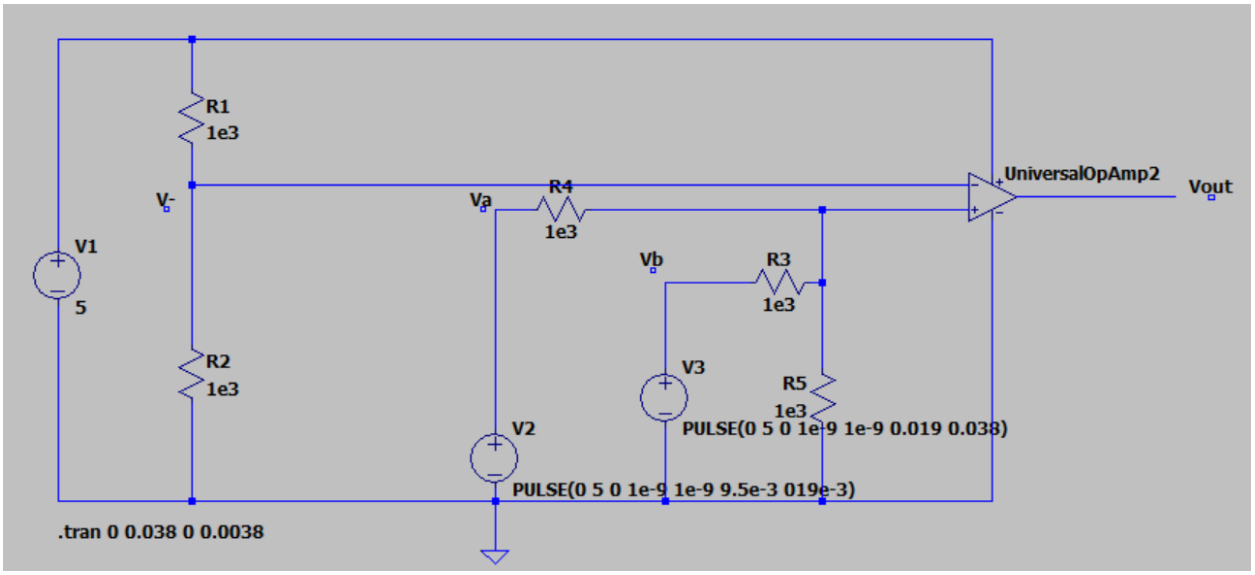
$$V_+ = \frac{V_a + V_b + V_{cc}}{3} = \bar{V}$$

7. **Include the output requirement for the OR gate.**

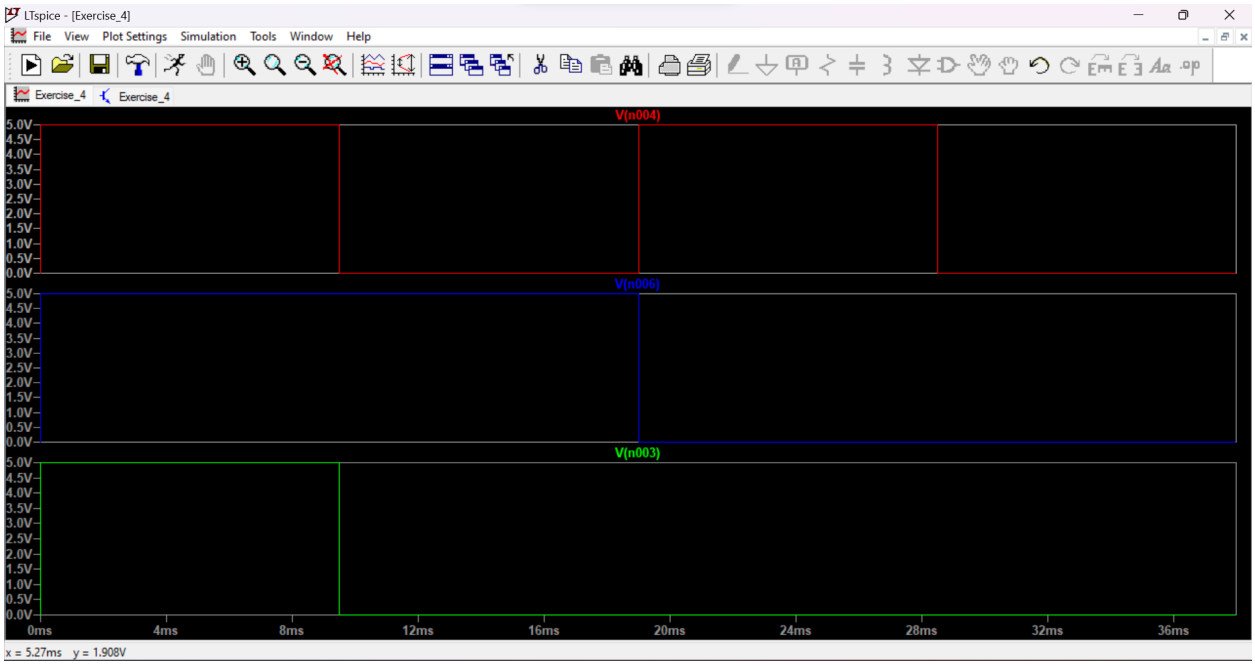
$V_{OUT} = 0$ V for $V_+ < 2.5$ V
$V_{OUT} = 5$ V for $V_+ > 2.5$ V

## Exercise #4: Simulate an AND gate in LTspice

1. **Include the complete schematic.**



2. **Include the three waveforms resulting from the simulation, with the output voltage below the input voltages, as described above.**




3. **Include the complete netlist.**

V1 N001 0 5
V3 N006 0 PULSE(0 5 0 1e-9 1e-9 0.019 0.038)
R1 N001 N002 1e3
R2 N002 0 1e3
R3 N005 N006 1e3
R4 N005 N004 1e3
R5 0 N005 1e3
XUniversalOpAmp2 N005 N002 N001 0 N003 level2 Avol=1Meg GBW=10Meg Slew=10Meg Ilimit=25m Rail=0 Vos=0 En=0 Enk=0 In=0 Ink=0 Rin=500Meg
V2 N004 0 PULSE(0 5 0 1e-9 1e-9 9.5e-3 019e-3)
.tran 0 0.038 0 0.0038
.lib UniversalOpAmp2.lib
.backanno
.end

4. **Include the name of the LTspice file with the AND-gate circuit.**

Exercise_4.asc

5. **Comment on whether the simulation results match the expected behavior, including a description of the expected behavior and any differences or anomalies in the simulation results.**

   Yes, my simulation behavior matches the expected behavior of the simulation. This is because since we are using an AND gate, we need both inputs high in order for our output to be high. My graph shows similar results, the output voltage is high only when both input voltages are high.

6. **A NAND gate is an AND gate with its output inverted. Of course, it can be made by cascading an AND gate and a NOT gate, but suggest how it might instead be designed with a single op-amp.**

   Similar to how a NOT gate can be made with just one op-amp, a NAND gate can also be made with just one. The op amp's output would then be inverted by switching the two inputs. If the pulse sources are connected to the inverting input and the constant voltage is applied to the non-inverting input of this circuit, it will function as a NAND gate.