RAMAIAH
Institute of Technology

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(Autonomous Institute, Affiliated to VTU)
Accredited by NBA & NAAC with 'A' Grade

SEMESTER END EXAMINATIONS – JANUARY 2020

Program	:	**B.E : Electronics and Communication Engineering**	**Semester**	:	**III**
Course Name	:	**Digital Design / Digital Electronics Circuits**	**Max. Marks**	:	**100**
Course Code	:	**EC33/EC304**	**Duration**	:	**3 Hrs**

Instructions to the Candidates:

- Answer one full question from each unit.

UNIT- I

1.	a)	Simply the following expression using K map and realize using NOR gates: $f(a, b, c, d) = \sum M(0,3,4,7,8,10,12,14)+\sum d(2,6)$	CO1	(07)
	b)	Write the condensed truth table for a 4 to 2 line priority encoder with a valid output where the highest priority is given to the highest bit position or input with highest index. Obtain the minimal SOP expression for the same and realize using logic gates.	CO1	(08)
	c)	Design 2 bit by 2 bit binary multiplier.	CO1	(05)
2.	a)	Design a 4 bit comparator.	CO1	(07)
	b)	Explain a BCD adder with example.	CO1	(07)
	c)	Explain with an example, how a decoder is implemented as a de-mux.	CO1	(06)

UNIT– II

3.	a)	A majority logic function is a Boolean function that is equal to 1 if the majority of the variables are equal to 1, equal to 0 otherwise. i. Write truth table for a 4-bit majority function ii. Write Verilog UDP for a 4-bit majority function.	CO2	(08)
	b)	Describe a 8:1 mux using 2:1 mux's in gate level Verilog coding. Write a test bench with 5 input combinations to check the correctness of this code.	CO2	(08)
	c)	Explain three ways of specifying delays in continuous assignment statements.	CO2	(04)
4.	a)	Design and develop a Verilog code for a 4 bit parallel adder using full adder as a component.	CO2	(07)
	b)	Design and develop a Verilog code for a 4:1 multiplexer in behavioral modeling. Write test bench for the same and show the simulation waveforms.	CO2	(08)
	c)	Explain three state gates with an example of 2:1 multiplexer and write the Verilog code for the same.	CO2	(05)

UNIT- III

5.	a)	Convert: i) SR flip flop to T flip flop	CO3	(06)

ii) JK flip flop to D flip flop.

b) Explain the working of a four-bit ripple up-counter, with the help of a logic diagram, timing diagram and counting sequence. CO3 (06)

c) Design a MOD-8 synchronous counter using JK-flip flops. Write the excitation table, state transition table and draw its logic diagram. CO3 (08)

6. a) Differentiate between Asynchronous Counter and synchronous Counter. CO3 (04)

b) Write the characteristic tables, Obtain the characteristic equation for D, SR & T flip flop. CO3 (08)

c) Design a 4-bit register using positive edge triggered D flip-flops to operate as indicated in the table below: CO3 (08)

Mode select		Register operation
a_0	a_1	
0	0	hold
0	1	Synchronous clear
1	0	Complement contents
1	1	Circular shift right

UNIT- IV

7. a) Write Verilog Behavioral model for a D type flip flop: CO4 (06)
   i) Without reset
   ii) With asynchronous reset.

b) Write the Verilog code for the following flipflop conversions: CO4 (10)
   i) D flip flop from JK flip flop
   ii) T flip flop from JK flip flop.

c) Differentiate between Mealy and Moore machine. CO4 (04)

8. a) Write Verilog structural modeling for 4-bit universal shift registers, using D flipflop. CO4 (10)

b) Write a Verilog code and test the functionality of 4-bit ripple counter using D flip flop. CO4 (10)

UNIT- V

9. a) Explain the read and write operation performed by RAM. CO5 (06)

b) Define PLA and Implement the following function using 4X4X2 PLA with only uncomplemented outputs CO5 (10)
$F_1(a,b,c,d) = \sum m(2,4,5,10,12,13,14)$
$F_2(a,b,c,d) = \sum m(2,9,10,11,13,14,15)$

c) Differentiate between PLA and PAL. CO5 (04)

10. a) Design a combinational circuit using a ROM. The circuit accepts a 3-bit number and generates an output binary number equal to the square of the input number. CO5 (10)

b) What is Logic synthesis, explain with the flow chart for designing a digital system. CO5 (10)

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