RAMAIAH
Institute of Technology

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(Autonomous Institute, Affiliated to VTU)
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SEMESTER END EXAMINATIONS FEBRUARY – MARCH 2021

Program	:	**B.E. : Electronics and Communication Engineering**	**Semester**	:	**III**
Course Name	:	**Digital Design**	**Max. Marks**	:	**100**
Course Code	:	**EC33**	**Duration**	:	**3 Hrs**

Instructions to the Candidates:
- Answer one full question from each unit.

UNIT- I

1.	a)	Simplify the Boolean Functions using three variable K-Map: i. F(w,x,y,z)=Σ(1,4,5,6,12,14,15) ii. F(a,b,c,d)=∏(1,3,5,7,13,15)	CO1	(06)
	b)	Design a combinational circuit that converts a four-bit Gray code to a four-bit Binary number. Implement the circuit with exclusive-OR gates.	CO1	(06)
	c)	Implement the Boolean function *f(abcd)*= ∑m(4,5,7,8,10,12,13,15) using a 4:1 MUX and external gates if, i) *c* and b are connected to select lines S_1 and S_0 respectively. ii) *a* and *d* are connected to select lines S_1 and S_0 respectively.	CO1	(08)
2.	a)	Using a decoder and external gates, design the combinational circuit defined by the following the Boolean Functions: F1=x'yz'+xz, F2=xy'z'+x'y, F3=x'y'z'+xy	CO1	(06)
	b)	Draw and explain the block diagram of BCD Adder with examples.	CO1	(08)
	c)	Implement 2-to-1 line MUX and 4-to-1 line MUX using Three State gates.	CO1	(06)

UNIT – II

3.	a)	Write the Verilog code for 1-bit full adder using UDP-AND and UDP-OR.	CO2	(08)
	b)	Write the dataflow description of BCD to excess-3 code converter.	CO2	(06)
	c)	Write the Behavioral Description of 2 to 4 Decoder.	CO2	(06)
4.	a)	Write the Verilog code and Verify a 4 to 1 mux, using a test bench.	CO2	(10)
	b)	Write the Verilog code and Verify a gate level hierarchical model for 4-bit RCA using bottom-up approach.	CO2	(10)

UNIT – III

5.	a)	What is a sequential circuit? Discuss the different types of sequential circuit.	CO3	(04)
	b)	Explain Johnson Counter, with its circuit diagram, and timing diagram.	CO3	(08)
	c)	Explain the operation of a positive edge triggered 'D' flip flop with the help of a logic diagram and truth table. Draw the relevant waveforms.	CO3	(08)
6.	a)	Explain the following: i) Switch debouncing and its elimination. ii) Race around problem and its elimination.	CO3	(04)
	b)	Explain the working principle of a mod-8 binary ripple counter, configured using positive edge triggered T flip flop. Also draw the timing diagram.	CO3	(08)
	c)	What is a shift register? Draw the logic diagram of a 4 bit serial in serial out (SISO) shift register using negative edge triggered JK or D flip-flops and explain its operation with the waveform to shift the binary number 1010 into the register.	CO3	(08)

UNIT – IV

7.	a)	Explain D-flip flop with the help of its truth table and gate level implementation. Write Verilog code in behavioral description for D-latch.	CO4	(10)
	b)	Write the behavioral description of a 4-bit universal shift register.	CO4	(10)
8.	a)	Explain in detail the Mealy and Moore models of FSM.	CO4	(05)
	b)	Write a Verilog code for converting a JK flip flop into D flip flop.	CO4	(05)
	c)	Write the structural description of a 4-bit universal shift register.	CO4	(10)

UNIT – V

9.	a)	Implement the following functions using PAL & PLA: $F_1(A,B,C) = \sum m(0,1,2,4,6,7)$ $F_2(A,B,C) = \sum m(2,4,5,6)$ $F_3(A,B,C) = \sum m(1,4,6)$	CO5	(10)
	b)	Explain Write and Read operations of RAM. Illustrate the operations of memory unit in Verilog HDL with timing waveforms.	CO5	(10)
10.	a)	Using the smallest size PROM PLD implement the decimal arithmetic expression $F(\alpha) = 5\alpha + 2$ for $0 \leq \alpha \leq 7$ where $F(\alpha)$ and α are in binary.	CO5	(10)
	b)	With neat diagram, explain the flowchart for HDL-based modeling, verification and synthesis.	CO5	(10)

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