EC35

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RAMAIAH Institute of Technology

(Autonomous Institute, Affiliated to VTU)
(Approved by AICTE, New Delhi & Govt. of Karnataka)
Accredited by NBA & NAAC with 'A+' Grade

SEMESTER END EXAMINATIONS – APRIL 2023

Program	:	**B.E. – Electronics and Communication Engineering**	**Semester**	:	**III**
Course Name	:	**Digital Design with HDL**	**Max. Marks**	:	**100**
Course Code	:	**EC35**	**Duration**	:	**3 Hrs**

Instructions to the Candidates:

- Answer one full question from each unit.

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UNIT - I

1.	a)	Simplify the following function using K-map and realize it using only NOR gates. f(a, b, c, d) = π M (4,5,6,7,8,12,13) + d (1,15).	CO1	(08)
	b)	Discuss the various levels of abstractions provided by Verilog HDL.	CO1	(05)
	c)	Write a Verilog code for the function F = AB+BC+CD using User defined primitives.	CO1	(07)
2.	a)	Draw the multi-level NOR circuit for the following expression: CD(B+C) A+(BC'+DE')	CO1	(06)
	b)	Determine the minimum sum of product expression for f(a, b, c, d) = ∑m (7,11,13,14,15) and realize it using only NAND gates.	CO1	(08)
	c)	What are Degenerate and Non degenerate forms, considering two level combinations of gates? Explain with an example for each form.	CO1	(06)

UNIT - II

3.	a)	Write a Verilog code for a 4-bit carry look ahead adder using data flow modelin.	CO2	(06)
	b)	Construct a 4-to-16-line decoder with five 2-to-4-line decoders with enable. Using a decoder and external gates, design the combinational circuit defined by the following three Boolean functions. (a) F 1 = x ' y z ' + x z F 2 = x y ' z ' + x ' y F 3 = x ' y ' z ' + x y	CO2	(07)
	c)	Construct a 16: 1 multiplexer with two 8: 1 and one 2: 1multiplexer and write the Verilog code using a behavioral description.	CO2	(07)
4.	a)	Using a case statement, write an HDL behavioral description of an eight-bit arithmetic-logic unit (ALU) and write the test bench for the same.	CO2	(07)
	b)	If A=12, B=-6, P=4'b10x1, Q=4'b1011 R=4'b10xx and S=4'b1110, perform the following using Verilog operators. i) A*B ii) ~B iii)A<=R iv)C={A[1],B[2:0],R[1:0]} v) Q>>2 vi)E=A +(S>>>3)	CO2	(06)
	c)	Design a four-bit combinational circuit 2's complementer. The output generates the 2's complement of the input binary number. Show that the circuit can be constructed with exclusive-OR gates.	CO2	(07)

UNIT - III

5.	a)	Describe a D Latch, with a logic diagram and function table	CO3	(05)
	b)	Analyze and obtain the logic diagram, next state table and state diagram of the sequential circuit specified by the following Flip Flop input equations: $D_A = A'X + BX$, $D_B = BX' + AB'X$	CO3	(10)
	c)	Write a Verilog code, using behavioral description for a JK flip flop, using case statement.	CO3	(05)

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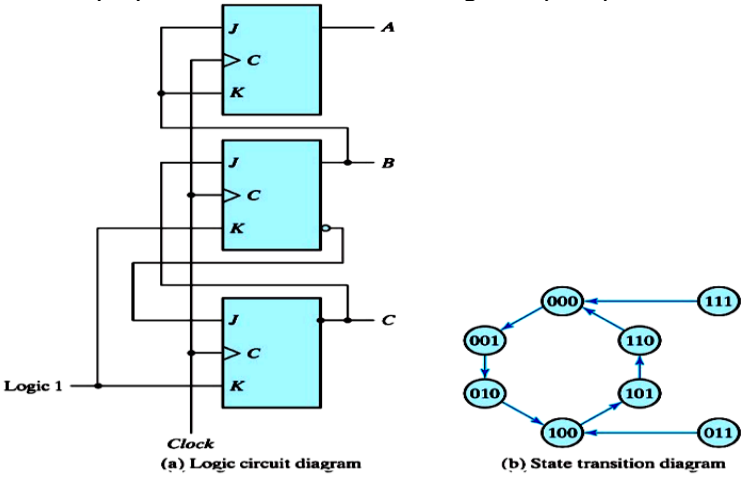
6.	a)	Construct a JK Flip Flop, with a D Flip flop and gates, and draw its circuit diagram.	CO3	(06)
	b)	Write a Verilog behavioral code to implement a T Flip Flop, from D Flip flop and gates.	CO3	(06)
	c)	Analyze and obtain the logic diagram, next state table of the sequential circuit specified by the following Flip Flop input equations: $J_A=B$, $K_A=Bx'$, $J_B=x'$, $K_B=A'x+Ax'=A\oplus x$	CO3	(08)

UNIT- IV

7.	a)	Design a four-bit shift register (not a universal shift register) with parallel load using D flip-flops. There are two control inputs: shift and load. When shift=1, the content of the register is shifted toward A3 by one position. New data are transferred into the register when load=1 and shift=0. If both control inputs are equal to 0, the content of the register does not change.	CO4	(08)
	b)	Write Verilog behavioral code for 4-bit ripple up/down counter using T flip flop.	CO4	(06)
		A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if: i. The normal outputs of the flip-flops are connected to the clock; and ii. The complement outputs of the flip-flops are connected to the clock?	CO4	(06)
8.	a)	Design a 4-bit binary synchronous counter using D flip flops.	CO4	(10)
	b)	 Fig.8(b) Write Verilog structural description for the counter shown.	CO4	(10)

UNIT - V

9.	a)	The combinational circuit is defined by the function: $F_1(A,B,C)=\Sigma m(0,1,3,7)$ $F_2(A,B,C)= \Sigma m(1,2,5,6)$ Implement the circuit in PLA	CO5	(08)
	b)	Write a verilog code for read and write operation performed by ROM.	CO5	(08)
	c)	Differentiate between PLA,PAL and PROM	CO5	(04)
10.	a)	Implement the following functions using PLA with only un-completed outputs $F_1(A,B,C,D)=\Sigma m(2,4,5,10,12,13,14)$ $F_2(A,B,C,D)= \Sigma m(2,9,10,11,13,14,15)$	CO5	(10)
	b)	Explain the logic synthesis flow from RTL to gates.	CO5	(10)

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