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RAMAIAH Institute of Technology

(Autonomous Institute, Affiliated to VTU)
(Approved by AICTE, New Delhi & Govt. of Karnataka)
Accredited by NBA & NAAC with 'A+' Grade

SEMESTER END EXAMINATIONS – APRIL 2023

Program	:	**B.E. – Electronics and Communication Engineering**	**Semester**	:	**III**
Course Name	:	**Analog Electronics Circuits**	**Max. Marks**	:	**100**
Course Code	:	**EC33**	**Duration**	:	**3 Hrs**

Instructions to the Candidates:

- Answer one full question from each unit.

UNIT - I

1. a) Consider a single stage CE amplifier as shown in fig.1.a with R_s= 1KΩ , R_1=50KΩ, R_2= 2KΩ, R_c= 1KΩ, R_L=1.2KΩ, h_{fe}=50 ,h_{ie}=1.1kΩ, h_{oe}=25 μA/V and h_{re}=2.5x10^{-4}. Determine A_i, R_i, A_v and A_{vs}. CO1 (07)

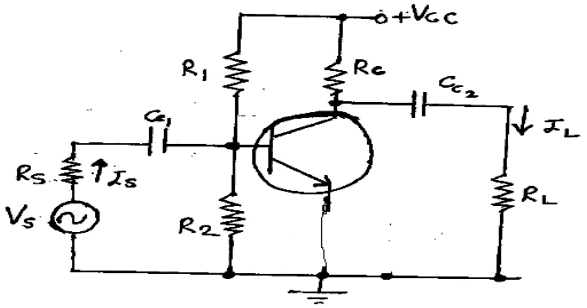

Fig.1(a)

b) Derive an expression for the Bandwidth of voltage series feedback amplifier. CO1 (06)

c) Discus the working of Transistorized RC phase shift oscillator. What are the demerits and merits of this circuit. CO1 (07)

2. a) Using h-parameter model for a transistor in CE configuration, Derive the expressions for A_i, Z_i, A_v and Y_O. CO1 (10)

b) An amplifier has mid-band voltage gain of 2000 with f_L=70Hz and f_H=600KHz, if 5% negative feedback is applied, Calculate gain, f_L,f_H and bandwidth with feedback. CO1 (06)

c) In a Colpitts oscillator, each inductor having the value of 200pF and 150pF each respectively and Inductor of 50μH.Compute the frequency of oscillations CO1 (04)

UNIT - II

3. a) Explain with neat circuit diagram the working of Complementary symmetry of class B power amplifier with input and output waveforms. CO2 (10)

b) With neat sketches explain biasing of a JFET using self bias configuration and show the operating points. CO2 (10)

4. a) With neat circuit diagram explain the voltage divider Bias of JFET and show the operating points. CO2 (10)

b) A transformer – coupled Class A power amplifier drives a load of 8Ω through a 3:1 transformer with VCC = 24V, the circuit delivers 2W to the load. The transformer efficiency is 80% find: CO2 (10)
   i) Power across the transformer primary.
   ii) Rms voltage across load and transformer primary
   iii) Rms values of load current and primary current.
   iv) Conversion efficiency if dc collector current is 260mA.

UNIT - III

5. a) For the circuit shown determine V_G, I_{DQ}, V_{GSQ}, V_D, V_S, V_{DSQ} and locate the operating point on the transfer characteristics. CO3 (08)

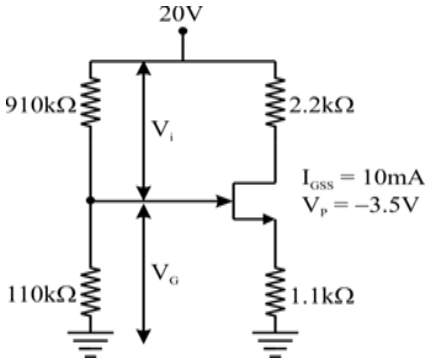

Fig.5(a)

b) Using the small signal model of a emitter follower derive necessary expressions: CO3 (06)

i. $A_V = \frac{V_0}{V_i}$ ii. Z_i iii. Z_0 iv. Z_0'

c) Explain the transfer characteristics of JFET and show how to evaluate the trans conductance? CO3 (06)

6. a) With JFET small signal model of a common source amplifier derive expressions for input impedance, voltage gain and output impedance. CO3 (06)

b) Given circuit of self-bias the drop across R_S is 1.7V and $R_D = 2k\Omega$ and $R_S = 0.51k\Omega$. Assume V_P is $-4V$. Find I_{DQ}, V_{GSQ}, I_{DSS}, V_D and V_G. Draw theload line. CO3 (08)

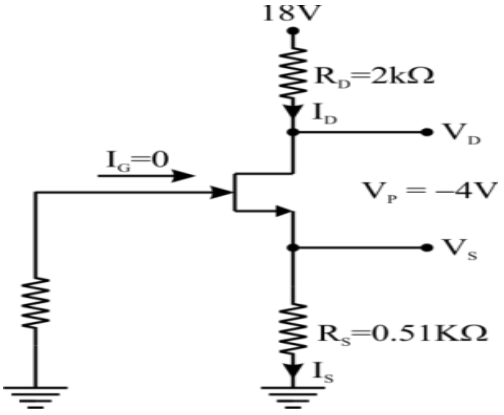

Fig.6(b)

c) Define pinch-off voltage and dynamic drain resistance for JFET. Mention the applications of JFET. CO3 (06)

UNIT- IV

7.	a)	With neat diagram construct an instrumentation amplifier and derive an expression for output voltage and explain the importance of amplifier?	C04	(08)
	b)	Explain the following parameters of an operational amplifier: i) input offset voltage ii) slew rate iii)CMRR iv)PSRR.	C04	(08)
	c)	Mention any two differences between difference amplifier and instrumentation amplifier.	CO4	(04)
8.	a)	Design a wide band rejection filter having fh=400Hz and fl=2kHz and pass band gain of 2 find the Q value of the filter and plot the frequency response.	CO4	(10)
	b)	Explain the principle and operation of a sample and hold circuit.	CO4	(05)
	c)	Explain with circuit the operation of a Band rejection filter.	CO4	(05)

UNIT - V

9.	a)	Explain the operation of a 4-bit R-2R type DAC and derive the expression for the output voltage.	CO5	(06)
	b)	For the Schmitt trigger shown in fig. 9.b, calculate the trip points and hysteresis, if $V_{sat} = \pm 13.5V$. The resistances have a tolerance of $\pm$5%. What is the minimum hysteresis.	CO5	(08)

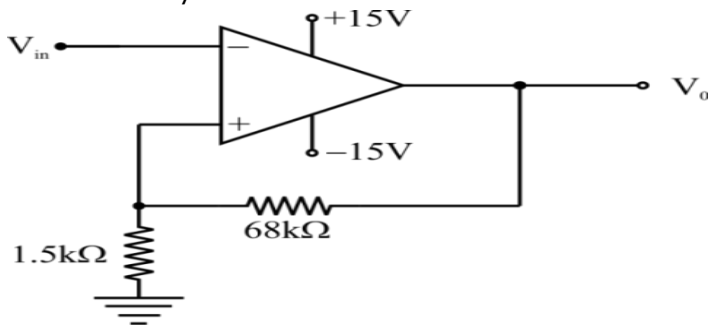

Fig.9(b)

	c)	Explain the working of monostable multivibrator using functional diagram of IC 555 timer.	CO5	(06)
10.	a)	Design an inverting Schmitt trigger circuit to have UTP=6V and LTP=-3.5V, use a 741 op-amp with $V_{cc} = \pm 18V$. Draw the input/output characteristic for the circuit.	CO5	(08)
	b)	Explain the working of a 3-bit flash type ADC.	CO5	(06)
	c)	Explain the working of astable multivibrator using functional diagram of IC555 timer.	CO5	(06)

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