

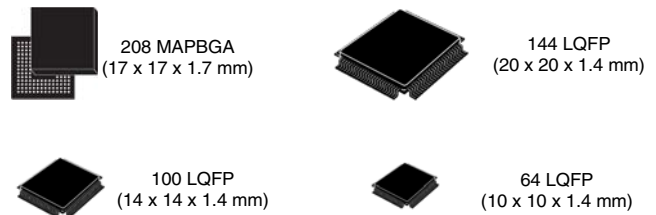
## MPC5604B/C Microcontroller Data Sheet

32-bit MCU family built on the Power Architecture® for automotive body electronics applications

### Features

- Single issue, 32-bit CPU core complex (e200z0)
  - Compliant with the Power Architecture® embedded category
  - Includes an instruction set enhancement allowing variable length encoding (VLE) for code size footprint reduction. With the optional encoding of mixed 16-bit and 32-bit instructions, it is possible to achieve significant code size footprint reduction.
- Up to 512 Kbytes on-chip data flash supported with the flash controller
- 64 (4 × 16) KB on-chip data flash memory with ECC
- Up to 48 Kbytes on-chip SRAM
- Memory protection unit (MPU) with 8 region descriptors and 32-byte region granularity
- Interrupt controller (INTC) with 148 interrupt vectors, including 16 external interrupt sources and 18 external interrupt/wakeup sources
- Frequency modulated phase-locked loop (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- Boot assist module (BAM) supports internal flash programming via a serial link (CAN or SCI)
- Timer supports input/output channels providing a range of 16-bit input capture, output compare, and pulse width modulation functions (eMIOS-lite)
- 10-bit analog-to-digital converter (ADC)
- 3 serial peripheral interface (DSPI) modules
- Up to 4 serial communication interface (LINFlex) modules

## MPC5604B/C



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## Introduction

- Up to 6 enhanced full CAN (FlexCAN) modules with configurable buffers
- 1 inter IC communication interface (I<sup>2</sup>C) module
- Up to 123 configurable general purpose pins supporting input and output operations (package dependent)
- Real Time Counter (RTC) with clock source from 128 kHz or 16 MHz internal RC oscillator supporting autonomous wakeup with 1 ms resolution with max timeout of 2 seconds
- Up to 6 periodic interrupt timers (PIT) with 32-bit counter resolution
- 1 System Module Timer (STM)
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 Class Two Plus standard
- Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) of IEEE (IEEE 1149.1)
- On-chip voltage regulator (VREG) for regulation of input supply for all internal levels

# 1 Introduction

## 1.1 Document overview

This document describes the features of the family and options available within the family members, and highlights important electrical and physical characteristics of the device. To ensure a complete understanding of the device functionality, refer also to the device reference manual and errata sheet.

## 1.2 Description

The MPC5604B/C is a family of next generation microcontrollers built on the Power Architecture® embedded category.

The MPC5604B/C family of 32-bit microcontrollers is the latest achievement in integrated automotive application controllers. It belongs to an expanding family of automotive-focused products designed to address the next wave of body electronics applications within the vehicle. The advanced and cost-efficient host processor core of this automotive controller family complies with the Power Architecture embedded category and only implements the VLE (variable-length encoding) APU, providing improved code density. It operates at speeds of up to 64 MHz and offers high performance processing optimized for low power consumption. It capitalizes on the available development infrastructure of current Power Architecture devices and is supported with software drivers, operating systems and configuration code to assist with users implementations.

Table 1. MPC5604B/C device comparison<sup>1</sup>

Feature	Device															
	MPC5602BxLH	MPC5602BxLL	MPC5602BxLQ	MPC5602CxLH	MPC5602CxLL	MPC5603BxLH	MPC5603BxLL	MPC5603BxLQ	MPC5603CxLH	MPC5603CxLL	MPC5604BxLH	MPC5604BxLL	MPC5604BxLQ	MPC5604CxLH	MPC5604CxLL	MPC5604BxMG
CPU	e200z0h															
Execution speed <sup>2</sup>	Static – up to 64 MHz															
Code Flash	256 KB						384 KB					512 KB				
Data Flash	64 KB (4 × 16 KB)															
RAM	24 KB			32 KB		28 KB			40 KB		32 KB			48 KB		
MPU	8-entry															
ADC	12 ch, 10-bit	28 ch, 10-bit	36 ch, 10-bit	8 ch, 10-bit	28 ch, 10-bit	12 ch, 10-bit	28 ch, 10-bit	36 ch, 10-bit	8 ch, 10-bit	28 ch, 10-bit	12 ch, 10-bit	28 ch, 10-bit	36 ch, 10-bit	8 ch, 10-bit	28 ch, 10-bit	36 ch, 10-bit
CTU	Yes															
Total timer I/O <sup>3</sup>	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit	12 ch, 16-bit	28 ch, 16-bit	56 ch, 16-bit
eMIOS																
• PWM + MC + IC/OC <sup>4</sup>	2 ch	5 ch	10 ch	2 ch	5 ch	2 ch	5 ch	10 ch	2 ch	5 ch	2 ch	5 ch	10 ch	2 ch	5 ch	10 ch
• PWM + IC/OC <sup>4</sup>	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	10 ch	20 ch	40 ch	10 ch	20 ch	40 ch
• IC/OC <sup>4</sup>	0 ch	3 ch	6 ch	0 ch	3 ch	0 ch	3 ch	6 ch	0 ch	3 ch	0 ch	3 ch	6 ch	0 ch	3 ch	6 ch
SCI (LINFlex)	3 <sup>5</sup>				4											
SPI (DSPI)	2	3		2	3	2	3		2	3	2	3		2	3	
CAN (FlexCAN)	2 <sup>6</sup>			5	6	3 <sup>7</sup>			5	6	3 <sup>7</sup>			5	6	
I <sup>2</sup> C	1															
32 kHz oscillator	Yes															
GPIO <sup>8</sup>	45	79	123	45	79	45	79	123	45	79	45	79	123	45	79	123
Debug	JTAG															Nexus2+

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5604BxMG products in 208 MAPBGA packages

Table 1. MPC5604B/C device comparison<sup>1</sup> (continued)

Feature	Device															
	MPC5602BxLH	MPC5602BxLL	MPC5602BxLQ	MPC5602CxLH	MPC5602CxLL	MPC5603BxLH	MPC5603BxLL	MPC5603BxLQ	MPC5603CxLH	MPC5603CxLL	MPC5604BxLH	MPC5604BxLL	MPC5604BxLQ	MPC5604CxLH	MPC5604CxLL	MPC5604BxMG
Package	64 LQFP <sup>9</sup>	100 LQFP	144 LQFP	64 LQFP <sup>9</sup>	100 LQFP	64 LQFP <sup>9</sup>	100 LQFP	144 LQFP	64 LQFP <sup>9</sup>	100 LQFP	64 LQFP <sup>9</sup>	100 LQFP	144 LQFP	64 LQFP <sup>9</sup>	100 LQFP	208 MAPBGA <sup>10</sup>

<sup>1</sup> Feature set dependent on selected peripheral multiplexing—table shows example implementation

<sup>2</sup> Based on 105 °C ambient operating temperature

<sup>3</sup> Refer to eMIOS section of device reference manual for information on the channel configuration and functions

<sup>4</sup> IC - Input Capture; OC - Output Compare; PWM - Pulse Width Modulation; MC - Modulus counter

<sup>5</sup> SCI0, SCI1 and SCI2 are available. SCI3 is not available.

<sup>6</sup> CAN0, CAN1 are available. CAN2, CAN3, CAN4 and CAN5 are not available.

<sup>7</sup> CAN0, CAN1 and CAN2 are available. CAN3, CAN4 and CAN5 are not available.

<sup>8</sup> I/O count based on multiplexing with peripherals

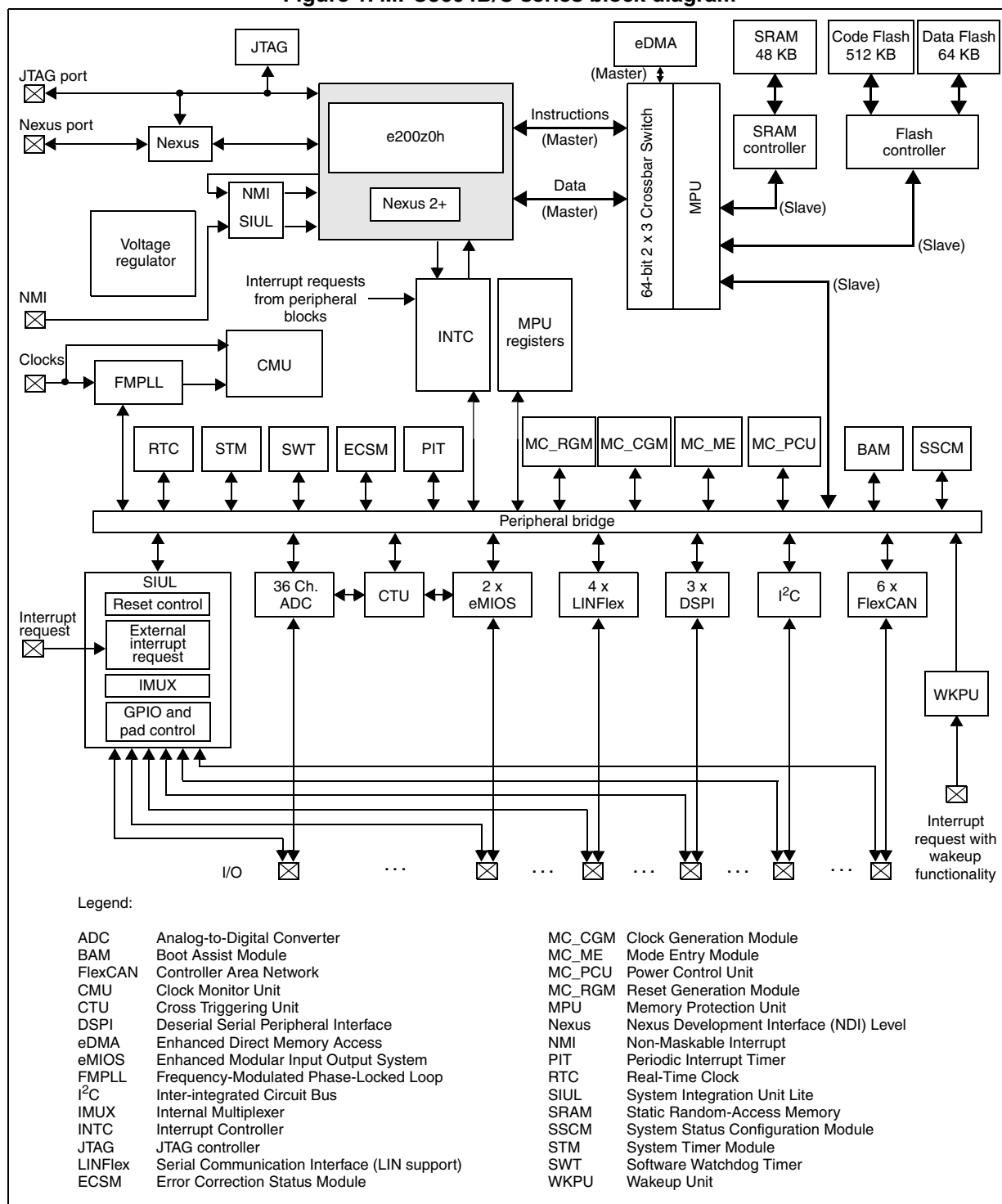
<sup>9</sup> All 64 LQFP information is indicative and must be confirmed during silicon validation.

<sup>10</sup> 208 MAPBGA available only as development package for Nexus2+

## 2 Block diagram

Figure 1 shows a top-level block diagram of the MPC5604B/C device series.

Figure 1. MPC5604B/C series block diagram



## Block diagram

Table 2 summarizes the functions of all blocks present in the MPC5604B/C series of microcontrollers. Please note that the presence and number of blocks varies by device and package.

**Table 2. MPC5604B/C series block summary**

Block	Function
Analog-to-digital converter (ADC)	Multi-channel, 10-bit analog-to digital-converter
Boot assist module (BAM)	A block of read-only memory containing VLE code which is executed according to the boot mode of the device
Clock monitor unit (CMU)	Monitors clock source (internal and external) integrity
Cross triggering unit (CTU)	Enables synchronization of ADC conversions with a timer event from the eMIOS or from the PIT
Deserial serial peripheral interface (DSPI)	Provides a synchronous serial interface for communication with external devices
Error Correction Status Module (ECSM)	Provides a myriad of miscellaneous control functions for the device including program-visible information about configuration and revision levels, a reset status register, wakeup control for exiting sleep modes, and optional features such as information on memory errors reported by error-correcting codes
Enhanced Direct Memory Access (eDMA)	Performs complex data transfers with minimal intervention from a host processor via “n” programmable channels.
Enhanced modular input output system (eMIOS)	Provides the functionality to generate or measure events
Flash memory	Provides non-volatile storage for program code, constants and variables
FlexCAN (controller area network)	Supports the standard CAN communications protocol
FMPLL (frequency-modulated phase-locked loop)	Generates high-speed system clocks and supports programmable frequency modulation
Internal multiplexer (IMUX) SIU subblock	Allows flexible mapping of peripheral interface on the different pins of the device
Inter-integrated circuit (I <sup>2</sup> C™) bus	A two wire bidirectional serial bus that provides a simple and efficient method of data exchange between devices
Interrupt controller (INTC)	Provides priority-based preemptive scheduling of interrupt requests
JTAG controller	Provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode
LINflex controller	Manages a high number of LIN (Local Interconnect Network protocol) messages efficiently with a minimum of CPU load
Clock generation module (MC_CGM)	Provides logic and control required for the generation of system and peripheral clocks
Mode entry module (MC_ME)	Provides a mechanism for controlling the device operational mode and mode transition sequences in all functional states; also manages the power control unit, reset generation module and clock generation module, and holds the configuration, control and status registers accessible for applications
Power control unit (MC_PCU)	Reduces the overall power consumption by disconnecting parts of the device from the power supply via a power switching device; device components are grouped into sections called “power domains” which are controlled by the PCU
Reset generation module (MC_RGM)	Centralizes reset sources and manages the device reset sequence of the device

**Table 2. MPC5604B/C series block summary (continued)**

Block	Function
Memory protection unit (MPU)	Provides hardware access control for all memory references generated in a device
Nexus development interface (NDI)	Provides real-time development support capabilities in compliance with the IEEE-ISTO 5001-2003 standard
Periodic interrupt timer (PIT)	Produces periodic interrupts and triggers
Real-time counter (RTC)	A free running counter used for time keeping applications, the RTC can be configured to generate an interrupt at a predefined interval independent of the mode of operation (run mode or low-power mode)
System integration unit (SIU)	Provides control over all the electrical pad controls and up 32 ports with 16 bits of bidirectional, general-purpose input and output signals and supports up to 32 external interrupts with trigger event configuration
Static random-access memory (SRAM)	Provides storage for program code, constants, and variables
System status configuration module (SSCM)	Provides system configuration and status data (such as memory size and status, device mode and security status), device identification data, debug status port enable and selection, and bus and peripheral abort enable/disable
System timer module (STM)	Provides a set of output compare events to support AUTOSAR and operating system tasks
System watchdog timer (SWT)	Provides protection from runaway code
Wakeup unit (WKPU)	The wakeup unit supports up to 18 external sources that can generate interrupts or wakeup events, of which 1 can cause non-maskable interrupt requests or wakeup events.
Crossbar (XBAR) switch	Supports simultaneous connections between two master ports and three slave ports. The crossbar supports a 32-bit address bus width and a 64-bit data bus width

## 3 Package pinouts and signal descriptions

### 3.1 Package pinouts

The available LQFP pinouts and the 208 MAPBGA ballmap are provided in the following figures. For pin signal descriptions, please refer to the device reference manual.

Figure 2. LQFP 64-pin configuration (top view)<sup>1</sup>

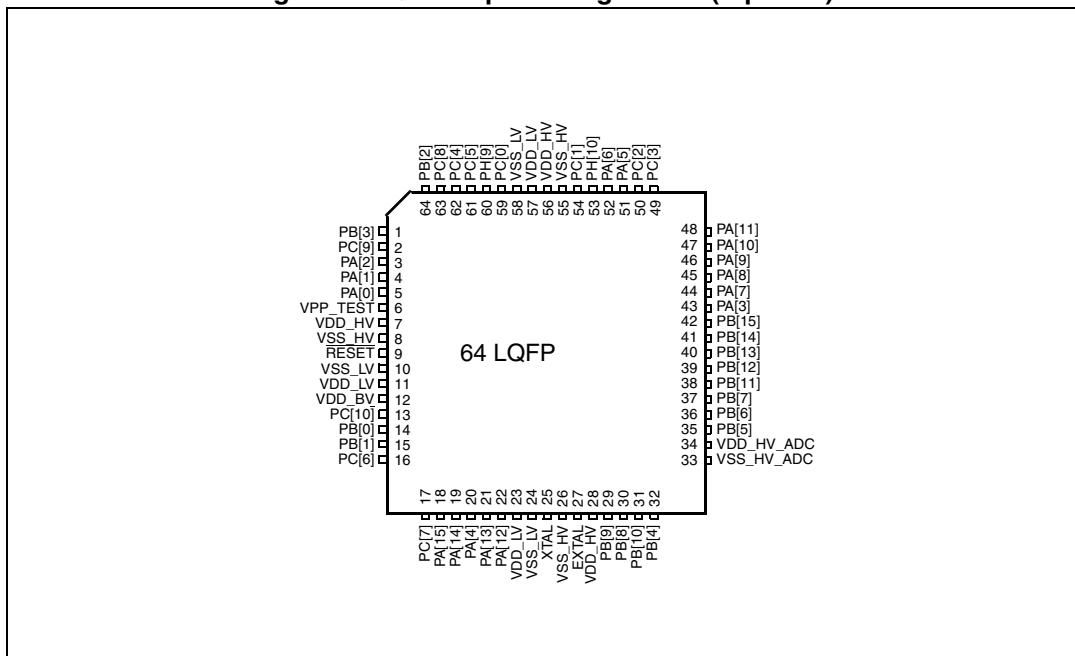
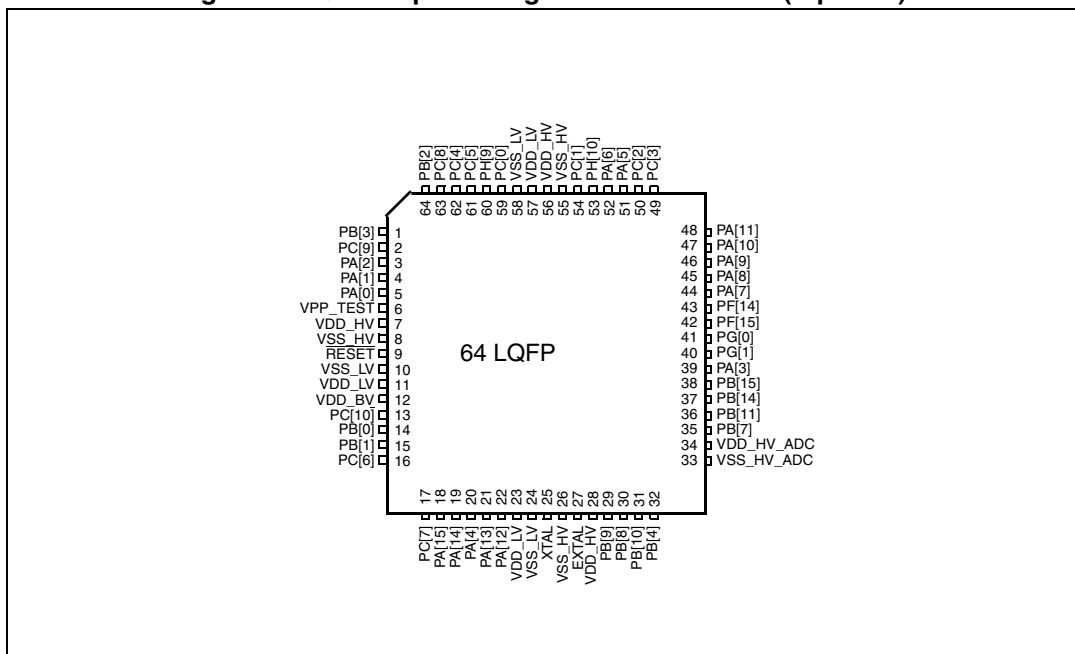


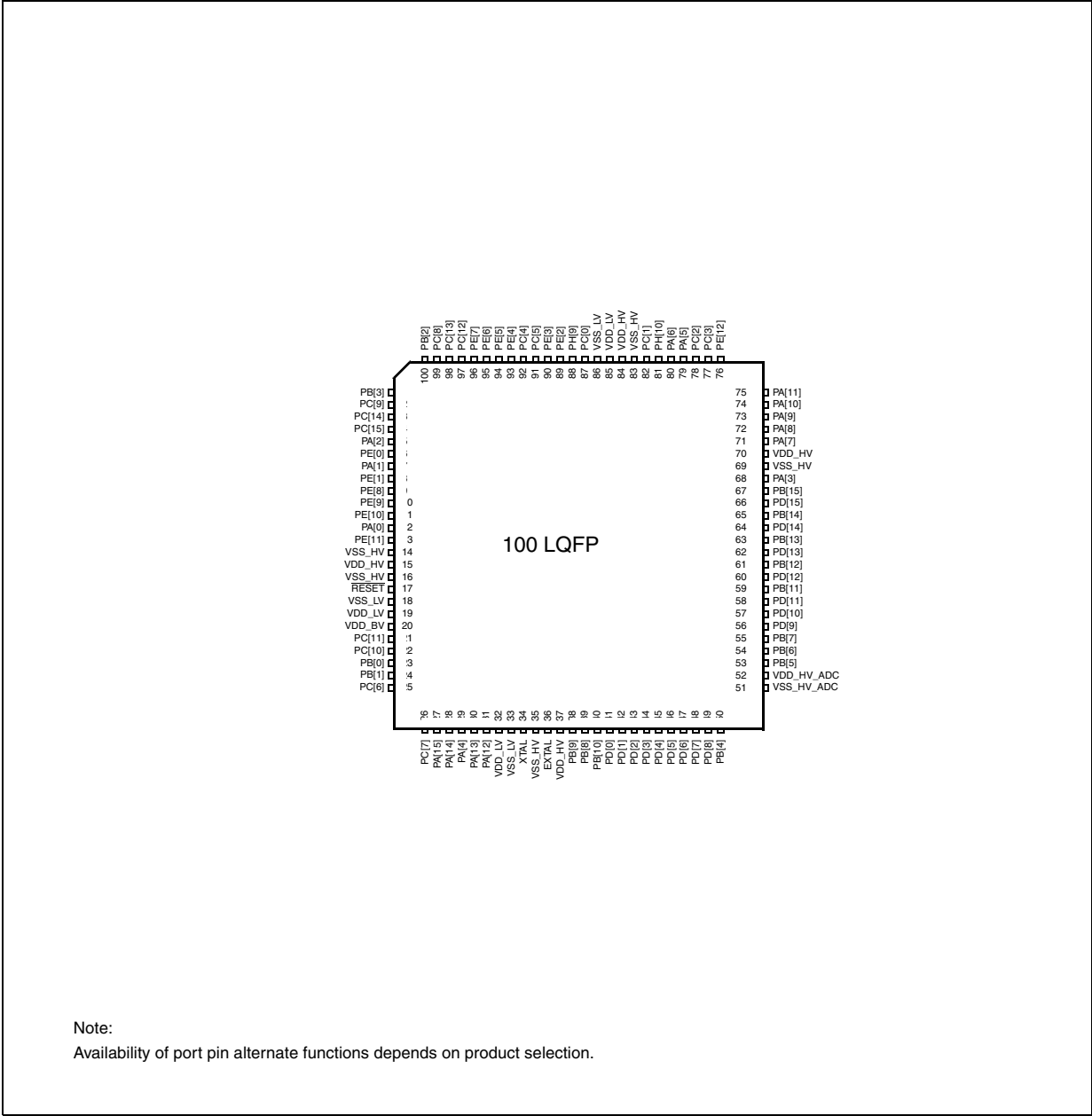
Figure 3. LQFP 64-pin configuration 5CAN 4LIN (top view)<sup>2</sup>



1. All 64 LQFP information is indicative and must be confirmed during silicon validation.

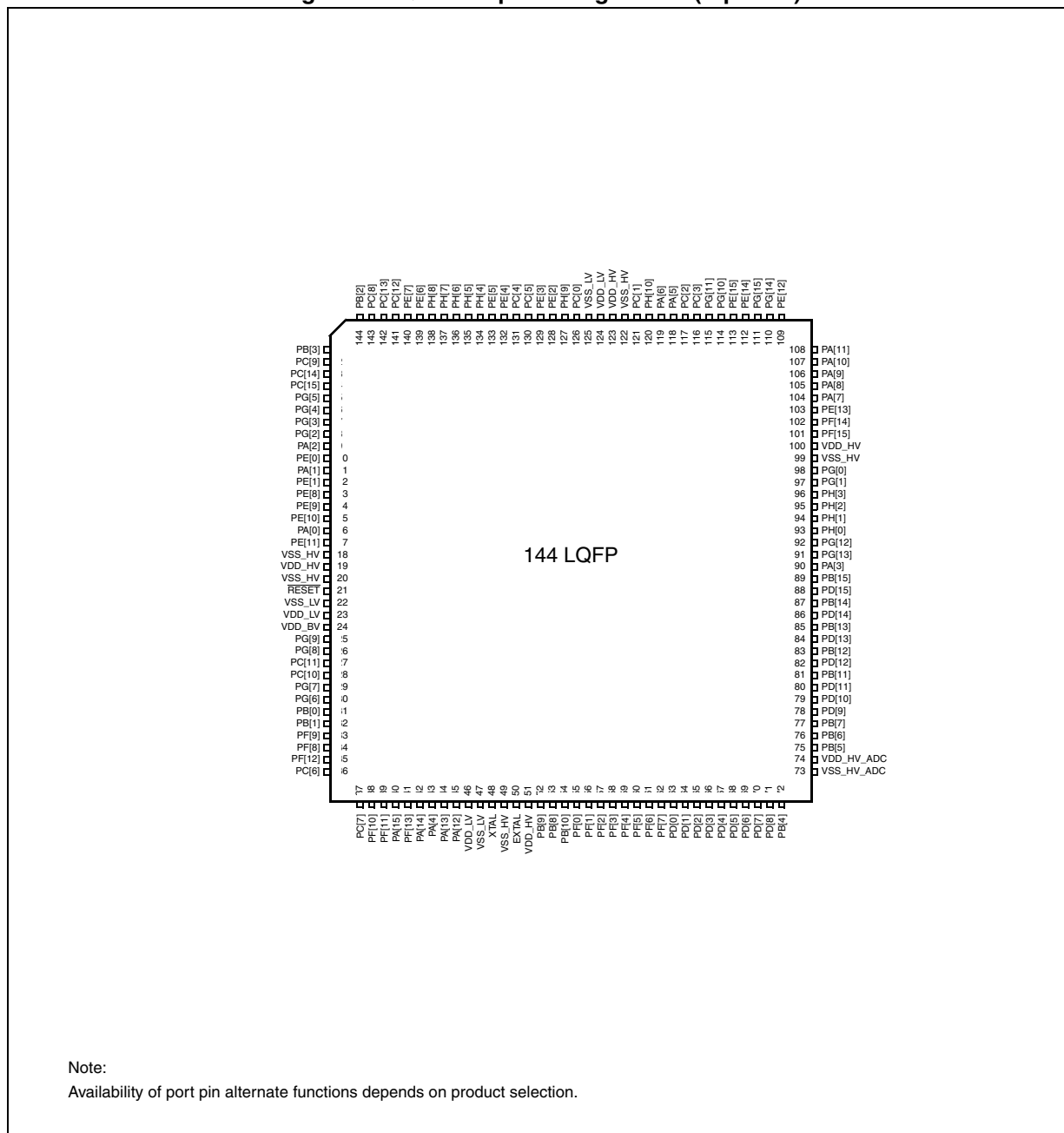


Figure 4. LQFP 100-pin configuration (top view)



2. All 64 LQFP information is indicative and must be confirmed during silicon validation.

Figure 5. LQFP 144-pin configuration (top view)



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	PC[8]	PC[13]	NC	NC	PH[8]	PH[4]	PC[5]	PC[0]	NC	NC	PC[2]	NC	PE[15]	NC	NC	NC	A
B	PC[9]	PB[2]	NC	PC[12]	PE[6]	PH[5]	PC[4]	PH[9]	PH[10]	NC	PC[3]	PG[11]	PG[15]	PG[14]	PA[11]	PA[10]	B
C	PC[14]	VDD_HV	PB[3]	PE[7]	PH[7]	PE[5]	PE[3]	VSS_LV	PC[1]	NC	PA[5]	NC	PE[14]	PE[12]	PA[9]	PA[8]	C
D	NC	NC	PC[15]	NC	PH[6]	PE[4]	PE[2]	VDD_LV	VDD_HV	NC	PA[6]	NC	PG[10]	PF[14]	PE[13]	PA[7]	D
E	PG[4]	PG[5]	PG[3]	PG[2]									PG[1]	PG[0]	PF[15]	VDD_HV	E
F	PE[0]	PA[2]	PA[1]	PE[1]									PH[0]	PH[1]	PH[3]	PH[2]	F
G	PE[9]	PE[8]	PE[10]	PA[0]									VDD_HV	NC	NC	MSEO	G
H	VSS_HV	PE[11]	VDD_HV	NC									MDO3	MDO2	MDO0	MDO1	H
J	RESET	VSS_LV	NC	NC									NC	NC	NC	NC	J
K	EVTI	NC	VDD_BV	VDD_LV									NC	PG[12]	PA[3]	PG[13]	K
L	PG[9]	PG[8]	NC	EVTO									PB[15]	PD[15]	PD[14]	PB[14]	L
M	PG[7]	PG[6]	PC[10]	PC[11]									PB[13]	PD[13]	PD[12]	PB[12]	M
N	PB[1]	PF[9]	PB[0]	NC	NC	PA[4]	VSS_LV	EXTAL	VDD_HV	PF[0]	PF[4]	NC	PB[11]	PD[10]	PD[9]	PD[11]	N
P	PF[8]	NC	PC[7]	NC	NC	PA[14]	VDD_LV	XTAL	PB[10]	PF[1]	PF[5]	PD[0]	PD[3]	VDD_HV_ADC	PB[6]	PB[7]	P
R	PF[12]	PC[6]	PF[10]	PF[11]	VDD_HV	PA[15]	PA[13]	NC	OSC32K_XTAL	PF[3]	PF[7]	PD[2]	PD[4]	PD[7]	VSS_HV_ADC	PB[5]	R
T	NC	NC	NC	MCKO	NC	PF[13]	PA[12]	NC	OSC32K_EXTAL	PF[2]	PF[6]	PD[1]	PD[5]	PD[6]	PD[8]	PB[4]	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Note: 208 MAPBGA available only as development package for Nexus 2+.

NC = Not connected

Figure 6. 208 MAPBGA configuration

## 3.2 Pin muxing

Table 1 defines the pin list and muxing for this device.

Each entry of Table 1 shows all the possible configurations for each pin, via the alternate functions. The default function assigned to each pin after reset is indicated by AF0.

**Table 1. Functional port pin descriptions**

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PA[0]	PCR[0]	AF0 AF1 AF2 AF3 —	GPIO[0] E0UC[0] CLKOUT — WKUP[19] <sup>4</sup>	SIUL eMIOS0 CGL — WKPU	I/O I/O O — I	M	Tristate	5	5	12	16	G4
PA[1]	PCR[1]	AF0 AF1 AF2 AF3 — —	GPIO[1] E0UC[1] — — NMI <sup>5</sup> WKUP[2] <sup>4</sup>	SIUL eMIOS0 — — WKPU WKPU	I/O I/O — — I I	S	Tristate	4	4	7	11	F3
PA[2]	PCR[2]	AF0 AF1 AF2 AF3 —	GPIO[2] E0UC[2] — — WKUP[3] <sup>4</sup>	SIUL eMIOS0 — — WKPU	I/O I/O — — I	S	Tristate	3	3	5	9	F2
PA[3]	PCR[3]	AF0 AF1 AF2 AF3 —	GPIO[3] E0UC[3] — — EIRQ[0]	SIUL eMIOS0 — — SIUL	I/O I/O — — I	S	Tristate	43	39	68	90	K15
PA[4]	PCR[4]	AF0 AF1 AF2 AF3 —	GPIO[4] E0UC[4] — — WKUP[9] <sup>4</sup>	SIUL eMIOS0 — — WKPU	I/O I/O — — I	S	Tristate	20	20	29	43	N6
PA[5]	PCR[5]	AF0 AF1 AF2 AF3	GPIO[5] E0UC[5] — —	SIUL eMIOS0 — —	I/O I/O — —	M	Tristate	51	51	79	118	C11
PA[6]	PCR[6]	AF0 AF1 AF2 AF3 —	GPIO[6] E0UC[6] — — EIRQ[1]	SIUL eMIOS0 — — SIUL	I/O I/O — — I	S	Tristate	52	52	80	119	D11

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PA[7]	PCR[7]	AF0 AF1 AF2 AF3 —	GPIO[7] E0UC[7] LIN3TX — EIRQ[2]	SIUL eMIOS0 LINFlex_3 — SIUL	I/O I/O O — I	S	Tristate	44	44	71	104	D16
PA[8]	PCR[8]	AF0 AF1 AF2 AF3 — N/A <sup>6</sup> —	GPIO[8] E0UC[8] — — EIRQ[3] ABS[0] LIN3RX	SIUL eMIOS0 — — SIUL BAM LINFlex_3	I/O I/O — — I I I	S	Input, weak pull-up	45	45	72	105	C16
PA[9]	PCR[9]	AF0 AF1 AF2 AF3 N/A <sup>6</sup>	GPIO[9] E0UC[9] — — FAB	SIUL eMIOS_0 — — BAM	I/O I/O — — I	S	Pull-down	46	46	73	106	C15
PA[10]	PCR[10]	AF0 AF1 AF2 AF3	GPIO[10] E0UC[10] SDA —	SIUL eMIOS_0 I2C_0 —	I/O I/O I/O —	S	Tristate	47	47	74	107	B16
PA[11]	PCR[11]	AF0 AF1 AF2 AF3	GPIO[11] E0UC[11] SCL —	SIUL eMIOS0 I2C_0 —	I/O I/O I/O —	S	Tristate	48	48	75	108	B15
PA[12]	PCR[12]	AF0 AF1 AF2 AF3 —	GPIO[12] — — — SIN_0	SIUL — — — DSPI0	I/O — — — I	S	Tristate	22	22	31	45	T7
PA[13]	PCR[13]	AF0 AF1 AF2 AF3	GPIO[13] SOUT_0 — —	SIUL DSPI_0 — —	I/O O — —	M	Tristate	21	21	30	44	R7
PA[14]	PCR[14]	AF0 AF1 AF2 AF3 —	GPIO[14] SCK_0 CS0_0 — EIRQ[4]	SIUL DSPI_0 DSPI_0 — SIUL	I/O I/O I/O — I	M	Tristate	19	19	28	42	P6

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PA[15]	PCR[15]	AF0 AF1 AF2 AF3 —	GPIO[15] CS0_0 SCK_0 — WKUP[10] <sup>4</sup>	SIUL DSPI_0 DSPI_0 — WKPU	I/O I/O I/O — I	M	Tristate	18	18	27	40	R6
PB[0]	PCR[16]	AF0 AF1 AF2 AF3	GPIO[16] CAN0TX — —	SIUL FlexCAN_0 — —	I/O O — —	M	Tristate	14	14	23	31	N3
PB[1]	PCR[17]	AF0 AF1 AF2 AF3 — —	GPIO[17] — — — WKUP[4] <sup>4</sup> CAN0RX	SIUL — — — WKPU FlexCAN_0	I/O — — — I I	DC Motors				24	32	N1
PB[2]	PCR[18]	AF0 AF1 AF2 AF3	GPIO[18] LIN0TX SDA —	SIUL LINFlex_0 I2C_0 —	I/O O I/O —	M	Tristate	64	64	100	144	B2
PB[3]	PCR[19]	AF0 AF1 AF2 AF3 — —	GPIO[19] — SCL — WKUP[11] <sup>4</sup> LIN0RX	SIUL — I2C_0 — WKPU LINFlex_0	I/O — I/O — I I	S	Tristate	1	1	1	1	C3
PB[4]	PCR[20]	AF0 AF1 AF2 AF3 —	GPIO[20] — — — ANP[0]	SIUL — — — ADC	I — — — I	I	Tristate	32	32	50	72	T16
PB[5]	PCR[21]	AF0 AF1 AF2 AF3 —	GPIO[21] — — — ANP[1]	SIUL — — — ADC	I — — — I	I	Tristate	35	—	53	75	R16
PB[6]	PCR[22]	AF0 AF1 AF2 AF3 —	GPIO[22] — — — ANP[2]	SIUL — — — ADC	I — — — I	I	Tristate	36	—	54	76	P15

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PB[7]	PCR[23]	AF0 AF1 AF2 AF3 —	GPIO[23] — — — ANP[3]	SIUL — — — ADC	I — — — I	I	Tristate	37	35	55	77	P16
PB[8]	PCR[24]	AF0 AF1 AF2 AF3 — —	GPIO[24] — — — — ANS[0] OSC32K_XTAL <sup>7</sup>	SIUL — — — — ADC SXOSC	I — — — — I I/O	I	Tristate	30	30	39	53	R9
PB[9]	PCR[25]	AF0 AF1 AF2 AF3 — —	GPIO[25] — — — — ANS[1] OSC32K_EXTAL <sup>7</sup>	SIUL — — — — ADC SXOSC	I — — — — I I/O	I	Tristate	29	29	38	52	T9
PB[10]	PCR[26]	AF0 AF1 AF2 AF3 — —	GPIO[26] — — — — ANS[2] WKUP[8] <sup>4</sup>	SIUL — — — — ADC WKPU	I/O — — — — I I	J	Tristate	31	31	40	54	P9
PB[11] <sup>8</sup>	PCR[27]	AF0 AF1 AF2 AF3 —	GPIO[27] E0UC[3] — CS0_0 ANS[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — I/O I	J	Tristate	38	36	59	81	N13
PB[12]	PCR[28]	AF0 AF1 AF2 AF3 —	GPIO[28] E0UC[4] — CS1_0 ANX[0]	SIUL eMIOS — DSPI_0 ADC	I/O I/O — O I	J	Tristate	39	—	61	83	M16
PB[13]	PCR[29]	AF0 AF1 AF2 AF3 —	GPIO[29] E0UC[5] — CS2_0 ANX[1]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	40	—	63	85	M13

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PB[14]	PCR[30]	AF0 AF1 AF2 AF3 —	GPIO[30] E0UC[6] — CS3_0 ANX[2]	SIUL eMIOS0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	41	37	65	87	L16
PB[15]	PCR[31]	AF0 AF1 AF2 AF3 —	GPIO[31] E0UC[7] — CS4_0 ANX[3]	SIUL eMIOS_0 — DSPI_0 ADC	I/O I/O — O I	J	Tristate	42	38	67	89	L13
PC[0] <sup>9</sup>	PCR[32]	AF0 AF1 AF2 AF3	GPIO[32] — TDI —	SIUL — JTAGC —	I/O — I —	M	Input, weak pull-up	59	59	87	126	A8
PC[1] <sup>9</sup>	PCR[33]	AF0 AF1 AF2 AF3	GPIO[33] — TDO <sup>10</sup> —	SIUL — JTAGC —	I/O — O —	M	Tristate	54	54	82	121	C9
PC[2]	PCR[34]	AF0 AF1 AF2 AF3 —	GPIO[34] SCK_1 CAN4TX <sup>11</sup> — EIRQ[5]	SIUL DSPI_1 LINFlex_4 — SIUL	I/O I/O O — I	M	Tristate	50	50	78	117	A11
PC[3]	PCR[35]	AF0 AF1 AF2 AF3 — — —	GPIO[35] CS0_1 MA[0] — CAN1RX CAN4RX <sup>11</sup> EIRQ[6]	SIUL DSPI_1 ADC — FlexCAN_1 FlexCAN_4 SIUL	I/O I/O O — I I I	S	Tristate	49	49	77	116	B11
PC[4]	PCR[36]	AF0 AF1 AF2 AF3 — —	GPIO[36] — — — SIN_1 CAN3RX <sup>11</sup>	SIUL — — — DSPI_1 FlexCAN_3	I/O — — — I I	M	Tristate	62	62	92	131	B7
PC[5]	PCR[37]	AF0 AF1 AF2 AF3 —	GPIO[37] SOUT_1 CAN3TX <sup>11</sup> — EIRQ[7]	SIUL DSPI1 FlexCAN_3 — SIUL	I/O O O — I	M	Tristate	61	61	91	130	A7



Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PC[6]	PCR[38]	AF0 AF1 AF2 AF3	GPIO[38] LIN1TX — —	SIUL LINFlex_1 — —	I/O O — —	S	Tristate	16	16	25	36	R2
PC[7]	PCR[39]	AF0 AF1 AF2 AF3 — —	GPIO[39] — — — LIN1RX WKUP[12] <sup>4</sup>	SIUL — — — LINFlex_1 WKPU	I/O — — — I I	S	Tristate	17	17	26	37	P3
PC[8]	PCR[40]	AF0 AF1 AF2 AF3	GPIO[40] LIN2TX — —	SIUL LINFlex_2 — —	I/O O — —	S	Tristate	63	63	99	143	A1
PC[9]	PCR[41]	AF0 AF1 AF2 AF3 — —	GPIO[41] — — — LIN2RX WKUP[13] <sup>4</sup>	SIUL — — — LINFlex_2 WKPU	I/O — — — I I	S	Tristate	2	2	2	2	B1
PC[10]	PCR[42]	AF0 AF1 AF2 AF3	GPIO[42] CAN1TX CAN4TX <sup>11</sup> MA[1]	SIUL FlexCAN_1 FlexCAN_4 ADC	I/O O O O	M	Tristate	13	13	22	28	M3
PC[11]	PCR[43]	AF0 AF1 AF2 AF3 — — —	GPIO[43] — — — CAN1RX CAN4RX <sup>11</sup> WKUP[5] <sup>4</sup>	SIUL — — — FlexCAN_1 FlexCAN_4 WKPU	I/O — — — I I I	S	Tristate	—	—	21	27	M4
PC[12]	PCR[44]	AF0 AF1 AF2 AF3 —	GPIO[44] E0UC[12] — — SIN_2	SIUL eMIOS_0 — — DSPI_2	I/O I/O — — I	M	Tristate	—	—	97	141	B4
PC[13]	PCR[45]	AF0 AF1 AF2 AF3	GPIO[45] E0UC[13] SOUT_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O O —	S	Tristate	—	—	98	142	A2

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PC[14]	PCR[46]	AF0 AF1 AF2 AF3 —	GPIO[46] E0UC[14] SCK_2 — EIRQ[8]	SIUL eMIOS_0 DSPI_2 — SIUL	I/O I/O I/O — I	S	Tristate	—	—	3	3	C1
PC[15]	PCR[47]	AF0 AF1 AF2 AF3	GPIO[47] E0UC[15] CS0_2 —	SIUL eMIOS_0 DSPI_2 —	I/O I/O I/O —	M	Tristate	—	—	4	4	D3
PD[0]	PCR[48]	AF0 AF1 AF2 AF3 —	GPIO[48] — — — ANP[4]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	41	63	P12
PD[1]	PCR[49]	AF0 AF1 AF2 AF3 —	GPIO[49] — — — ANP[5]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	42	64	T12
PD[2]	PCR[50]	AF0 AF1 AF2 AF3 —	GPIO[50] — — — ANP[6]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	43	65	R12
PD[3]	PCR[51]	AF0 AF1 AF2 AF3 —	GPIO[51] — — — ANP[7]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	44	66	P13
PD[4]	PCR[52]	AF0 AF1 AF2 AF3 —	GPIO[52] — — — ANP[8]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	45	67	R13
PD[5]	PCR[53]	AF0 AF1 AF2 AF3 —	GPIO[53] — — — ANP[9]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	46	68	T13

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PD[6]	PCR[54]	AF0 AF1 AF2 AF3 —	GPIO[54] — — — ANP[10]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	47	69	T14
PD[7]	PCR[55]	AF0 AF1 AF2 AF3 —	GPIO[55] — — — ANP[11]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	48	70	R14
PD[8]	PCR[56]	AF0 AF1 AF2 AF3 —	GPIO[56] — — — ANP[12]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	49	71	T15
PD[9]	PCR[57]	AF0 AF1 AF2 AF3 —	GPIO[57] — — — ANP[13]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	56	78	N15
PD[10]	PCR[58]	AF0 AF1 AF2 AF3 —	GPIO[58] — — — ANP[14]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	57	79	N14
PD[11]	PCR[59]	AF0 AF1 AF2 AF3 —	GPIO[59] — — — ANP[15]	SIUL — — — ADC	I — — — I	I	Tristate	—	—	58	80	N16
PD[12] <sup>8</sup>	PCR[60]	AF0 AF1 AF2 AF3 —	GPIO[60] CS5_0 E0UC[24] — ANS[4]	SIUL DSPI_0 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	—	60	82	M15
PD[13]	PCR[61]	AF0 AF1 AF2 AF3 —	GPIO[61] CS0_1 E0UC[25] — ANS[5]	SIUL DSPI_1 eMIOS_0 — ADC	I/O I/O I/O — I	J	Tristate	—	—	62	84	M14

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PD[14]	PCR[62]	AF0 AF1 AF2 AF3 —	GPIO[62] CS1_1 E0UC[26] — ANS[6]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	—	64	86	L15
PD[15]	PCR[63]	AF0 AF1 AF2 AF3 —	GPIO[63] CS2_1 E0UC[27] — ANS[7]	SIUL DSPI_1 eMIOS_0 — ADC	I/O O I/O — I	J	Tristate	—	—	66	88	L14
PE[0]	PCR[64]	AF0 AF1 AF2 AF3 — —	GPIO[64] E0UC[16] — — CAN5RX <sup>11</sup> WKUP[6] <sup>4</sup>	SIUL eMIOS_0 — — FlexCAN_5 WKPU	I/O I/O — — I I	S	Tristate	—	—	6	10	F1
PE[1]	PCR[65]	AF0 AF1 AF2 AF3	GPIO[65] E0UC[17] CAN5TX <sup>11</sup> —	SIUL eMIOS_0 FlexCAN_5 —	I/O I/O O —	M	Tristate	—	—	8	12	F4
PE[2]	PCR[66]	AF0 AF1 AF2 AF3 —	GPIO[66] E0UC[18] — — SIN_1	SIUL eMIOS0 — — DSPI_1	I/O I/O — — I	M	Tristate	—	—	89	128	D7
PE[3]	PCR[67]	AF0 AF1 AF2 AF3	GPIO[67] E0UC[19] SOUT_1 —	SIUL eMIOS0 DSPI_1 —	I/O I/O O —	M	Tristate	—	—	90	129	C7
PE[4]	PCR[68]	AF0 AF1 AF2 AF3 —	GPIO[68] E0UC[20] SCK_1 — EIRQ[9]	SIUL eMIOS0 DSPI_1 — SIUL	I/O I/O I/O — I	M	Tristate	—	—	93	132	D6
PE[5]	PCR[69]	AF0 AF1 AF2 AF3	GPIO[69] E0UC[21] CS0_1 MA[2]	SIUL eMIOS_0 DSPI_1 ADC	I/O I/O I/O O	M	Tristate	—	—	94	133	C6
PE[6]	PCR[70]	AF0 AF1 AF2 AF3	GPIO[70] E0UC[22] CS3_0 MA[1]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	—	—	95	139	B5

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PE[7]	PCR[71]	AF0 AF1 AF2 AF3	GPIO[71] E0UC[23] CS2_0 MA[0]	SIUL eMIOS_0 DSPI_0 ADC	I/O I/O O O	M	Tristate	—	—	96	140	C4
PE[8]	PCR[72]	AF0 AF1 AF2 AF3	GPIO[72] CAN2TX <sup>12</sup> E0UC[22] CAN3TX <sup>11</sup>	SIUL FlexCAN_2 I/O FlexCAN_3	I/O O eMIOS0 O	M	Tristate	—	—	9	13	G2
PE[9]	PCR[73]	AF0 AF1 AF2 AF3 — — —	GPIO[73] — E0UC[23] — WKUP[7] <sup>4</sup> CAN2RX <sup>12</sup> CAN3RX <sup>11</sup>	SIUL — eMIOS_0 — WKPU FlexCAN_2 FlexCAN_3	I/O — I/O — I I I	S	Tristate	—	—	10	14	G1
PE[10]	PCR[74]	AF0 AF1 AF2 AF3 —	GPIO[74] LIN3TX CS3_1 — EIRQ[10]	SIUL LINFlex_3 DSPI_1 — SIUL	I/O O O — I	S	Tristate	—	—	11	15	G3
PE[11]	PCR[75]	AF0 AF1 AF2 AF3 — —	GPIO[75] — CS4_1 — LIN3RX WKUP[14] <sup>4</sup>	SIUL — DSPI_1 — LINFlex_3 WKPU	I/O — O — I I	S	Tristate	—	—	13	17	H2
PE[12]	PCR[76]	AF0 AF1 AF2 AF3 — —	GPIO[76] — E1UC[19] <sup>13</sup> — SIN_2 EIRQ[11]	SIUL — eMIOS_1 — DSPI_2 SIUL	I/O — I/O — I I	S	Tristate	—	—	76	109	C14
PE[13]	PCR[77]	AF0 AF1 AF2 AF3	GPIO[77] SOUT2 E1UC[20] —	SIUL DSPI_2 eMIOS_1 —	I/O O I/O —	S	Tristate	—	—	—	103	D15
PE[14]	PCR[78]	AF0 AF1 AF2 AF3 —	GPIO[78] SCK_2 E1UC[21] — EIRQ[12]	SIUL DSPI_2 eMIOS_1 — SIUL	I/O I/O I/O — I	S	Tristate	—	—	—	112	C13

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PE[15]	PCR[79]	AF0 AF1 AF2 AF3	GPIO[79] CS0_2 E1UC[22] —	SIUL DSPI_2 eMIOS_1 —	I/O I/O I/O —	M	Tristate	—	—	—	113	A13
PF[0]	PCR[80]	AF0 AF1 AF2 AF3 —	GPIO[80] E0UC[10] CS3_1 — ANS[8]	SIUL eMIOS_0 DSPI_1 — ADC	I/O I/O O — I	J	Tristate	—	—	—	55	N10
PF[1]	PCR[81]	AF0 AF1 AF2 AF3 —	GPIO[81] E0UC[11] CS4_1 — ANS[9]	SIUL eMIOS_0 DSPI_1 — I	I/O I/O O — I	J	Tristate	—	—	—	56	P10
PF[2]	PCR[82]	AF0 AF1 AF2 AF3 —	GPIO[82] E0UC[12] CS0_2 — ANS[10]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O I/O — I	J	Tristate	—	—	—	57	T10
PF[3]	PCR[83]	AF0 AF1 AF2 AF3 —	GPIO[83] E0UC[13] CS1_2 — ANS[11]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	—	58	R10
PF[4]	PCR[84]	AF0 AF1 AF2 AF3 —	GPIO[84] E0UC[14] CS2_2 — ANS[12]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	—	59	N11
PF[5]	PCR[85]	AF0 AF1 AF2 AF3 —	GPIO[85] E0UC[22] CS3_2 — ANS[13]	SIUL eMIOS_0 DSPI_2 — ADC	I/O I/O O — I	J	Tristate	—	—	—	60	P11
PF[6]	PCR[86]	AF0 AF1 AF2 AF3 —	GPIO[86] E0UC[23] — — ANS[14]	SIUL eMIOS_0 — — ADC	I/O I/O — — I	J	Tristate	—	—	—	61	T11

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PF[7]	PCR[87]	AF0 AF1 AF2 AF3 —	GPIO[87] — — — ANS[15]	SIUL — — — ADC	I/O — — — I	J	Tristate	—	—	—	62	R11
PF[8]	PCR[88]	AF0 AF1 AF2 AF3	GPIO[88] CAN3TX <sup>14</sup> CS4_0 CAN2TX <sup>15</sup>	SIUL FlexCAN_3 DSPI_0 FlexCAN_2	I/O O O O	M	Tristate	—	—	—	34	P1
PF[9]	PCR[89]	AF0 AF1 AF2 AF3 — —	GPIO[89] — CS5_0 — CAN2RX <sup>15</sup> CAN3RX <sup>14</sup>	SIUL — DSPI_0 — FlexCAN_2 FlexCAN_3	I/O — O — I I	S	Tristate	—	—	—	33	N2
PF[10]	PCR[90]	AF0 AF1 AF2 AF3	GPIO[90] — — — —	SIUL — — — —	I/O — — — —	M	Tristate	—	—	—	38	R3
PF[11]	PCR[91]	AF0 AF1 AF2 AF3 —	GPIO[91] — — — WKUP[15] <sup>4</sup>	SIUL — — — WKPU	I/O — — — I	S	Tristate	—	—	—	39	R4
PF[12]	PCR[92]	AF0 AF1 AF2 AF3	GPIO[92] E1UC[25] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	35	R1
PF[13]	PCR[93]	AF0 AF1 AF2 AF3 —	GPIO[93] E1UC[26] — — WKUP[16] <sup>4</sup>	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	—	—	41	T6
PF[14]	PCR[94]	AF0 AF1 AF2 AF3	GPIO[94] CAN4TX <sup>11</sup> E1UC[27] CAN1TX	SIUL FlexCAN_4 eMIOS_1 FlexCAN_4	I/O O I/O O	M	Tristate	—	43	—	102	D14

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PF[15]	PCR[95]	AF0 AF1 AF2 AF3 — — —	GPIO[95] — — — CAN1RX CAN4RX <sup>11</sup> EIRQ[13]	SIUL — — — FlexCAN_1 FlexCAN_4 SIUL	I/O — — — I I I	S	Tristate	—	42	—	101	E15
PG[0]	PCR[96]	AF0 AF1 AF2 AF3	GPIO[96] CAN5TX <sup>11</sup> E1UC[23] —	SIUL FlexCAN_5 eMIOS_1 —	I/O O I/O —	M	Tristate	—	41	—	98	E14
PG[1]	PCR[97]	AF0 AF1 AF2 AF3 — —	GPIO[97] — E1UC[24] — CAN5RX <sup>11</sup> EIRQ[14]	SIUL — eMIOS_1 — FlexCAN_5 SIUL	I/O — I/O — I I	S	Tristate	—	40	—	97	E13
PG[2]	PCR[98]	AF0 AF1 AF2 AF3	GPIO[98] E1UC[11] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	8	E4
PG[3]	PCR[99]	AF0 AF1 AF2 AF3 —	GPIO[99] E1UC[12] — — WKUP[17] <sup>4</sup>	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	—	—	7	E3
PG[4]	PCR[100]	AF0 AF1 AF2 AF3	GPIO[100] E1UC[13] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	6	E1
PG[5]	PCR[101]	AF0 AF1 AF2 AF3 —	GPIO[101] E1UC[14] — — WKUP[18] <sup>4</sup>	SIUL eMIOS_1 — — WKPU	I/O I/O — — I	S	Tristate	—	—	—	5	E2
PG[6]	PCR[102]	AF0 AF1 AF2 AF3	GPIO[102] E1UC[15] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	30	M2



Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PG[7]	PCR[103]	AF0 AF1 AF2 AF3	GPIO[103] E1UC[16] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	29	M1
PG[8]	PCR[104]	AF0 AF1 AF2 AF3 —	GPIO[104] E1UC[17] — CS0_2 EIRQ[15]	SIUL eMIOS_1 — DSPI_2 SIUL	I/O I/O — I/O I	S	Tristate	—	—	—	26	L2
PG[9]	PCR[105]	AF0 AF1 AF2 AF3	GPIO[105] E1UC[18] — SCK_2	SIUL eMIOS1 — DSPI_2	I/O I/O — I/O	S	Tristate	—	—	—	25	L1
PG[10]	PCR[106]	AF0 AF1 AF2 AF3	GPIO[106] E0UC[24] — —	SIUL eMIOS_0 — —	I/O I/O — —	S	Tristate	—	—	—	114	D13
PG[11]	PCR[107]	AF0 AF1 AF2 AF3	GPIO[107] E0UC[25] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	—	115	B12
PG[12]	PCR[108]	AF0 AF1 AF2 AF3	GPIO[108] E0UC[26] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	—	92	K14
PG[13]	PCR[109]	AF0 AF1 AF2 AF3	GPIO[109] E0UC[27] — —	SIUL eMIOS_0 — —	I/O I/O — —	M	Tristate	—	—	—	91	K16
PG[14]	PCR[110]	AF0 AF1 AF2 AF3	GPIO[110] E1UC[0] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	—	—	110	B14
PG[15]	PCR[111]	AF0 AF1 AF2 AF3	GPIO[111] E1UC[1] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	111	B13

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PH[0]	PCR[112]	AF0 AF1 AF2 AF3 —	GPIO[112] E1UC[2] — — SIN1	SIUL eMIOS_1 — — DSPI_1	I/O I/O — — I	M	Tristate	—	—	—	93	F13
PH[1]	PCR[113]	AF0 AF1 AF2 AF3	GPIO[113] E1UC[3] SOUT1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O O —	M	Tristate	—	—	—	94	F14
PH[2]	PCR[114]	AF0 AF1 AF2 AF3	GPIO[114] E1UC[4] SCK_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	—	—	95	F16
PH[3]	PCR[115]	AF0 AF1 AF2 AF3	GPIO[115] E1UC[5] CS0_1 —	SIUL eMIOS_1 DSPI_1 —	I/O I/O I/O —	M	Tristate	—	—	—	96	F15
PH[4]	PCR[116]	AF0 AF1 AF2 AF3	GPIO[116] E1UC[6] — —	SIUL eMIOS_1 — —	I/O I/O — —	M	Tristate	—	—	—	134	A6
PH[5]	PCR[117]	AF0 AF1 AF2 AF3	GPIO[117] E1UC[7] — —	SIUL eMIOS_1 — —	I/O I/O — —	S	Tristate	—	—	—	135	B6
PH[6]	PCR[118]	AF0 AF1 AF2 AF3	GPIO[118] E1UC[8] — MA[2]	SIUL eMIOS_1 — ADC	I/O I/O — O	M	Tristate	—	—	—	136	D5
PH[7]	PCR[119]	AF0 AF1 AF2 AF3	GPIO[119] E1UC[9] CS3_2 MA[1]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	M	Tristate	—	—	—	137	C5
PH[8]	PCR[120]	AF0 AF1 AF2 AF3	GPIO[120] E1UC[10] CS2_2 MA[0]	SIUL eMIOS_1 DSPI_2 ADC	I/O I/O O O	M	Tristate	—	—	—	138	A5
PH[9] <sup>9</sup>	PCR[121]	AF0 AF1 AF2 AF3	GPIO[121] — TCK —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	—	—	88	127	B8

Table 1. Functional port pin descriptions (continued)

Port pin	PCR register	Alternate function <sup>1</sup>	Function	Peripheral	I/O direction <sup>2</sup>	Pad type	RESET config.	Pin No.				
								64 LQFP	64 LQFP 5CAN 4 LIN	100 LQFP	144 LQFP	208 MAPBGA <sup>3</sup>
PH[10] <sup>9</sup>	PCR[122]	AF0 AF1 AF2 AF3	GPIO[122] — TMS —	SIUL — JTAGC —	I/O — I —	S	Input, weak pull-up	—	—	81	120	B9

<sup>1</sup> Alternate functions are chosen by setting the values of the PCR.PA bitfields inside the SIUL module. PCR.PA = 00 -> AF0; PCR.PA = 01 -> AF1; PCR.PA = 10 -> AF2; PCR.PA = 11 -> AF3. This is intended to select the output functions; to use one of the input functions, the PCR.IBE bit must be written to '1', regardless of the values selected in the PCR.PA bitfields. For this reason, the value corresponding to an input only function is reported as "—".

<sup>2</sup> Multiple inputs are routed to all respective modules internally. The input of some modules must be configured by setting the values of the PSMIO.PADSELx bitfields inside the SIUL module.

<sup>3</sup> 208 MAPBGA available only as development package for Nexus2+

<sup>4</sup> All WKUP pins also support external interrupt capability. See wakeup unit chapter for further details.

<sup>5</sup> NMI has higher priority than alternate function. When NMI is selected, the PCR.AF field is ignored.

<sup>6</sup> "Not applicable" because these functions are available only while the device is booting. Refer to BAM chapter of the reference manual for details.

<sup>7</sup> Value of PCR.IBE bit must be 0

<sup>8</sup> This pad is used on MPC5607B 100-pin and 144-pin to provide supply for the second ADC. Therefore it is recommended not using it to keep the compatibility with the family devices.

<sup>9</sup> Out of reset all the functional pins except PC[0:1] and PH[9:10] are available to the user as GPIO.

PC[0:1] are available as JTAG pins (TDI and TDO respectively).

PH[9:10] are available as JTAG pins (TCK and TMS respectively).

It is up to the user to configure these pins as GPIO when needed, in this case MPC5604B/C get in compliance with IEEE 1149.1-2001.

<sup>10</sup> The TDO pad has been moved into the STANDBY domain in order to allow low-power debug handshaking in STANDBY mode. However, no pull-resistor is active on the TDO pad while in STANDBY mode. At this time the pad is configured as an input. When no debugger is connected the TDO pad is floating causing additional current consumption. To avoid the extra consumption TDO must be connected. An external pull-up resistor in the range of 47–100 kOhms should be added between the TDO pin and VDD. Only in case the TDO pin is used as application pin and a pull-up cannot be used then a pull-down resistor with the same value should be used between TDO pin and GND instead.

<sup>11</sup> Available only on MPC560xC versions and MPC5604B 208 MAPBGA devices

<sup>12</sup> Not available on MPC5602B devices

<sup>13</sup> Not available in 100 LQFP package

<sup>14</sup> Available only on MPC5604B 208 MAPBGA devices

<sup>15</sup> Not available on MPC5603B 144-pin devices

## 4 Electrical characteristics

### 4.1 Introduction

This section contains electrical characteristics of the device as well as temperature and power considerations.

This product contains devices to protect the inputs against damage due to high static voltages. However, it is advisable to take precautions to avoid application of any voltage higher than the specified maximum rated voltages.

To enhance reliability, unused inputs can be driven to an appropriate logic voltage level ( $V_{DD}$  or  $V_{SS}$ ). This could be done by the internal pull-up and pull-down, which is provided by the product for most general purpose pins.

The parameters listed in the following tables represent the characteristics of the device and its demands on the system.

In the tables where the device logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics is included in the Symbol column.

In the tables where the external system must provide signals with their respective timing characteristics to the device, the symbol “SR” for System Requirement is included in the Symbol column.

### CAUTION

All 64 LQFP information is indicative and must be confirmed during silicon validation.

### 4.2 Parameter classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding, the classifications listed in [Table 2](#) are used and the parameters are tagged accordingly in the tables where appropriate.

**Table 2. Parameter classifications**

Classification tag	Tag description
P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

### NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

### 4.3 NVUSRO register

Portions of the device configuration, such as high voltage supply, oscillator margin, and watchdog enable/disable after reset are controlled via bit values in the Non-Volatile User Options Register (NVUSRO) register.

### 4.3.1 NVUSRO[PAD3V5V] field description

Table 3 shows how NVUSRO[PAD3V5V] controls the device configuration.

**Table 3. PAD3V5V field description<sup>1</sup>**

Value <sup>2</sup>	Description
0	High voltage supply is 5.0 V
1	High voltage supply is 3.3 V

<sup>1</sup> See the device reference manual for more information on the NVUSRO register.

<sup>2</sup> '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

The DC electrical characteristics are dependent on the PAD3V5V bit value.

### 4.3.2 NVUSRO[OSCILLATOR\_MARGIN] field description

Table 4 shows how NVUSRO[OSCILLATOR\_MARGIN] controls the device configuration.

**Table 4. OSCILLATOR\_MARGIN field description<sup>1</sup>**

Value <sup>2</sup>	Description
0	Low consumption configuration (4 MHz/8 MHz)
1	High margin configuration (4 MHz/16 MHz)

<sup>1</sup> See the device reference manual for more information on the NVUSRO register.

<sup>2</sup> '1' is delivery value. It is part of shadow Flash, thus programmable by customer.

The fast external crystal oscillator consumption is dependent on the OSCILLATOR\_MARGIN bit value.

For a detailed description of the NVUSRO register, please refer to the MPC5604B/C Reference Manual.

## 4.4 Absolute maximum ratings

Table 5. Absolute maximum ratings

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
V <sub>SS</sub>	SR	Digital ground on VSS_HV pins	—	0	0	V
V <sub>DD</sub>	SR	Voltage on VDD_HV pins with respect to ground (V <sub>SS</sub> )	—	−0.3	6.0	V
V <sub>SS_LV</sub>	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground (V <sub>SS</sub> )	—	V <sub>SS</sub> −0.1	V <sub>SS</sub> +0.1	V
V <sub>DD_BV</sub>	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground (V <sub>SS</sub> )	—	−0.3	6.0	V
			Relative to V <sub>DD</sub>	−0.3	V <sub>DD</sub> +0.3	
V <sub>SS_ADC</sub>	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V <sub>SS</sub> )	—	V <sub>SS</sub> −0.1	V <sub>SS</sub> +0.1	V
V <sub>DD_ADC</sub>	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V <sub>SS</sub> )	—	−0.3	6.0	V
			Relative to V <sub>DD</sub>	V <sub>DD</sub> −0.3	V <sub>DD</sub> +0.3	
V <sub>IN</sub>	SR	Voltage on any GPIO pin with respect to ground (V <sub>SS</sub> )	—	−0.3	6.0	V
			Relative to V <sub>DD</sub>	—	V <sub>DD</sub> +0.3	
I <sub>INPAD</sub>	SR	Injected input current on any pin during overload condition	—	−10	10	mA
I <sub>INJSUM</sub>	SR	Absolute sum of all injected input currents during overload condition	—	−50	50	
I <sub>AVGSEG</sub>	SR	Sum of all the static I/O current within a supply segment	V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	—	70	mA
			V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1	—	64	
I <sub>CORELV</sub>	SR	Low voltage static current sink through VDD_BV	—	—	150	mA
T <sub>STORAGE</sub>	SR	Storage temperature	—	−55	150	°C

### NOTE

Stresses exceeding the recommended absolute maximum ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ( $V_{IN} > V_{DD}$  or  $V_{IN} < V_{SS}$ ), the voltage on pins with respect to ground (V<sub>SS</sub>) must not exceed the recommended values.

## 4.5 Recommended operating conditions

Table 6. Recommended operating conditions (3.3 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$V_{SS}$	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD}^1$	SR	Voltage on VDD_HV pins with respect to ground ( $V_{SS}$ )	—	3.0	3.6	V
$V_{SS\_LV}^2$	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground ( $V_{SS}$ )	—	$V_{SS}-0.1$	$V_{SS}+0.1$	V
$V_{DD\_BV}^3$	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground ( $V_{SS}$ )	—	3.0	3.6	V
			Relative to $V_{DD}$	$V_{DD}-0.1$	$V_{DD}+0.1$	
$V_{SS\_ADC}$	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground ( $V_{SS}$ )	—	$V_{SS}-0.1$	$V_{SS}+0.1$	V
$V_{DD\_ADC}^4$	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground ( $V_{SS}$ )	—	3.0 <sup>5</sup>	3.6	V
			Relative to $V_{DD}$	$V_{DD}-0.1$	$V_{DD}+0.1$	
$V_{IN}$	SR	Voltage on any GPIO pin with respect to ground ( $V_{SS}$ )	—	$V_{SS}-0.1$	—	V
			Relative to $V_{DD}$	—	$V_{DD}+0.1$	
$I_{INJPAD}$	SR	Injected input current on any pin during overload condition	—	-5	5	mA
$I_{INJSUM}$	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
$TV_{DD}$	SR	$V_{DD}$ slope to ensure correct power up <sup>6</sup>	—	—	0.25	V/ $\mu$ s
$T_A$ C-Grade Part	SR	Ambient temperature under bias	—	-40	85	°C
$T_J$ C-Grade Part	SR	Junction temperature under bias	—	-40	110	
$T_A$ V-Grade Part	SR	Ambient temperature under bias	—	-40	105	
$T_J$ V-Grade Part	SR	Junction temperature under bias	—	-40	130	
$T_A$ M-Grade Part	SR	Ambient temperature under bias	—	-40	125	
$T_J$ M-Grade Part	SR	Junction temperature under bias	—	-40	150	

<sup>1</sup> 100 nF capacitance needs to be provided between each  $V_{DD}/V_{SS}$  pair

<sup>2</sup> 330 nF capacitance needs to be provided between each  $V_{DD\_LV}/V_{SS\_LV}$  supply pair.

<sup>3</sup> 400 nF capacitance needs to be provided between  $V_{DD\_BV}$  and the nearest  $V_{SS\_LV}$  (higher value may be needed depending on external regulator characteristics).

<sup>4</sup> 100 nF capacitance needs to be provided between  $V_{DD\_ADC}/V_{SS\_ADC}$  pair.

<sup>5</sup> Full electrical specification cannot be guaranteed when voltage drops below 3.0 V. In particular, ADC electrical characteristics and I/Os DC electrical specification may not be guaranteed. When voltage drops below  $V_{LVDHVL}$ , device is reset.

<sup>6</sup> Guaranteed by device validation

Table 7. Recommended operating conditions (5.0 V)

Symbol		Parameter	Conditions	Value		Unit
				Min	Max	
$V_{SS}$	SR	Digital ground on VSS_HV pins	—	0	0	V
$V_{DD}^1$	SR	Voltage on VDD_HV pins with respect to ground ( $V_{SS}$ )	—	4.5	5.5	V
		Voltage drop <sup>2</sup>		3.0	5.5	
$V_{SS\_LV}^3$	SR	Voltage on VSS_LV (low voltage digital supply) pins with respect to ground ( $V_{SS}$ )	—	$V_{SS}-0.1$	$V_{SS}+0.1$	V
$V_{DD\_BV}^4$	SR	Voltage on VDD_BV pin (regulator supply) with respect to ground ( $V_{SS}$ )	—	4.5	5.5	V
		Voltage drop <sup>2</sup>		3.0	5.5	
		Relative to $V_{DD}$		$V_{DD}-0.1$	$V_{DD}+0.1$	
$V_{SS\_ADC}$	SR	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground ( $V_{SS}$ )	—	$V_{SS}-0.1$	$V_{SS}+0.1$	V
$V_{DD\_ADC}^5$	SR	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground ( $V_{SS}$ )	—	4.5	5.5	V
		Voltage drop <sup>2</sup>		3.0	5.5	
		Relative to $V_{DD}$		$V_{DD}-0.1$	$V_{DD}+0.1$	
$V_{IN}$	SR	Voltage on any GPIO pin with respect to ground ( $V_{SS}$ )	—	$V_{SS}-0.1$	—	V
		Relative to $V_{DD}$		—	$V_{DD}+0.1$	
$I_{INJPAD}$	SR	Injected input current on any pin during overload condition	—	-5	5	mA
$I_{INJSUM}$	SR	Absolute sum of all injected input currents during overload condition	—	-50	50	
$TV_{DD}$	SR	$V_{DD}$ slope to ensure correct power up <sup>6</sup>	—	—	0.25	V/ $\mu$ s
$T_A$ C-Grade Part	SR	Ambient temperature under bias	—	-40	85	°C
$T_J$ C-Grade Part	SR	Junction temperature under bias	—	-40	110	
$T_A$ V-Grade Part	SR	Ambient temperature under bias	—	-40	105	
$T_J$ V-Grade Part	SR	Junction temperature under bias	—	-40	130	
$T_A$ M-Grade Part	SR	Ambient temperature under bias	—	-40	125	
$T_J$ M-Grade Part	SR	Junction temperature under bias	—	-40	150	

<sup>1</sup> 100 nF capacitance needs to be provided between each  $V_{DD}/V_{SS}$  pair.

<sup>2</sup> Full device operation is guaranteed by design when the voltage drops below 4.5 V down to 3.0 V. However, certain analog electrical characteristics will not be guaranteed to stay within the stated limits.

<sup>3</sup> 330 nF capacitance needs to be provided between each  $V_{DD\_LV}/V_{SS\_LV}$  supply pair.

<sup>4</sup> 100 nF capacitance needs to be provided between  $V_{DD\_BV}$  and the nearest  $V_{SS\_LV}$  (higher value may be needed depending on external regulator characteristics).

<sup>5</sup> 100 nF capacitance needs to be provided between  $V_{DD\_ADC}/V_{SS\_ADC}$  pair.

<sup>6</sup> Guaranteed by device validation



**NOTE**

RAM data retention is guaranteed with  $V_{DD\_LV}$  not below 1.08 V.

**4.6 Thermal characteristics****4.6.1 Package thermal characteristics****Table 8. LQFP thermal characteristics<sup>1</sup>**

Symbol		C	Parameter	Conditions <sup>2</sup>	Pin count	Value	Unit
$R_{\theta JA}$	CC	D	Thermal resistance, junction-to-ambient natural convection <sup>3</sup>	Single-layer board - 1s	64	TBD	°C/W
					100	64	
					144	64	
				Four-layer board - 2s2p	64	TBD	
					100	51	
					144	49	
$R_{\theta JB}$	CC	D	Thermal resistance, junction-to-board <sup>4</sup>	Single-layer board - 1s	64	TBD	°C/W
					100	36	
					144	37	
				Four-layer board - 2s2p	64	TBD	
					100	34	
					144	35	
$R_{\theta JC}$	CC	D	Thermal resistance, junction-to-case <sup>5</sup>	Single-layer board - 1s	64	TBD	°C/W
					100	22	
					144	22	
				Four-layer board - 2s2p	64	TBD	
					100	22	
					144	22	
$\Psi_{JB}$	CC	D	Junction-to-board thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	33	
					144	34	
				Four-layer board - 2s2p	64	TBD	
					100	34	
					144	35	

Table 8. LQFP thermal characteristics<sup>1</sup> (continued)

Symbol		C	Parameter	Conditions <sup>2</sup>	Pin count	Value	Unit
$\Psi_{JC}$	CC	D	Junction-to-case thermal characterization parameter, natural convection	Single-layer board - 1s	64	TBD	°C/W
					100	9	
					144	10	
				Four-layer board - 2s2p	64	TBD	
					100	9	
					144	10	

<sup>1</sup> Thermal characteristics are based on simulation.

<sup>2</sup>  $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125\text{ }^{\circ}\text{C}$

<sup>3</sup> Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESD51-6. Thermal test board meets JEDEC specification for this package. When Greek letters are not available, the symbols are typed as  $R_{thJA}$  and  $R_{thJMA}$ .

<sup>4</sup> Junction-to-board thermal resistance determined per JEDEC JESD51-8. Thermal test board meets JEDEC specification for the specified package. When Greek letters are not available, the symbols are typed as  $R_{thJB}$ .

<sup>5</sup> Junction-to-case at the top of the package determined using MIL-STD 883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer. When Greek letters are not available, the symbols are typed as  $R_{thJC}$ .

## 4.6.2 Power considerations

The average chip-junction temperature,  $T_J$ , in degrees Celsius, may be calculated using Equation 1:

$$T_J = T_A + (P_D \times R_{\theta JA}) \quad \text{Eqn. 1}$$

Where:

$T_A$  is the ambient temperature in °C.

$R_{\theta JA}$  is the package junction-to-ambient thermal resistance, in °C/W.

$P_D$  is the sum of  $P_{INT}$  and  $P_{I/O}$  ( $P_D = P_{INT} + P_{I/O}$ ).

$P_{INT}$  is the product of  $I_{DD}$  and  $V_{DD}$ , expressed in watts. This is the chip internal power.

$P_{I/O}$  represents the power dissipation on input and output pins; user determined.

Most of the time for the applications,  $P_{I/O} < P_{INT}$  and may be neglected. On the other hand,  $P_{I/O}$  may be significant, if the device is configured to continuously drive external modules and/or memories.

An approximate relationship between  $P_D$  and  $T_J$  (if  $P_{I/O}$  is neglected) is given by:

$$P_D = K / (T_J + 273 \text{ °C}) \quad \text{Eqn. 2}$$

Therefore, solving equations 1 and 2:

$$K = P_D \times (T_A + 273 \text{ °C}) + R_{\theta JA} \times P_D^2 \quad \text{Eqn. 3}$$

Where:

$K$  is a constant for the particular part, which may be determined from Equation 3 by measuring  $P_D$  (at equilibrium) for a known  $T_A$ . Using this value of  $K$ , the values of  $P_D$  and  $T_J$  may be obtained by solving equations 1 and 2 iteratively for any value of  $T_A$ .

## 4.7 I/O pad electrical characteristics

### 4.7.1 I/O pad types

The device provides four main I/O pad types depending on the associated alternate functions:

- Slow pads—These pads are the most common pads, providing a good compromise between transition time and low electromagnetic emission.
- Medium pads—These pads provide transition fast enough for the serial communication channels with controlled current to reduce electromagnetic emission.
- Fast pads—These pads provide maximum speed. There are used for improved Nexus debugging capability.
- Input only pads—These pads are associated to ADC channels and the external 32 kHz crystal oscillator (SXOSC) providing low input leakage.

Medium and Fast pads can use slow configuration to reduce electromagnetic emission, at the cost of reducing AC performance.

## 4.7.2 I/O input DC characteristics

Table 9 provides input DC electrical characteristics as described in Figure 7.

Figure 7. I/O input DC electrical characteristics definition

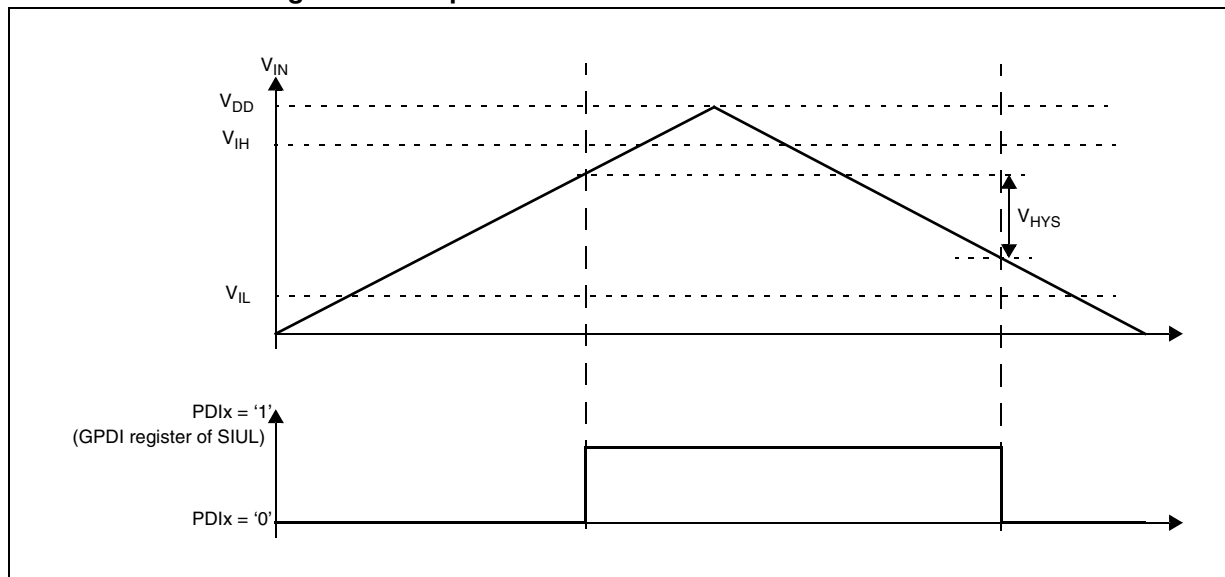


Table 9. I/O input DC electrical characteristics

Symbol		C	Parameter	Conditions <sup>1</sup>		Value			Unit
						Min	Typ	Max	
V <sub>IH</sub>	SR	P	Input high level CMOS (Schmitt Trigger)	—		0.65V <sub>DD</sub>	—	V <sub>DD</sub> +0.4	V
V <sub>IL</sub>	SR	P	Input low level CMOS (Schmitt Trigger)	—		−0.4	—	0.35V <sub>DD</sub>	V
V <sub>HYS</sub>	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—		0.1V <sub>DD</sub>	—	—	V
I <sub>LKG</sub>	CC	P	Digital input leakage	No injection on adjacent pin	T <sub>A</sub> = −40 °C	—	2	—	nA
		T <sub>A</sub> = 25 °C			—	2	—		
		T <sub>A</sub> = 105 °C			—	12	500		
		T <sub>A</sub> = 125 °C			—	70	1000		
W <sub>FI</sub> <sup>2</sup>	SR	P	Wakeup input filtered pulse	—		—	—	40	ns
W <sub>NFI</sub> <sup>2</sup>	SR	P	Wakeup input not filtered pulse	—		1000	—	—	ns

<sup>1</sup>  $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified

<sup>2</sup> In the range from 40 to 1000 ns, pulses can be filtered or not filtered, according to operating temperature and voltage.

### 4.7.3 I/O output DC characteristics

The following tables provide DC characteristics for bidirectional pads:

- Table 10 provides weak pull figures. Both pull-up and pull-down resistances are supported.
- Table 11 provides output driver characteristics for I/O pads when in SLOW configuration.
- Table 12 provides output driver characteristics for I/O pads when in MEDIUM configuration.
- Table 13 provides output driver characteristics for I/O pads when in FAST configuration.

**Table 10. I/O pull-up/pull-down DC electrical characteristics**

Symbol		C	Parameter	Conditions <sup>1</sup>		Value			Unit
						Min	Typ	Max	
I <sub>WPU</sub>	CC	P	Weak pull-up current absolute value	V <sub>IN</sub> = V <sub>IL</sub> , V <sub>DD</sub> = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	μA
		PAD3V5V = 1 <sup>2</sup>			10	—	250		
		P		V <sub>IN</sub> = V <sub>IL</sub> , V <sub>DD</sub> = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	
I <sub>WPD</sub>	CC	P	Weak pull-down current absolute value	V <sub>IN</sub> = V <sub>IH</sub> , V <sub>DD</sub> = 5.0 V ± 10%	PAD3V5V = 0	10	—	150	μA
		PAD3V5V = 1			10	—	250		
		P		V <sub>IN</sub> = V <sub>IH</sub> , V <sub>DD</sub> = 3.3 V ± 10%	PAD3V5V = 1	10	—	150	

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified.

<sup>2</sup> The configuration PAD3V5 = 1 when V<sub>DD</sub> = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

**Table 11. SLOW configuration output buffer electrical characteristics**

Symbol		C	Parameter	Conditions <sup>1</sup>		Value			Unit
						Min	Typ	Max	
V <sub>OH</sub>	CC	P	Output high level SLOW configuration	Push Pull	I <sub>OH</sub> = −2 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V <sub>DD</sub>	—	—	V
		I <sub>OH</sub> = −2 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 1 <sup>2</sup>			0.8V <sub>DD</sub>	—	—		
		I <sub>OH</sub> = −1 mA, V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 (recommended)			V <sub>DD</sub> −0.8	—	—		
V <sub>OL</sub>	CC	P	Output low level SLOW configuration	Push Pull	I <sub>OL</sub> = 2 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V <sub>DD</sub>	V
		I <sub>OL</sub> = 2 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 1 <sup>2</sup>			—	—	0.1V <sub>DD</sub>		
		I <sub>OL</sub> = 1 mA, V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 (recommended)			—	—	0.5		

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> The configuration PAD3V5 = 1 when V<sub>DD</sub> = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 12. MEDIUM configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions <sup>1</sup>	Value			Unit
				Min	Typ	Max	
V <sub>OH</sub>	CC	Output high level MEDIUM configuration	Push Pull	I <sub>OH</sub> = -3.8 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	0.8V <sub>DD</sub>	—	V
				I <sub>OH</sub> = -2 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V <sub>DD</sub>	—	
				I <sub>OH</sub> = -1 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 1 <sup>2</sup>	0.8V <sub>DD</sub>	—	
				I <sub>OH</sub> = -1 mA, V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V <sub>DD</sub> -0.8	—	
				I <sub>OH</sub> = -100 μA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	0.8V <sub>DD</sub>	—	
V <sub>OL</sub>	CC	Output low level MEDIUM configuration	Push Pull	I <sub>OL</sub> = 3.8 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	—	—	V
				I <sub>OL</sub> = 2 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.2V <sub>DD</sub>
				I <sub>OL</sub> = 1 mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 1 <sup>2</sup>	—	—	0.1V <sub>DD</sub>
				I <sub>OL</sub> = 1 mA, V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5
				I <sub>OH</sub> = 100 μA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	—	—	0.1V <sub>DD</sub>

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> The configuration PAD3V5 = 1 when V<sub>DD</sub> = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

Table 13. FAST configuration output buffer electrical characteristics

Symbol	C	Parameter	Conditions <sup>1</sup>	Value			Unit
				Min	Typ	Max	
V <sub>OH</sub>	CC	Output high level FAST configuration	Push Pull	I <sub>OH</sub> = -14mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	0.8V <sub>DD</sub>	—	V
				I <sub>OH</sub> = -7mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 1 <sup>2</sup>	0.8V <sub>DD</sub>	—	
				I <sub>OH</sub> = -11mA, V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	V <sub>DD</sub> -0.8	—	

Table 13. FAST configuration output buffer electrical characteristics (continued)

Symbol		C	Parameter	Conditions <sup>1</sup>		Value			Unit
						Min	Typ	Max	
V <sub>OL</sub>	CC	P	Output low level FAST configuration	Push Pull	I <sub>OL</sub> = 14mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 (recommended)	—	—	0.1V <sub>DD</sub>	V
		C			I <sub>OL</sub> = 7mA, V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 1 <sup>2</sup>	—	—	0.1V <sub>DD</sub>	
		C			I <sub>OL</sub> = 11mA, V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 (recommended)	—	—	0.5	

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> The configuration PAD3V5 = 1 when V<sub>DD</sub> = 5 V is only a transient configuration during power-up. All pads but RESET and Nexus output (MDOx, EVTO, MCKO) are configured in input or in high impedance state.

## 4.7.4 Output pin transition times

Table 14. Output pin transition times

Symbol		C	Parameter	Conditions <sup>1</sup>		Value			Unit
						Min	Typ	Max	
T <sub>tr</sub>	CC	D	Output transition time output pin <sup>2</sup> SLOW configuration	C <sub>L</sub> = 25 pF	V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	—	—	50	ns
		T		C <sub>L</sub> = 50 pF		—	—	100	
		D		C <sub>L</sub> = 100 pF		—	—	125	
		D		C <sub>L</sub> = 25 pF	V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1	—	—	50	
		T		C <sub>L</sub> = 50 pF		—	—	100	
		D		C <sub>L</sub> = 100 pF		—	—	125	
T <sub>tr</sub>	CC	D	Output transition time output pin <sup>2</sup> MEDIUM configuration	C <sub>L</sub> = 25 pF	V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 SIUL.PCRx.SRC = 1	—	—	10	ns
		T		C <sub>L</sub> = 50 pF		—	—	20	
		D		C <sub>L</sub> = 100 pF		—	—	40	
		D		C <sub>L</sub> = 25 pF	V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 SIUL.PCRx.SRC = 1	—	—	12	
		T		C <sub>L</sub> = 50 pF		—	—	25	
		D		C <sub>L</sub> = 100 pF		—	—	40	
T <sub>tr</sub>	CC	D	Output transition time output pin <sup>2</sup> FAST configuration	C <sub>L</sub> = 25 pF	V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	—	—	4	ns
		C <sub>L</sub> = 50 pF		—		—	6		
		C <sub>L</sub> = 100 pF		—		—	12		
		C <sub>L</sub> = 25 pF		V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1	—	—	4		
		C <sub>L</sub> = 50 pF			—	—	7		
		C <sub>L</sub> = 100 pF			—	—	12		

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

## Electrical characteristics

<sup>2</sup>  $C_L$  includes device and package capacitances ( $C_{PKG} < 5$  pF).

### 4.7.5 I/O pad current specification

The I/O pads are distributed across the I/O supply segment. Each I/O supply segment is associated to a  $V_{DD}/V_{SS}$  supply pair as described in Table 15.

Table 16 provides I/O consumption figures.

In order to ensure device reliability, the average current of the I/O on a single segment should remain below the  $I_{AVGSEG}$  maximum value.

In order to ensure device functionality, the sum of the dynamic and static current of the I/O on a single segment should remain below the  $I_{DYNSEG}$  maximum value.

**Table 15. I/O supply segment**

Package	Supply segment					
	1	2	3	4	5	6
208 MAPBGA <sup>1</sup>	Equivalent to 144 LQFP segment pad distribution				MCKO	MDO <sub>n</sub> /MSEO
144 LQFP	pin20–pin49	pin51–pin99	pin100–pin122	pin 123–pin19	—	—
100 LQFP	pin16–pin35	pin37–pin69	pin70–pin83	pin 84–pin15	—	—
64 LQFP <sup>2</sup>	pin8–pin26	pin28–pin55	pin56–pin7	—	—	—

<sup>1</sup> 208 MAPBGA available only as development package for Nexus2+

<sup>2</sup> All 64 LQFP information is indicative and must be confirmed during silicon validation.

**Table 16. I/O consumption**

Symbol	C	D	Parameter	Conditions <sup>1</sup>		Value			Unit
						Min	Typ	Max	
$I_{SWTSLW}$ <sup>2</sup>	CC	D	Dynamic I/O current for SLOW configuration	$C_L = 25$ pF	$V_{DD} = 5.0$ V $\pm$ 10%, PAD3V5V = 0	—	—	20	mA
					$V_{DD} = 3.3$ V $\pm$ 10%, PAD3V5V = 1	—	—	16	
$I_{SWTMED}$ <sup>2</sup>	CC	D	Dynamic I/O current for MEDIUM configuration	$C_L = 25$ pF	$V_{DD} = 5.0$ V $\pm$ 10%, PAD3V5V = 0	—	—	29	mA
					$V_{DD} = 3.3$ V $\pm$ 10%, PAD3V5V = 1	—	—	17	
$I_{SWTFST}$ <sup>2</sup>	CC	D	Dynamic I/O current for FAST configuration	$C_L = 25$ pF	$V_{DD} = 5.0$ V $\pm$ 10%, PAD3V5V = 0	—	—	110	mA
					$V_{DD} = 3.3$ V $\pm$ 10%, PAD3V5V = 1	—	—	50	



Table 16. I/O consumption (continued)

Symbol		C	Parameter	Conditions <sup>1</sup>		Value			Unit
						Min	Typ	Max	
I <sub>RMSSLW</sub>	CC	D	Root medium square I/O current for SLOW configuration	C <sub>L</sub> = 25 pF, 2 MHz	V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	—	—	2.3	mA
				C <sub>L</sub> = 25 pF, 4 MHz		—	—	3.2	
				C <sub>L</sub> = 100 pF, 2 MHz		—	—	6.6	
				C <sub>L</sub> = 25 pF, 2 MHz	V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1	—	—	1.6	
				C <sub>L</sub> = 25 pF, 4 MHz		—	—	2.3	
				C <sub>L</sub> = 100 pF, 2 MHz		—	—	4.7	
I <sub>RMSMED</sub>	CC	D	Root medium square I/O current for MEDIUM configuration	C <sub>L</sub> = 25 pF, 13 MHz	V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	—	—	6.6	mA
				C <sub>L</sub> = 25 pF, 40 MHz		—	—	13.4	
				C <sub>L</sub> = 100 pF, 13 MHz		—	—	18.3	
				C <sub>L</sub> = 25 pF, 13 MHz	V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1	—	—	5	
				C <sub>L</sub> = 25 pF, 40 MHz		—	—	8.5	
				C <sub>L</sub> = 100 pF, 13 MHz		—	—	11	
I <sub>RMSFST</sub>	CC	D	Root medium square I/O current for FAST configuration	C <sub>L</sub> = 25 pF, 40 MHz	V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0	—	—	22	mA
				C <sub>L</sub> = 25 pF, 64 MHz		—	—	33	
				C <sub>L</sub> = 100 pF, 40 MHz		—	—	56	
				C <sub>L</sub> = 25 pF, 40 MHz	V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1	—	—	14	
				C <sub>L</sub> = 25 pF, 64 MHz		—	—	20	
				C <sub>L</sub> = 100 pF, 40 MHz		—	—	35	
I <sub>AVGSEG</sub>	SR	D	Sum of all the static I/O current within a supply segment	V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0		—	—	70	mA
				V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1		—	—	65	

<sup>1</sup>  $V_{\text{DD}} = 3.3 \text{ V} \pm 10\%$  /  $5.0 \text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125^\circ\text{C}$ , unless otherwise specified

<sup>2</sup> Stated maximum values represent peak consumption that lasts only a few ns during I/O transition.

Table 17 provides the weight of concurrent switching I/Os.

In order to ensure device functionality, the sum of the weight of concurrent switching I/Os on a single segment should remain below the 100%.

Table 17. I/O weight<sup>1</sup>

PAD	144/100 LQFP				64 LQFP <sup>2</sup>			
	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1
PB[3]	10%	—	12%	—	10%	—	12%	—
PC[9]	10%	—	12%	—	10%	—	12%	—
PC[14]	9%	—	11%	—	9%	—	11%	—
PC[15]	9%	13%	11%	12%	9%	13%	11%	12%

Table 17. I/O weight<sup>1</sup>

PAD	144/100 LQFP				64 LQFP <sup>2</sup>			
	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1
PG[5]	9%	—	11%	—	9%	—	11%	—
PG[4]	9%	12%	10%	11%	9%	12%	10%	11%
PG[3]	9%	—	10%	—	9%	—	10%	—
PG[2]	8%	12%	10%	10%	8%	12%	10%	10%
PA[2]	8%	—	9%	—	8%	—	9%	—
PE[0]	8%	—	9%	—	8%	—	9%	—
PA[1]	7%	—	9%	—	7%	—	9%	—
PE[1]	7%	10%	8%	9%	7%	10%	8%	9%
PE[8]	7%	9%	8%	8%	7%	9%	8%	8%
PE[9]	6%	—	7%	—	6%	—	7%	—
PE[10]	6%	—	7%	—	6%	—	7%	—
PA[0]	5%	8%	6%	7%	5%	8%	6%	7%
PE[11]	5%	—	6%	—	5%	—	6%	—
PG[9]	9%	—	10%	—	9%	—	10%	—
PG[8]	9%	—	11%	—	9%	—	11%	—
PC[11]	9%	—	11%	—	9%	—	11%	—
PC[10]	9%	13%	11%	12%	9%	13%	11%	12%
PG[7]	10%	14%	11%	12%	10%	14%	11%	12%
PG[6]	10%	14%	12%	12%	10%	14%	12%	12%
PB[0]	10%	14%	12%	12%	10%	14%	12%	12%
PB[1]	10%	—	12%	—	10%	—	12%	—
PF[9]	10%	—	12%	—	10%	—	12%	—
PF[8]	10%	15%	12%	13%	10%	15%	12%	13%
PF[12]	10%	15%	12%	13%	10%	15%	12%	13%
PC[6]	10%	—	12%	—	10%	—	12%	—
PC[7]	10%	—	12%	—	10%	—	12%	—
PF[10]	10%	14%	12%	12%	10%	14%	12%	12%
PF[11]	10%	—	11%	—	10%	—	11%	—
PA[15]	9%	12%	10%	11%	9%	12%	10%	11%
PF[13]	8%	—	10%	—	8%	—	10%	—
PA[14]	8%	11%	9%	10%	8%	11%	9%	10%
PA[4]	8%	—	9%	—	8%	—	9%	—
PA[13]	7%	10%	9%	9%	7%	10%	9%	9%

Table 17. I/O weight<sup>1</sup>

PAD	144/100 LQFP				64 LQFP <sup>2</sup>			
	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1
PA[12]	7%	—	8%	—	7%	—	8%	—
PB[9]	1%	—	1%	—	1%	—	1%	—
PB[8]	1%	—	1%	—	1%	—	1%	—
PB[10]	6%	—	7%	—	6%	—	7%	—
PF[0]	6%	—	7%	—	6%	—	7%	—
PF[1]	7%	—	8%	—	7%	—	8%	—
PF[2]	7%	—	8%	—	7%	—	8%	—
PF[3]	7%	—	9%	—	8%	—	9%	—
PF[4]	8%	—	9%	—	8%	—	9%	—
PF[5]	8%	—	10%	—	8%	—	10%	—
PF[6]	8%	—	10%	—	9%	—	10%	—
PF[7]	9%	—	10%	—	9%	—	11%	—
PD[0]	1%	—	1%	—	1%	—	1%	—
PD[1]	1%	—	1%	—	1%	—	1%	—
PD[2]	1%	—	1%	—	1%	—	1%	—
PD[3]	1%	—	1%	—	1%	—	1%	—
PD[4]	1%	—	1%	—	1%	—	1%	—
PD[5]	1%	—	1%	—	1%	—	1%	—
PD[6]	1%	—	1%	—	1%	—	1%	—
PD[7]	1%	—	1%	—	1%	—	1%	—
PD[8]	1%	—	1%	—	1%	—	1%	—
PB[4]	1%	—	1%	—	1%	—	1%	—
PB[5]	1%	—	1%	—	1%	—	2%	—
PB[6]	1%	—	1%	—	1%	—	2%	—
PB[7]	1%	—	1%	—	1%	—	2%	—
PD[9]	1%	—	1%	—	1%	—	2%	—
PD[10]	1%	—	1%	—	1%	—	2%	—
PD[11]	1%	—	1%	—	1%	—	2%	—
PB[11]	11%	—	13%	—	17%	—	21%	—
PD[12]	11%	—	13%	—	18%	—	21%	—
PB[12]	11%	—	13%	—	18%	—	21%	—
PD[13]	10%	—	12%	—	18%	—	21%	—
PB[13]	10%	—	12%	—	18%	—	21%	—

Table 17. I/O weight<sup>1</sup>

PAD	144/100 LQFP				64 LQFP <sup>2</sup>			
	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1
PD[14]	10%	—	12%	—	18%	—	21%	—
PB[14]	10%	—	12%	—	18%	—	21%	—
PD[15]	10%	—	11%	—	18%	—	21%	—
PB[15]	9%	—	11%	—	18%	—	21%	—
PA[3]	9%	—	11%	—	18%	—	21%	—
PG[13]	9%	13%	10%	11%	18%	26%	21%	23%
PG[12]	9%	12%	10%	11%	18%	26%	21%	23%
PH[0]	5%	8%	6%	7%	18%	26%	21%	23%
PH[1]	5%	7%	6%	6%	18%	26%	21%	23%
PH[2]	5%	6%	5%	6%	18%	25%	21%	22%
PH[3]	4%	6%	5%	5%	18%	25%	21%	22%
PG[1]	4%	—	4%	—	18%	—	21%	—
PG[0]	3%	4%	4%	4%	17%	25%	21%	22%
PF[15]	3%	—	4%	—	17%	—	20%	—
PF[14]	4%	5%	5%	5%	16%	23%	20%	21%
PE[13]	4%	—	5%	—	16%	—	19%	—
PA[7]	5%	—	6%	—	16%	—	19%	—
PA[8]	5%	—	6%	—	16%	—	19%	—
PA[9]	5%	—	6%	—	15%	—	18%	—
PA[10]	6%	—	7%	—	15%	—	18%	—
PA[11]	6%	—	8%	—	14%	—	17%	—
PE[12]	7%	—	8%	—	11%	—	14%	—
PG[14]	7%	—	8%	—	10%	—	12%	—
PG[15]	7%	10%	8%	9%	10%	14%	12%	12%
PE[14]	7%	—	8%	—	9%	—	11%	—
PE[15]	7%	9%	8%	8%	9%	12%	10%	11%
PG[10]	6%	—	8%	—	8%	—	10%	—
PG[11]	6%	9%	7%	8%	8%	11%	9%	10%
PC[3]	6%	—	7%	—	7%	—	9%	—
PC[2]	6%	8%	7%	7%	6%	9%	8%	8%
PA[5]	5%	7%	6%	6%	6%	8%	7%	7%
PA[6]	5%	—	6%	—	5%	—	6%	—
PC[1]	5%	—	5%	—	5%	—	5%	—

Table 17. I/O weight<sup>1</sup>

PAD	144/100 LQFP				64 LQFP <sup>2</sup>			
	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1	Weight 5V SRE=0	Weight 5V SRE=1	Weight 3.3V SRE=0	Weight 3.3V SRE=1
PC[0]	6%	9%	7%	8%	6%	9%	7%	8%
PE[2]	7%	10%	9%	9%	7%	10%	9%	9%
PE[3]	8%	11%	9%	9%	8%	11%	9%	9%
PC[5]	8%	11%	9%	10%	8%	11%	9%	10%
PC[4]	8%	12%	10%	10%	8%	12%	10%	10%
PE[4]	8%	12%	10%	11%	8%	12%	10%	11%
PE[5]	9%	12%	10%	11%	9%	12%	10%	11%
PH[4]	9%	13%	11%	11%	9%	13%	11%	11%
PH[5]	9%	—	11%	—	9%	—	11%	—
PH[6]	9%	13%	11%	12%	9%	13%	11%	12%
PH[7]	9%	13%	11%	12%	9%	13%	11%	12%
PH[8]	10%	14%	11%	12%	10%	14%	11%	12%
PE[6]	10%	14%	12%	12%	10%	14%	12%	12%
PE[7]	10%	14%	12%	12%	10%	14%	12%	12%
PC[12]	10%	14%	12%	13%	10%	14%	12%	13%
PC[13]	10%	—	12%	—	10%	—	12%	—
PC[8]	10%	—	12%	—	10%	—	12%	—
PB[2]	10%	15%	12%	13%	10%	15%	12%	13%

<sup>1</sup>  $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified

<sup>2</sup> All 64 LQFP information is indicative and must be confirmed during silicon validation.

# 4.8 $\overline{\text{RESET}}$ electrical characteristics

The device implements a dedicated bidirectional RESET pin.

Figure 8. Start-up reset requirements

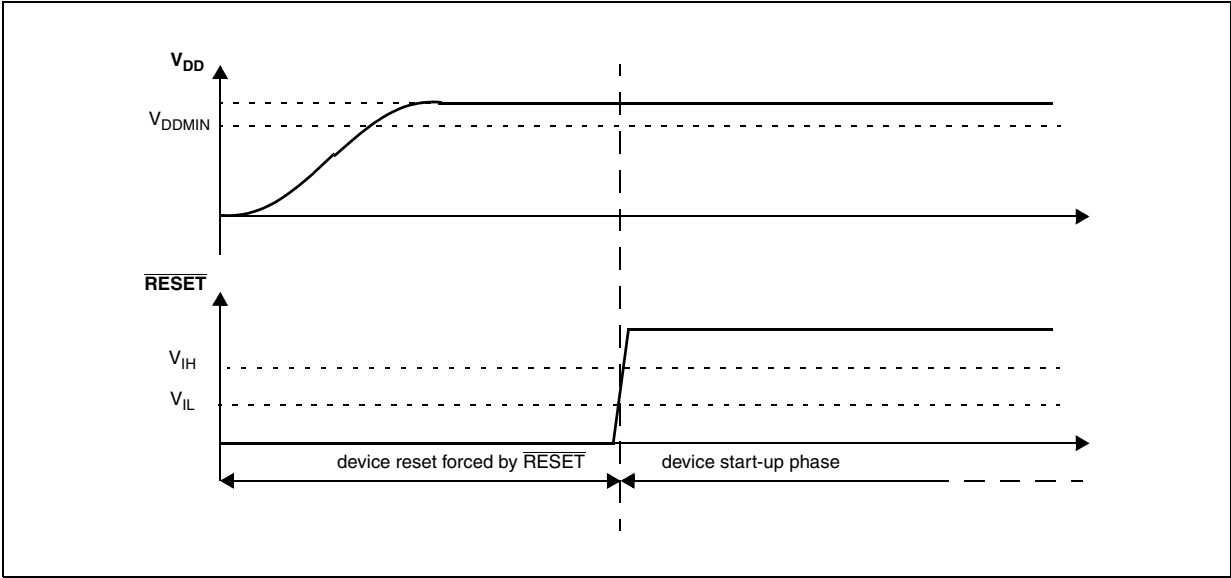


Figure 9. Noise filtering on reset signal

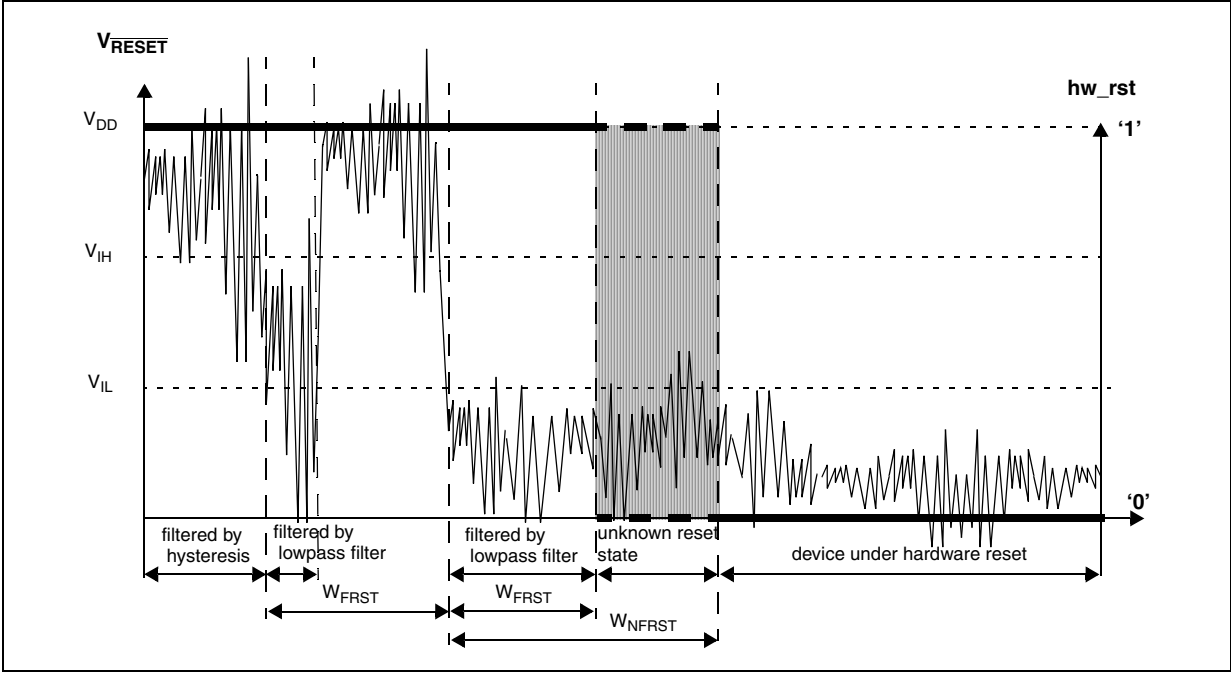


Table 18. Reset electrical characteristics

Symbol	C	Parameter	Conditions <sup>1</sup>	Value			Unit
				Min	Typ	Max	
$V_{IH}$	SR	P	Input High Level CMOS (Schmitt Trigger)	—	—	$V_{DD}+0.4$	V
$V_{IL}$	SR	P	Input low Level CMOS (Schmitt Trigger)	—	—	$0.35V_{DD}$	V
$V_{HYS}$	CC	C	Input hysteresis CMOS (Schmitt Trigger)	—	—	—	V
$V_{OL}$	CC	P	Output low level	Push Pull, $I_{OL} = 2\text{mA}$ , $V_{DD} = 5.0\text{ V} \pm 10\%$ , $PAD3V5V = 0$ (recommended)	—	$0.1V_{DD}$	V
				Push Pull, $I_{OL} = 1\text{mA}$ , $V_{DD} = 5.0\text{ V} \pm 10\%$ , $PAD3V5V = 1^2$	—	$0.1V_{DD}$	
				Push Pull, $I_{OL} = 1\text{mA}$ , $V_{DD} = 3.3\text{ V} \pm 10\%$ , $PAD3V5V = 1$ (recommended)	—	0.5	
$T_{tr}$	CC	D	Output transition time output pin <sup>3</sup>	$C_L = 25\text{pF}$ , $V_{DD} = 5.0\text{ V} \pm 10\%$ , $PAD3V5V = 0$	—	10	ns
				$C_L = 50\text{pF}$ , $V_{DD} = 5.0\text{ V} \pm 10\%$ , $PAD3V5V = 0$	—	20	
				$C_L = 100\text{pF}$ , $V_{DD} = 5.0\text{ V} \pm 10\%$ , $PAD3V5V = 0$	—	40	
				$C_L = 25\text{pF}$ , $V_{DD} = 3.3\text{ V} \pm 10\%$ , $PAD3V5V = 1$	—	12	
				$C_L = 50\text{pF}$ , $V_{DD} = 3.3\text{ V} \pm 10\%$ , $PAD3V5V = 1$	—	25	
				$C_L = 100\text{pF}$ , $V_{DD} = 3.3\text{ V} \pm 10\%$ , $PAD3V5V = 1$	—	40	
$W_{FRST}$	SR	P	$\overline{\text{RESET}}$ input filtered pulse	—	—	40	ns
$W_{NFRST}$	SR	P	$\overline{\text{RESET}}$ input not filtered pulse	—	1000	—	ns
$I_{WPU}$	CC	P	Weak pull-up current absolute value	$V_{DD} = 3.3\text{ V} \pm 10\%$ , $PAD3V5V = 1$	10	150	$\mu\text{A}$
				$V_{DD} = 5.0\text{ V} \pm 10\%$ , $PAD3V5V = 0$	10	150	
				$V_{DD} = 5.0\text{ V} \pm 10\%$ , $PAD3V5V = 1^2$	10	250	

<sup>1</sup>  $V_{DD} = 3.3\text{ V} \pm 10\%$  /  $5.0\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125\text{ }^\circ\text{C}$ , unless otherwise specified

<sup>2</sup> This transient configuration does not occurs when device is used in the  $V_{DD} = 3.3\text{ V} \pm 10\%$  range.

<sup>3</sup>  $C_L$  includes device and package capacitance ( $C_{PKG} < 5\text{ pF}$ ).

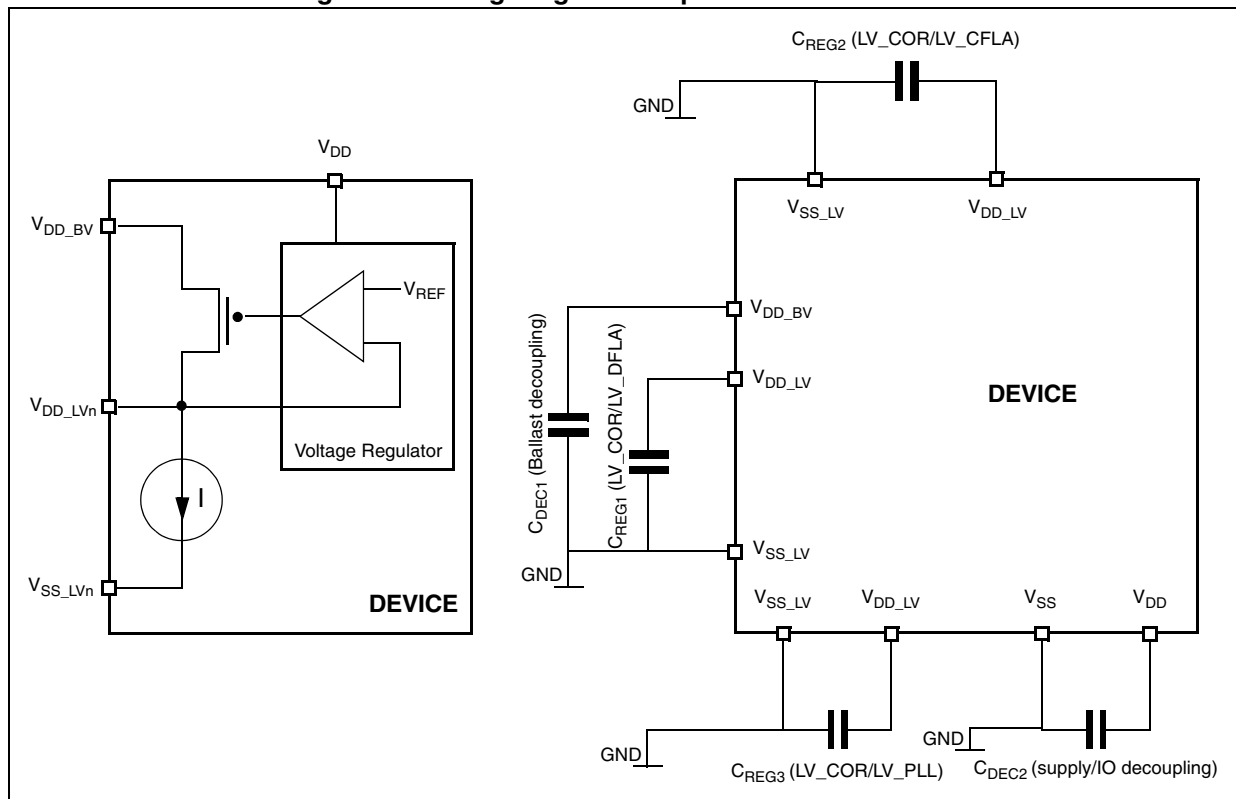
## 4.9 Power management electrical characteristics

### 4.9.1 Voltage regulator electrical characteristics

The device implements an internal voltage regulator to generate the low voltage core supply  $V_{DD\_LV}$  from the high voltage ballast supply  $V_{DD\_BV}$ . The regulator itself is supplied by the common I/O supply  $V_{DD}$ . The following supplies are involved:

- HV—High voltage external power supply for voltage regulator module. This must be provided externally through  $V_{DD}$  power pin.
- BV—High voltage external power supply for internal ballast module. This must be provided externally through  $V_{DD\_BV}$  power pin. Voltage values should be aligned with  $V_{DD}$ .
- LV—Low voltage internal power supply for core, FMPLL and flash digital logic. This is generated by the internal voltage regulator but provided outside to connect stability capacitor. It is further split into four main domains to ensure noise isolation between critical LV modules within the device:
  - LV\_COR—Low voltage supply for the core. It is also used to provide supply for FMPLL through double bonding.
  - LV\_CFLA—Low voltage supply for code flash module. It is supplied with dedicated ballast and shorted to LV\_COR through double bonding.
  - LV\_DFLA—Low voltage supply for data flash module. It is supplied with dedicated ballast and shorted to LV\_COR through double bonding.
  - LV\_PLL—Low voltage supply for FMPLL. It is shorted to LV\_COR through double bonding.

**Figure 10. Voltage regulator capacitance connection**



The internal voltage regulator requires external capacitance ( $C_{REGn}$ ) to be connected to the device in order to provide a stable low voltage digital supply to the device. Capacitances should be placed on the board as near as possible to the associated pins. Care should also be taken to limit the serial inductance of the board to less than 5 nH.



Each decoupling capacitor must be placed between each of the three  $V_{DD\_LV}/V_{SS\_LV}$  supply pairs to ensure stable voltage (see Section 4.5, “Recommended operating conditions”).

Table 19. Voltage regulator electrical characteristics

Symbol		C	Parameter	Conditions <sup>1</sup>	Value			Unit
					Min	Typ	Max	
C <sub>REGn</sub>	SR	—	Internal voltage regulator external capacitance	—	200	—	500	nF
R <sub>REG</sub>	SR	—	Stability capacitor equivalent serial resistance	—	—	—	0.2	Ω
C <sub>DEC1</sub>	SR	—	Decoupling capacitance <sup>2</sup> ballast	V <sub>DD_BV</sub> /V <sub>SS_LV</sub> pair: V <sub>DD_BV</sub> = 4.5 V to 5.5 V	100 <sup>3</sup>	470 <sup>4</sup>	—	nF
				V <sub>DD_BV</sub> /V <sub>SS_LV</sub> pair: V <sub>DD_BV</sub> = 3 V to 3.6 V	400		—	
C <sub>DEC2</sub>	SR	—	Decoupling capacitance regulator supply	V <sub>DD</sub> /V <sub>SS</sub> pair	10	100	—	nF
V <sub>MREG</sub>	CC	T	Main regulator output voltage	Before exting from reset	—	1.32	—	V
		P		After trimming	1.15	1.28	1.32	
I <sub>MREG</sub>	SR	—	Main regulator current provided to V <sub>DD_LV</sub> domain	—	—	—	150	mA
I <sub>MREGINT</sub>	CC	D	Main regulator module current consumption	I <sub>MREG</sub> = 200 mA	—	—	2	mA
				I <sub>MREG</sub> = 0 mA	—	—	1	
V <sub>LPREG</sub>	CC	P	Low power regulator output voltage	After trimming	1.15	1.23	1.32	V
I <sub>LPREG</sub>	SR	—	Low power regulator current provided to V <sub>DD_LV</sub> domain	—	—	—	15	mA
I <sub>LPREGINT</sub>	CC	D	Low power regulator module current consumption	I <sub>LPREG</sub> = 15 mA; T <sub>A</sub> = 55 °C	—	—	600	μA
		—		I <sub>LPREG</sub> = 0 mA; T <sub>A</sub> = 55 °C	—	5	—	
V <sub>ULPREG</sub>	CC	P	Ultra low power regulator output voltage	After trimming	1.15	1.23	1.32	V
I <sub>ULPREG</sub>	SR	—	Ultra low power regulator current provided to V <sub>DD_LV</sub> domain	—	—	—	5	mA
I <sub>ULPREGINT</sub>	CC	D	Ultra low power regulator module current consumption	I <sub>ULPREG</sub> = 5 mA; T <sub>A</sub> = 55 °C	—	—	100	μA
				I <sub>ULPREG</sub> = 0 mA; T <sub>A</sub> = 55 °C	—	2	—	
I <sub>DD_BV</sub>	CC	D	In-rush current on V <sub>DD_BV</sub> during power-up <sup>5</sup>	—	—	—	400 <sup>6</sup>	mA

<sup>1</sup>  $V_{DD} = 3.3 \text{ V} \pm 10\% / 5.0 \text{ V} \pm 10\%$ ,  $T_A = -40 \text{ to } 125 \text{ }^\circ\text{C}$ , unless otherwise specified

<sup>2</sup> This capacitance value is driven by the constraints of the external voltage regulator supplying the  $V_{DD\_BV}$  voltage. A typical value is in the range of 470 nF.

<sup>3</sup> This value is acceptable to guarantee operation from 4.5 V to 5.5 V

## Electrical characteristics

- <sup>4</sup> External regulator and capacitance circuitry must be capable of providing  $I_{DD\_BV}$  while maintaining supply  $V_{DD\_BV}$  in operating range.
- <sup>5</sup> In-rush current is seen only for short time during power-up and on standby exit (max 20  $\mu$ s, depending on external LV capacitances to be load)
- <sup>6</sup> The duration of the in-rush current depends on the capacitance placed on LV pins. BV decaps must be sized accordingly. Refer to IMREG value for minimum amount of current to be provided in cc.

### 4.9.2 Voltage monitor electrical characteristics

The device implements a Power-on Reset (POR) module to ensure correct power-up initialization, as well as four low voltage detectors (LVDs) to monitor the  $V_{DD}$  and the  $V_{DD\_LV}$  voltage while device is supplied:

- POR monitors  $V_{DD}$  during the power-up phase to ensure device is maintained in a safe reset state
- LVDHV3 monitors  $V_{DD}$  to ensure device reset below minimum functional supply
- LVDHV5 monitors  $V_{DD}$  when application uses device in the  $5.0\text{ V} \pm 10\%$  range
- LVDLVCOR monitors power domain No. 1
- LVDLVBKP monitors power domain No. 0

#### NOTE

When enabled, power domain No. 2 is monitored through LVD\_DIGBKP.

**Figure 11. Low voltage monitor vs reset**

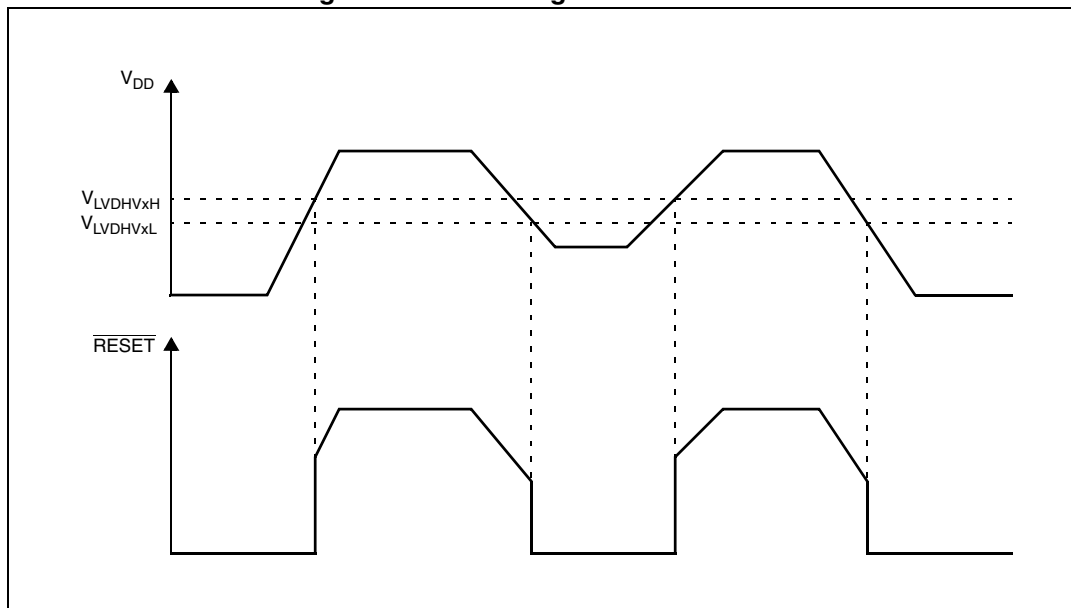


Table 20. Low voltage monitor electrical characteristics

Symbol		C	Parameter	Conditions <sup>1</sup>	Value			Unit
					Min	Typ	Max	
V <sub>PORUP</sub>	SR	P	Supply for functional POR module	—	1.0	—	5.5	V
V <sub>PORH</sub>	CC	P	Power-on reset threshold	T <sub>A</sub> = 25 °C, after trimming	1.5	—	2.6	
		T		—	1.5	—	2.6	
V <sub>LVDHV3H</sub>	CC	T	LVDHV3 low voltage detector high threshold	—	—	—	2.95	
V <sub>LVDHV3L</sub>	CC	P	LVDHV3 low voltage detector low threshold		2.6	—	2.9	
V <sub>LVDHV5H</sub>	CC	T	LVDHV5 low voltage detector high threshold		—	—	4.5	
V <sub>LVDHV5L</sub>	CC	P	LVDHV5 low voltage detector low threshold		3.8	—	4.4	
V <sub>LVDLVCORL</sub>	CC	P	LVDLVCOR low voltage detector low threshold		1.08	—	1.5	
V <sub>LVDLVBKPL</sub>	CC	P	LVDLVBKP low voltage detector low threshold		1.08	—	1.14	

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

## 4.10 Low voltage domain power consumption

Table 21 provides DC electrical characteristics for significant application modes. These values are indicative values; actual consumption depends on the application.

Table 21. Low voltage power domain electrical characteristics

Symbol		C	Parameter	Conditions <sup>1</sup>		Value			Unit
						Min	Typ	Max	
I <sub>DDMAX</sub> <sup>2</sup>	CC	D	RUN mode maximum average current	—		—	115	140 <sup>3</sup>	mA
I <sub>DDRUN</sub> <sup>4</sup>	CC	T	RUN mode typical average current <sup>5</sup>	f <sub>CPU</sub> = 8 MHz	—	7	—	mA	
		T		f <sub>CPU</sub> = 16 MHz	—	18	—		
		T		f <sub>CPU</sub> = 32 MHz	—	29	—		
		P		f <sub>CPU</sub> = 48 MHz	—	40	—		
		P		f <sub>CPU</sub> = 64 MHz	—	51	—		
I <sub>DDHALT</sub>	CC	C	HALT mode current <sup>6</sup>	Slow internal RC oscillator (128 kHz) running	T <sub>A</sub> = 25 °C	—	8	15	mA
		P			T <sub>A</sub> = 125 °C	—	14	25	
I <sub>DDSTOP</sub>	CC	P	STOP mode current <sup>7</sup>	Slow internal RC oscillator (128 kHz) running	T <sub>A</sub> = 25 °C	—	180	700 <sup>8</sup>	μA
		D			T <sub>A</sub> = 55 °C	—	500	—	
		D			T <sub>A</sub> = 85 °C	—	1	—	mA
		D			T <sub>A</sub> = 105 °C	—	2	—	
		P			T <sub>A</sub> = 125 °C	—	4.5	12 <sup>8</sup>	

Table 21. Low voltage power domain electrical characteristics (continued)

Symbol		C	Parameter	Conditions <sup>1</sup>		Value			Unit
						Min	Typ	Max	
I <sub>DDSTDBY2</sub>	CC	P	STANDBY2 mode current <sup>9</sup>	Slow internal RC oscillator (128 kHz) running	T <sub>A</sub> = 25 °C	—	30	100	μA
		D			T <sub>A</sub> = 55 °C	—	75	—	
		D			T <sub>A</sub> = 85 °C	—	180	—	
		D			T <sub>A</sub> = 105 °C	—	315	—	
		P			T <sub>A</sub> = 125 °C	—	560	1700	
I <sub>DDSTDBY1</sub>	CC	T	STANDBY1 mode current <sup>10</sup>	Slow internal RC oscillator (128 kHz) running	T <sub>A</sub> = 25 °C	—	20	60	μA
		D			T <sub>A</sub> = 55 °C	—	45	—	
		D			T <sub>A</sub> = 85 °C	—	100	—	
		D			T <sub>A</sub> = 105 °C	—	165	—	
		D			T <sub>A</sub> = 125 °C	—	280	900	

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> Running consumption is given on voltage regulator supply (V<sub>DDREG</sub>). I<sub>DDMAX</sub> is composed of three components: I<sub>DDMAX</sub> = I<sub>DD</sub>(vdd\_bv) + I<sub>DD</sub>(vdd\_hv) + I<sub>DD</sub>(Vdd\_hv\_adc). It does not include a fourth component linked to I/Os toggling which is **highly** dependent on the application. The given value is thought to be a **worst case value** with all peripherals running, and code fetched from code flash while modify operation on-going on data flash. It is to be noticed that this value can be significantly reduced by application: switch-off not used peripherals (default), reduce peripheral frequency through internal prescaler, fetch from RAM most used functions, use low power mode when possible.

<sup>3</sup> Higher current may be sinked by device during power-up and standby exit. please refer to in rush current on [Table 19](#).

<sup>4</sup> RUN current measured with typical application with accesses on both flash and RAM.

<sup>5</sup> Only for the “P” classification: Data and Code Flash in Normal Power. Code fetched from RAM: Serial IPs CAN and LIN in loop back mode, DSPi as Master, PLL as system Clock (4 x Multiplier) peripherals on (eMIOS/CTU/ADC) and running at max frequency, periodic SW/WDG timer reset enabled.

<sup>6</sup> Data Flash Power Down. Code Flash in Low Power. RC-osc128kHz & RC-OSC 16MHz on. 10MHz XTAL clock. FlexCAN: instances: 0, 1, 2 ON (clocked but not reception or transmission), instances: 4, 5, 6 clock gated. LINFlex: instances: 0, 1, 2 ON (clocked but not reception or transmission), instance: 3 clock gated. eMIOS: instance: 0 ON (16 channels on PA[0]-PA[11] and PC[12]-PC[15]) with PWM 20kHz, instance: 1 clock gated. DSPi: instance: 0 (clocked but no communication). RTC/API ON. PIT ON. STM ON. ADC ON but not conversion except 2 analogue watchdog

<sup>7</sup> Only for the “P” classification: No clock, RC 16MHz off, RC128kHz on, PLL off, HPvreg off, ULPVreg/LPVreg on. All possible peripherals off and clock gated. Flash in power down mode.

<sup>8</sup> When going from RUN to STOP mode and the core consumption is > 6 mA, it is normal operation for the main regulator module to be kept on by the on-chip current monitoring circuit. This is most likely to occur with junction temperatures exceeding 125 °C and under these circumstances, it is possible for the current to initially exceed the maximum STOP specification by up to 2 mA. After entering stop, the application junction temperature will reduce to the ambient level and the main regulator will be automatically switched off when the load current is below 6 mA.

<sup>9</sup> Only for the “P” classification: ULPreg on, HP/LPVreg off, 32kB RAM on, device configured for minimum consumption, all possible modules switched-off.

<sup>10</sup> ULPreg on, HP/LPVreg off, 8kB RAM on, device configured for minimum consumption, all possible modules switched-off.

## 4.11 Flash memory electrical characteristics

### 4.11.1 Program/Erase characteristics

Table 22 shows the program and erase characteristics.

**Table 22. Program and erase specifications**

Symbol		C	Parameter	Value				Unit
				Min	Typ <sup>1</sup>	Initial max <sup>2</sup>	Max <sup>3</sup>	
T <sub>dwprogram</sub>	CC	C	Double word (64 bits) program time <sup>4</sup>	—	22	50	500	μs
T <sub>16Kpperase</sub>			16 KB block pre-program and erase time	—	300	500	5000	ms
T <sub>32Kpperase</sub>			32 KB block pre-program and erase time	—	400	600	5000	ms
T <sub>128Kpperase</sub>			128 KB block pre-program and erase time	—	800	1300	7500	ms
T <sub>eslat</sub>	CC	D	Erase Suspend Latency	—	—	30	30	μs

<sup>1</sup> Typical program and erase times assume nominal supply values and operation at 25 °C.

<sup>2</sup> Initial factory condition: < 100 program/erase cycles, 25 °C, typical supply voltage.

<sup>3</sup> The maximum program and erase times occur after the specified number of program/erase cycles. These maximum values are characterized but not guaranteed.

<sup>4</sup> Actual hardware programming times. This does not include software overhead.

**Table 23. Flash module life**

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
P/E	CC	C	Number of program/erase cycles per block for 16 Kbyte blocks over the operating temperature range (T <sub>J</sub> )	100,000	—	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 32 Kbyte blocks over the operating temperature range (T <sub>J</sub> )	10,000	100,000	—	cycles
P/E	CC	C	Number of program/erase cycles per block for 128 Kbyte blocks over the operating temperature range (T <sub>J</sub> )	1,000	100,000	—	cycles
Retention	CC	C	Minimum data retention at 85 °C average ambient temperature <sup>1</sup>	Blocks with 0–1,000 P/E cycles	20	—	years
				Blocks with 1,001–10,000 P/E cycles	10	—	years
				Blocks with 10,001–100,000 P/E cycles	5	—	years

# Electrical characteristics

<sup>1</sup> Ambient temperature averaged over duration of application, not to exceed recommended product operating temperature range.

ECC circuitry provides correction of single bit faults and is used to improve further automotive reliability results. Some units will experience single bit corrections throughout the life of the product with no impact to product reliability.

Table 24. Flash read access timing

Symbol		C	Parameter	Conditions <sup>1</sup>	Max	Unit
f <sub>READ</sub>	CC	P	Maximum frequency for Flash reading	2 wait states	64	MHz
		C		1 wait state	40	
		C		0 wait states	20	

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

## 4.11.2 Flash power supply DC characteristics

Table 25 shows the power supply DC characteristics on external supply.

**Table 25. Code Flash power supply DC electrical characteristics**

Symbol	C	D	Parameter	Conditions <sup>1</sup>	Value			Unit
					Min	Typ	Max	
I <sub>FREAD</sub> <sup>2</sup>	CC	D	Sum of the current consumption on V <sub>DDHV</sub> and V <sub>DDBV</sub> on read access	Code Flash module read f <sub>CPU</sub> = 64 MHz <sup>3</sup>	—	15	33	mA
				Data Flash module read f <sub>CPU</sub> = 64 MHz <sup>3</sup>	—	15	33	
I <sub>FMOD</sub> <sup>2</sup>	CC	D	Sum of the current consumption on V <sub>DDHV</sub> and V <sub>DDBV</sub> on matrix modification (program/erase)	Program/Erase on-going while reading Code Flash registers f <sub>CPU</sub> = 64 MHz <sup>3</sup>	—	15	33	mA
				Program/Erase on-going while reading Data Flash registers f <sub>CPU</sub> = 64 MHz <sup>3</sup>	—	15	33	
I <sub>FLPW</sub>	CC	D	Sum of the current consumption on V <sub>DDHV</sub> and V <sub>DDBV</sub>	during Code Flash low-power mode	—	—	900	μA
				during Data Flash low-power mode	—	—	900	
I <sub>FPWD</sub>	CC	D	Sum of the current consumption on V <sub>DDHV</sub> and V <sub>DDBV</sub>	during Code Flash powe-down mode	—	—	150	μA
				during Data Flash powe-down mode	—	—	150	

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> This value is only relative to the actual duration of the read cycle

<sup>3</sup> f<sub>CPU</sub> 64 MHz can be achieved only at up to 105 °C

### 4.11.3 Start-up/Switch-off timings

Table 26. Start-up time/Switch-off time

Symbol	C	Parameter	Conditions <sup>1</sup>	Value			Unit
				Min	Typ	Max	
T <sub>FLARSTEXIT</sub>	CC	Delay for Flash module to exit reset mode	Code Flash	—	—	125	μs
			Data Flash	—	—	125	
T <sub>FLALPEXIT</sub>	CC	Delay for Flash module to exit low-power mode	Code Flash	—	—	0.5	
			Data Flash	—	—	0.5	
T <sub>FLAPDEXIT</sub>	CC	Delay for Flash module to exit power-down mode	Code Flash	—	—	30	
			Data Flash	—	—	30	
T <sub>FLALPENTRY</sub>	CC	Delay for Flash module to enter low-power mode	Code Flash	—	—	0.5	
			Data Flash	—	—	0.5	
T <sub>FLAPDENTRY</sub>	CC	Delay for Flash module to enter power-down mode	Code Flash	—	—	1.5	
			Data Flash	—	—	1.5	

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = –40 to 125 °C, unless otherwise specified



## 4.12 Electromagnetic compatibility (EMC) characteristics

Susceptibility tests are performed on a sample basis during product characterization.

### 4.12.1 Designing hardened software to avoid noise problems

EMC characterization and optimization are performed at component level with a typical application environment and simplified MCU software. It should be noted that good EMC performance is highly dependent on the user application and the software in particular.

Therefore it is recommended that the user apply EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

- Software recommendations: The software flowchart must include the management of runaway conditions such as:
  - Corrupted program counter
  - Unexpected reset
  - Critical data corruption (control registers...)
- Prequalification trials: Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the reset pin or the oscillator pins for 1 second.  
To complete these trials, ESD stress can be applied directly on the device. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring.

### 4.12.2 Electromagnetic interference (EMI)

The product is monitored in terms of emission based on a typical application. This emission test conforms to the IEC 61967-1 standard, which specifies the general conditions for EMI measurements.

**Table 27. EMI radiated emission measurement<sup>1,2</sup>**

Symbol	C	Parameter	Conditions	Value			Unit
				Min	Typ	Max	
—	SR	Scan range	—	0.150	—	1000	MHz
$f_{\text{CPU}}$	SR	Operating frequency	—	—	64	—	MHz
$V_{\text{DD\_LV}}$	SR	LV operating voltages	—	—	1.28	—	V
$S_{\text{EMI}}$	CC	T	Peak level $V_{\text{DD}} = 5 \text{ V}$ , $T_{\text{A}} = 25 \text{ }^{\circ}\text{C}$ , LQFP144 package Test conforming to IEC 61967-2, $f_{\text{OSC}} = 8 \text{ MHz}/f_{\text{CPU}} = 64 \text{ MHz}$	No PLL frequency modulation	—	—	18 dB $\mu$ V
				$\pm 2\%$ PLL frequency modulation	—	—	14 dB $\mu$ V

<sup>1</sup> EMI testing and I/O port waveforms per IEC 61967-1, -2, -4

<sup>2</sup> For information on conducted emission and susceptibility measurement (norm IEC 61967-4), please contact your local marketing representative.

### 4.12.3 Absolute maximum ratings (electrical sensitivity)

Based on two different tests (ESD and LU) using specific measurement methods, the product is stressed in order to determine its performance in terms of electrical sensitivity.

### 4.12.3.1 Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts\*(n+1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**Table 28. ESD absolute maximum ratings<sup>1 2</sup>**

Symbol	C		Ratings	Conditions	Class	Max value	Unit
V <sub>ESD(HBM)</sub>	CC	T	Electrostatic discharge voltage (Human Body Model)	T <sub>A</sub> = 25 °C conforming to AEC-Q100-002	H1C	2000	V
V <sub>ESD(MM)</sub>	CC	T	Electrostatic discharge voltage (Machine Model)	T <sub>A</sub> = 25 °C conforming to AEC-Q100-003	M2	200	
V <sub>ESD(CDM)</sub>	CC	T	Electrostatic discharge voltage (Charged Device Model)	T <sub>A</sub> = 25 °C conforming to AEC-Q100-011	C3A	500 750 (corners)	

<sup>1</sup> All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

<sup>2</sup> A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

### 4.12.3.2 Static latch-up (LU)

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with the EIA/JESD 78 IC latch-up standard.

**Table 29. Latch-up results**

Symbol	C		Parameter	Conditions	Class
LU	CC	T	Static latch-up class	T <sub>A</sub> = 125 °C conforming to JESD 78	II level A

## 4.13 Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

The device provides an oscillator/resonator driver. Figure 12 describes a simple model of the internal oscillator driver and provides an example of a connection for an oscillator or a resonator.

Table 30 provides the parameter description of 4 MHz to 16 MHz crystals used for the design simulations.

**Figure 12. Crystal oscillator and resonator connection scheme**

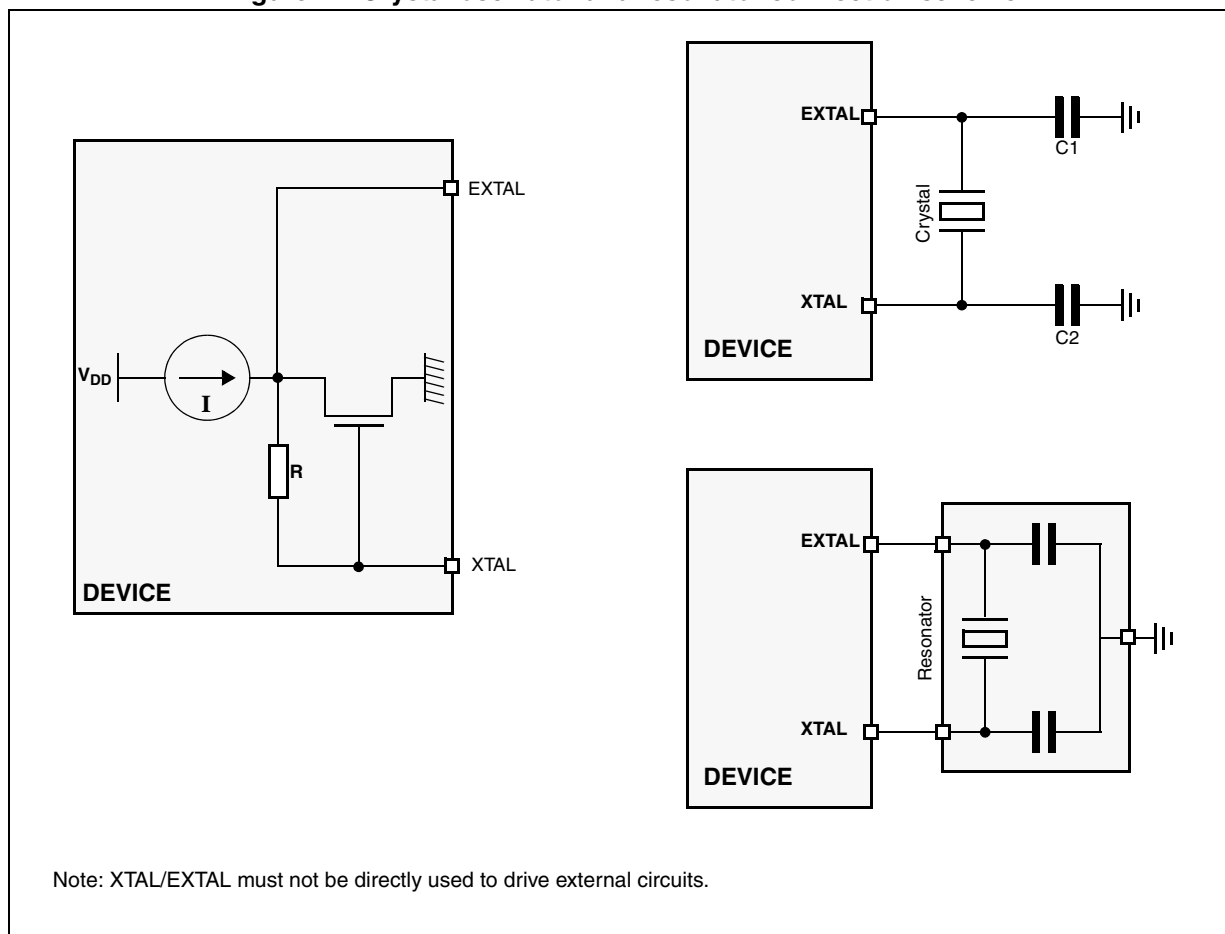


Table 30. Crystal description

Nominal frequency (MHz)	NDK crystal reference	Crystal equivalent series resistance ESR $\Omega$	Crystal motional capacitance ( $C_m$ ) fF	Crystal motional inductance ( $L_m$ ) mH	Load on xtalín/xtalout $C1 = C2$ (pF) <sup>1</sup>	Shunt capacitance between xtalout and xtalín $C0^2$ (pF)
4	NX8045GB	300	2.68	591.0	21	2.93
8	NX5032GA	300	2.46	160.7	17	3.01
10		150	2.93	86.6	15	2.91
12		120	3.11	56.5	15	2.93
16		120	3.90	25.3	10	3.00

<sup>1</sup> The values specified for C1 and C2 are the same as used in simulations. It should be ensured that the testing includes all the parasitics (from the board, probe, crystal, etc.) as the AC / transient behavior depends upon them.

<sup>2</sup> The value of C0 specified here includes 2 pF additional capacitance for parasitics (to be seen with bond-pads, package, etc.).

Figure 13. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

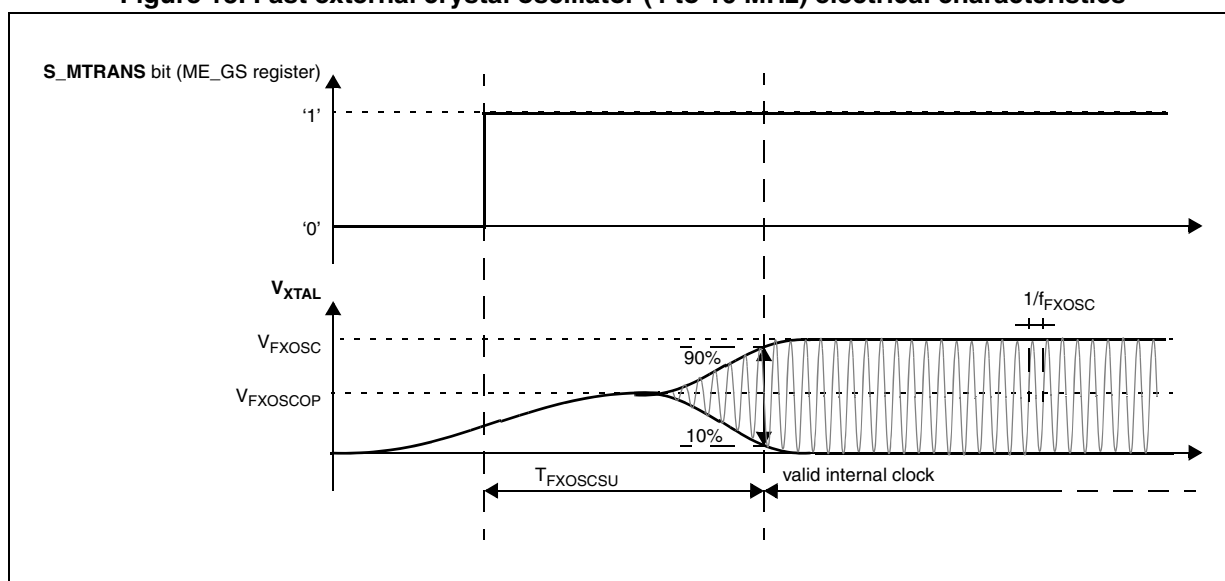


Table 31. Fast external crystal oscillator (4 to 16 MHz) electrical characteristics

Symbol		C	Parameter	Conditions <sup>1</sup>	Value			Unit
					Min	Typ	Max	
f <sub>FXOSC</sub>	SR	—	Fast external crystal oscillator frequency	—	4.0	—	16.0	MHz
g <sub>mFXOSC</sub>	CC	C	Fast external crystal oscillator transconductance	V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 0	2.2	—	8.2	mA/V
	CC	P		V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 0	2.0	—	7.4	
	CC	C		V <sub>DD</sub> = 3.3 V ± 10%, PAD3V5V = 1 OSCILLATOR_MARGIN = 1	2.7	—	9.7	
	CC	C		V <sub>DD</sub> = 5.0 V ± 10%, PAD3V5V = 0 OSCILLATOR_MARGIN = 1	2.5	—	9.2	
V <sub>FXOSC</sub>	CC	T	Oscillation amplitude at EXTAL	f <sub>OSC</sub> = 4 MHz, OSCILLATOR_MARGIN = 0	1.3	—	—	V
				f <sub>OSC</sub> = 16 MHz, OSCILLATOR_MARGIN = 1	1.3	—	—	
V <sub>FXOSCOPI</sub>	CC	P	Oscillation operating point	—	—	0.95		V
I <sub>FXOSC</sub> <sup>2</sup>	CC	T	Fast external crystal oscillator consumption	—	—	2	3	mA
T <sub>FXOSCSU</sub>	CC	T	Fast external crystal oscillator start-up time	f <sub>OSC</sub> = 4 MHz, OSCILLATOR_MARGIN = 0	—	—	6	ms
				f <sub>OSC</sub> = 16 MHz, OSCILLATOR_MARGIN = 1	—	—	1.8	
V <sub>IH</sub>	SR	P	Input high level CMOS (Schmitt Trigger)	Oscillator bypass mode	0.65V <sub>DD</sub>	—	V <sub>DD</sub> +0.4	V
V <sub>IL</sub>	SR	P	Input low level CMOS (Schmitt Trigger)	Oscillator bypass mode	−0.4	—	0.35V <sub>DD</sub>	V

<sup>1</sup>  $V_{DD} = 3.3\text{ V} \pm 10\%$  /  $5.0\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified

<sup>2</sup> Stated values take into account only analog module consumption but not the digital contributor (clock tree and enabled peripherals)

# 4.14 Slow external crystal oscillator (32 kHz) electrical characteristics

The device provides a low power oscillator/resonator driver.

Figure 14. Crystal oscillator and resonator connection scheme

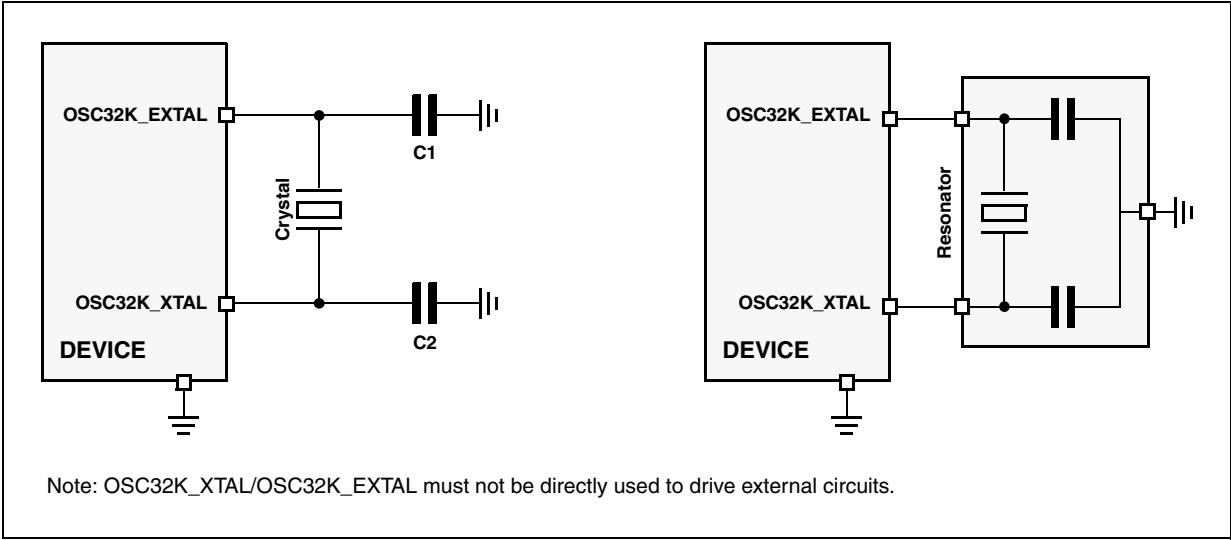


Figure 15. Equivalent circuit of a quartz crystal

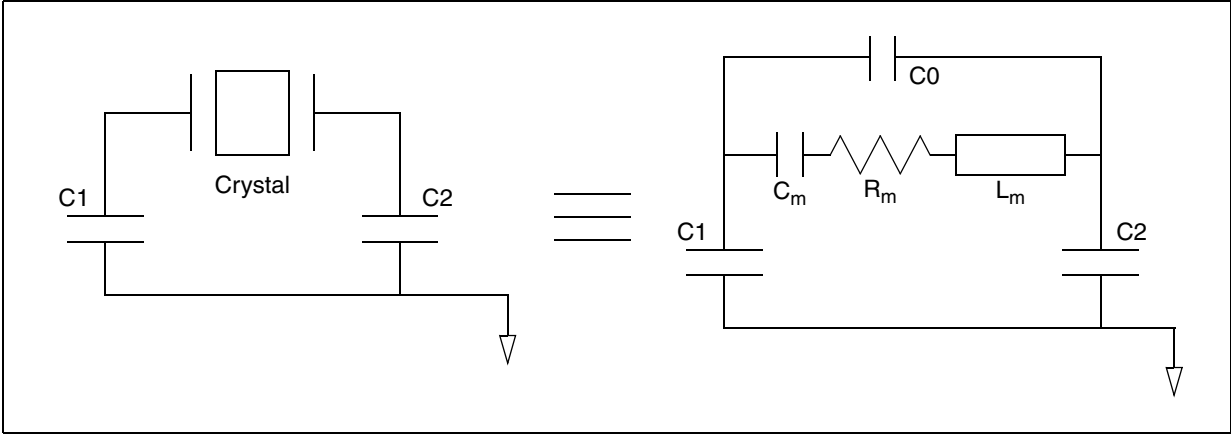


Table 32. Crystal motional characteristics<sup>1</sup>

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$L_m$	Motional inductance	—	—	11.796	—	KH
$C_m$	Motional capacitance	—	—	2	—	fF
C1/C2	Load capacitance at OSC32K_XTAL and OSC32K_EXTAL with respect to ground <sup>2</sup>	—	18	—	28	pF
$R_m$ <sup>3</sup>	Motional resistance	AC coupled @ $C_0 = 2.85 \text{ pF}$ <sup>4</sup>	—	—	65	k $\Omega$
		AC coupled @ $C_0 = 4.9 \text{ pF}$ <sup>4</sup>	—	—	50	
		AC coupled @ $C_0 = 7.0 \text{ pF}$ <sup>4</sup>	—	—	35	
		AC coupled @ $C_0 = 9.0 \text{ pF}$ <sup>4</sup>	—	—	30	

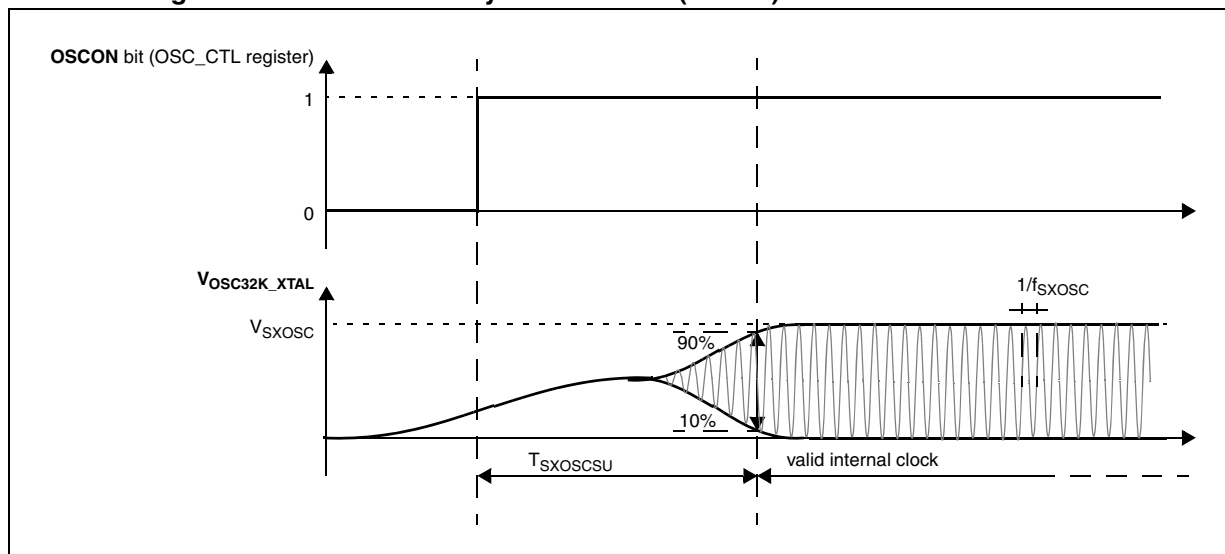
<sup>1</sup> The crystal used is Epson Toyocom MC306.

<sup>2</sup> This is the recommended range of load capacitance at OSC32K\_XTAL and OSC32K\_EXTAL with respect to ground. It includes all the parasitics due to board traces, crystal and package.

<sup>3</sup> Maximum ESR ( $R_m$ ) of the crystal is 50 k $\Omega$

<sup>4</sup>  $C_0$  Includes a parasitic capacitance of 2.0 pF between OSC32K\_XTAL and OSC32K\_EXTAL pins

Figure 16. Slow external crystal oscillator (32 kHz) electrical characteristics



**Table 33. Slow external crystal oscillator (32 kHz) electrical characteristics**

Symbol		C	Parameter	Conditions <sup>1</sup>	Value			Unit
					Min	Typ	Max	
f <sub>SXOSC</sub>	SR	—	Slow external crystal oscillator frequency	—	32	32.768	40	kHz
V <sub>SXOSC</sub>	CC	T	Oscillation amplitude	—	—	2.1	—	V
I <sub>SXOSCBIAS</sub>	CC	T	Oscillation bias current	—	—	2.5	—	μA
I <sub>SXOSC</sub>	CC	T	Slow external crystal oscillator consumption	—	—	—	8	μA
T <sub>SXOSCSU</sub>	CC	T	Slow external crystal oscillator start-up time	—	—	—	2 <sup>2</sup>	s

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified

<sup>2</sup> Start-up time has been measured with EPSON TOYOCOM MC306 crystal. Variation may be seen with other crystal

## 4.15 FMPLL electrical characteristics

The device provides a frequency-modulated phase-locked loop (FMPLL) module to generate a fast system clock from the main oscillator driver.

**Table 34. FMPLL electrical characteristics**

Symbol		C		Parameter	Conditions <sup>1</sup>	Value			Unit
						Min	Typ	Max	
f <sub>PLLIN</sub>	SR	—		FMPLL reference clock <sup>2</sup>	—	4	—	64	MHz
Δ <sub>PLLIN</sub>	SR	—		FMPLL reference clock duty cycle <sup>2</sup>	—	40	—	60	%
f <sub>PLLOUT</sub>	CC	D		FMPLL output clock frequency	—	16	—	64	MHz
f <sub>VCO</sub> <sup>3</sup>	CC	P		VCO frequency without frequency modulation	—	256	—	512	MHz
		P		VCO frequency with frequency modulation	—	245	—	533	
f <sub>CPU</sub>	SR	—		System clock frequency	—	—	—	64	MHz
f <sub>FREE</sub>	CC	P		Free-running frequency	—	20	—	150	MHz
t <sub>LOCK</sub>	CC	P		FMPLL lock time	Stable oscillator (f <sub>PLLIN</sub> = 16 MHz)		40	100	μs
Δt <sub>LTJIT</sub>	CC	—		FMPLL long term jitter	f <sub>PLLIN</sub> = 16 MHz (resonator), f <sub>PLLCLK</sub> @ 64 MHz, 4000 cycles	—	—	10	ns
I <sub>PLL</sub>	CC	C		FMPLL consumption	T <sub>A</sub> = 25 °C	—	—	4	mA

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = -40 to 125 °C, unless otherwise specified.

<sup>2</sup> PLLIN clock retrieved directly from FXOSC clock. Input characteristics are granted when oscillator is used in functional mode. When bypass mode is used, oscillator input clock should verify f<sub>PLLIN</sub> and Δ<sub>PLLIN</sub>.

<sup>3</sup> Frequency modulation is considered ± 4%



## 4.16 Fast internal RC oscillator (16 MHz) electrical characteristics

The device provides a 16 MHz fast internal RC oscillator. This is used as the default clock at the power-up of the device.

**Table 35. Fast internal RC oscillator (16 MHz) electrical characteristics**

Symbol	C	P	Parameter	Conditions <sup>1</sup>	Value			Unit
					Min	Typ	Max	
$f_{\text{FIRC}}$	CC	P	Fast internal RC oscillator high frequency	$T_A = 25\text{ }^{\circ}\text{C}$ , trimmed	—	16	—	MHz
	SR	—		—	12	—	20	
$I_{\text{FIRCRUN}}^2$	CC	T	Fast internal RC oscillator high frequency current in running mode	$T_A = 25\text{ }^{\circ}\text{C}$ , trimmed	—	—	200	$\mu\text{A}$
$I_{\text{FIRCPWD}}$	CC	D	Fast internal RC oscillator high frequency current in power down mode	$T_A = 125\text{ }^{\circ}\text{C}$	—	—	10	$\mu\text{A}$
$I_{\text{FIRCSTOP}}$	CC	T	Fast internal RC oscillator high frequency and system clock current in stop mode	$T_A = 25\text{ }^{\circ}\text{C}$ sysclk = off	—	500	—	$\mu\text{A}$
				sysclk = 2 MHz	—	600	—	
				sysclk = 4 MHz	—	700	—	
				sysclk = 8 MHz	—	900	—	
				sysclk = 16 MHz	—	1250	—	
$T_{\text{FIRCSU}}$	CC	C	Fast internal RC oscillator start-up time	$V_{\text{DD}} = 5.0\text{ V} \pm 10\%$	—	1.1	2.0	$\mu\text{s}$
$\Delta_{\text{FIRCPRE}}$	CC	T	Fast internal RC oscillator precision after software trimming of $f_{\text{FIRC}}$	$T_A = 25\text{ }^{\circ}\text{C}$	–1	—	+1	%
$\Delta_{\text{FIRC}}^{\text{TRIM}}$	CC	T	Fast internal RC oscillator trimming step	$T_A = 25\text{ }^{\circ}\text{C}$	—	1.6	—	%
$\Delta_{\text{FIRC}}^{\text{VAR}}$	CC	P	Fast internal RC oscillator variation in overtemperature and supply with respect to $f_{\text{FIRC}}$ at $T_A = 25\text{ }^{\circ}\text{C}$ in high-frequency configuration	—	–5	—	+5	%

<sup>1</sup>  $V_{\text{DD}} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.

<sup>2</sup> This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

## 4.17 Slow internal RC oscillator (128 kHz) electrical characteristics

The device provides a 128 kHz slow internal RC oscillator. This can be used as the reference clock for the RTC module.

Table 36. Slow internal RC oscillator (128 kHz) electrical characteristics

Symbol	C	Parameter	Conditions <sup>1</sup>	Value			Unit
				Min	Typ	Max	
$f_{SIRC}$	CC	P Slow internal RC oscillator low frequency	$T_A = 25\text{ }^{\circ}\text{C}$ , trimmed	—	128	—	kHz
	SR		—	100	—	150	
$I_{SIRC}^{2,}$	CC	C Slow internal RC oscillator low frequency current	$T_A = 25\text{ }^{\circ}\text{C}$ , trimmed	—	—	5	$\mu\text{A}$
$T_{SIRCSU}$	CC	P Slow internal RC oscillator start-up time	$T_A = 25\text{ }^{\circ}\text{C}$ , $V_{DD} = 5.0\text{ V} \pm 10\%$	—	8	12	$\mu\text{s}$
$\Delta_{SIRCPRE}$	CC	C Slow internal RC oscillator precision after software trimming of $f_{SIRC}$	$T_A = 25\text{ }^{\circ}\text{C}$	-2	—	+2	%
$\Delta_{SIRCTRM}$	CC	C Slow internal RC oscillator trimming step	—	—	2.7	—	
$\Delta_{SIRCVAR}$	CC	C Slow internal RC oscillator variation in temperature and supply with respect to $f_{SIRC}$ at $T_A = 55\text{ }^{\circ}\text{C}$ in high frequency configuration	High frequency configuration	-10	—	+10	%

<sup>1</sup>  $V_{DD} = 3.3\text{ V} \pm 10\% / 5.0\text{ V} \pm 10\%$ ,  $T_A = -40$  to  $125\text{ }^{\circ}\text{C}$ , unless otherwise specified.

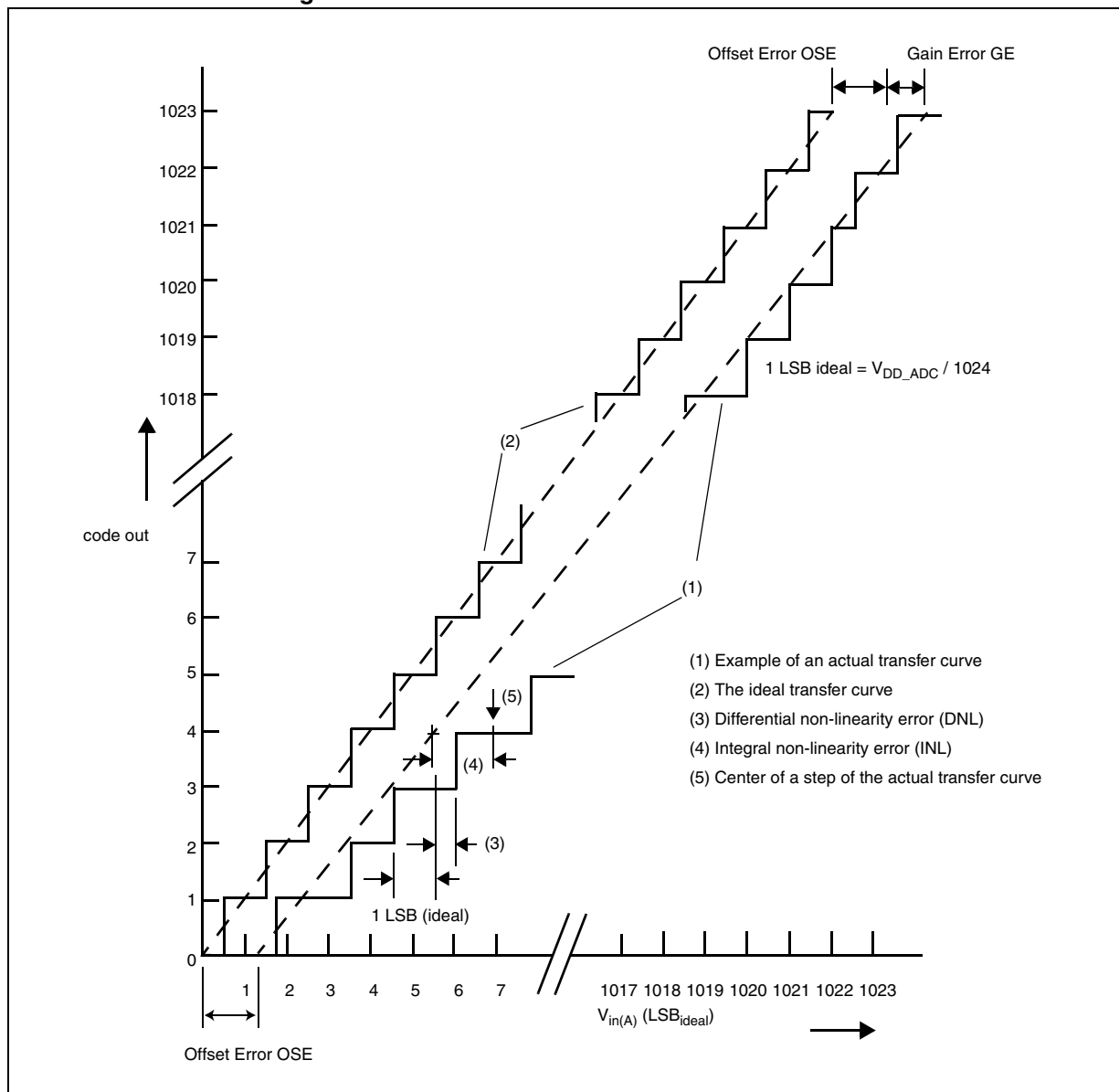
<sup>2</sup> This does not include consumption linked to clock tree toggling and peripherals consumption when RC oscillator is ON.

## 4.18 ADC electrical characteristics

### 4.18.1 Introduction

The device provides a 10-bit Successive Approximation Register (SAR) analog-to-digital converter.

Figure 17. ADC characteristic and error definitions



#### 4.18.2 Input impedance and ADC accuracy

In the following analysis, the input circuit corresponding to the precise channels is considered.

To preserve the accuracy of the A/D converter, it is necessary that analog input pins have low AC impedance. Placing a capacitor with good high frequency characteristics at the input pin of the device can be effective: the capacitor should be as large as possible, ideally infinite. This capacitor contributes to attenuating the noise present on the input pin; furthermore, it sources charge during the sampling phase, when the analog signal source is a high-impedance source.

A real filter can typically be obtained by using a series resistance with a capacitor on the input pin (simple RC filter). The RC filtering may be limited according to the value of source impedance of the transducer or circuit supplying the analog signal to be measured. The filter at the input pins must be designed taking into account the dynamic characteristics of the input signal (bandwidth) and the equivalent input impedance of the ADC itself.

## Electrical characteristics

In fact a current sink contributor is represented by the charge sharing effects with the sampling capacitance:  $C_S$  being substantially a switched capacitance, with a frequency equal to the conversion rate of the ADC, it can be seen as a resistive path to ground. For instance, assuming a conversion rate of 1 MHz, with  $C_S$  equal to 3 pF, a resistance of 330 kΩ is obtained ( $R_{EQ} = 1 / (f_c * C_S)$ , where  $f_c$  represents the conversion rate at the considered channel). To minimize the error induced by the voltage partitioning between this resistance (sampled voltage on  $C_S$ ) and the sum of  $R_S + R_F + R_L + R_{SW} + R_{AD}$ , the external circuit must be designed to respect the [Equation 4](#):

**Eqn. 4**

$$V_A \cdot \frac{R_S + R_F + R_L + R_{SW} + R_{AD}}{R_{EQ}} < \frac{1}{2} \text{LSB}$$

[Equation 4](#) generates a constraint for external network design, in particular on a resistive path. Internal switch resistances ( $R_{SW}$  and  $R_{AD}$ ) can be neglected with respect to external resistances.

**Figure 18. Input equivalent circuit (precise channels)**

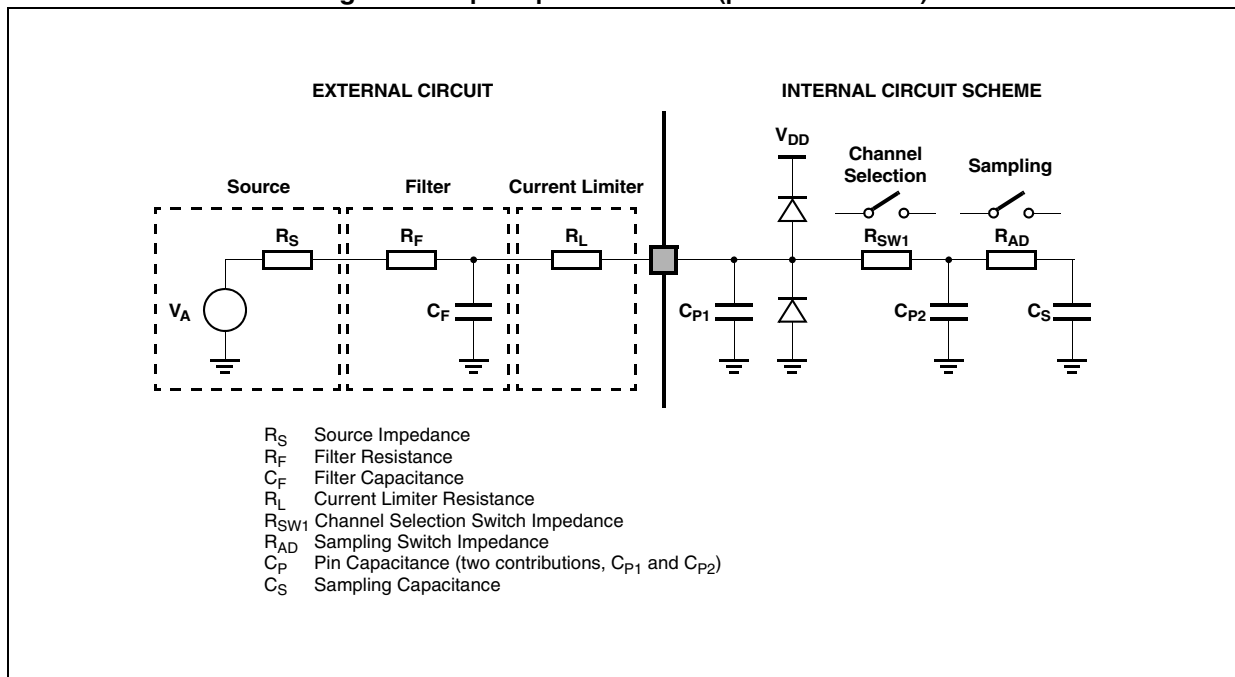
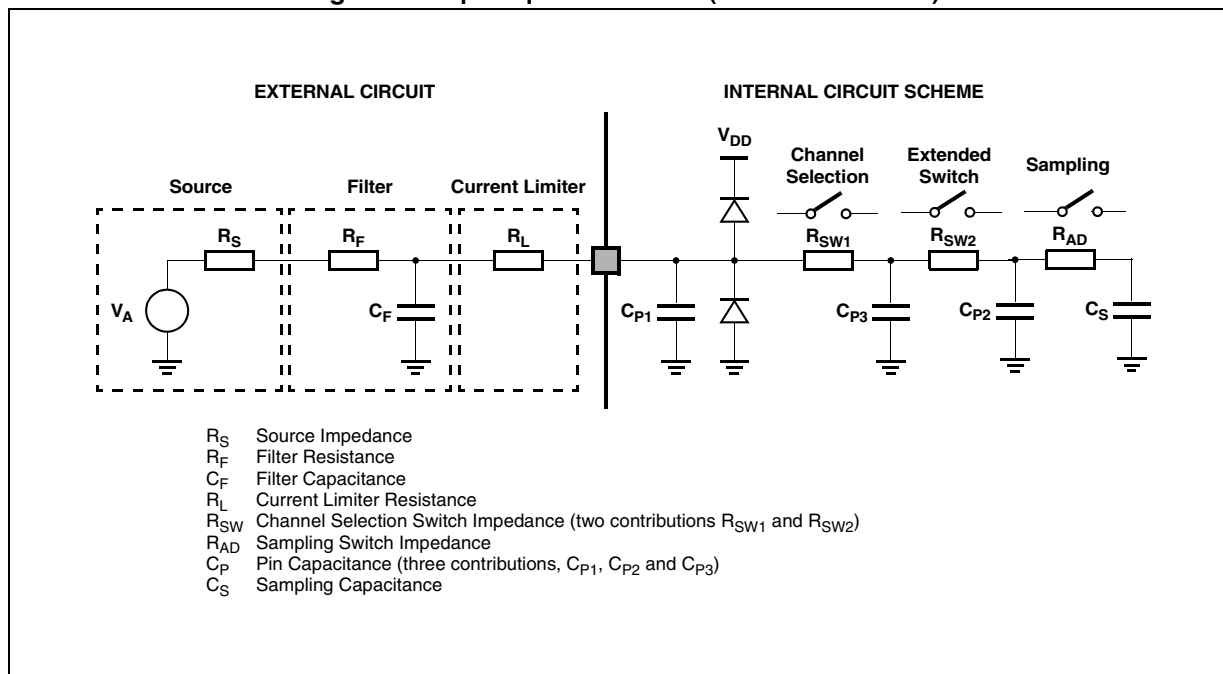
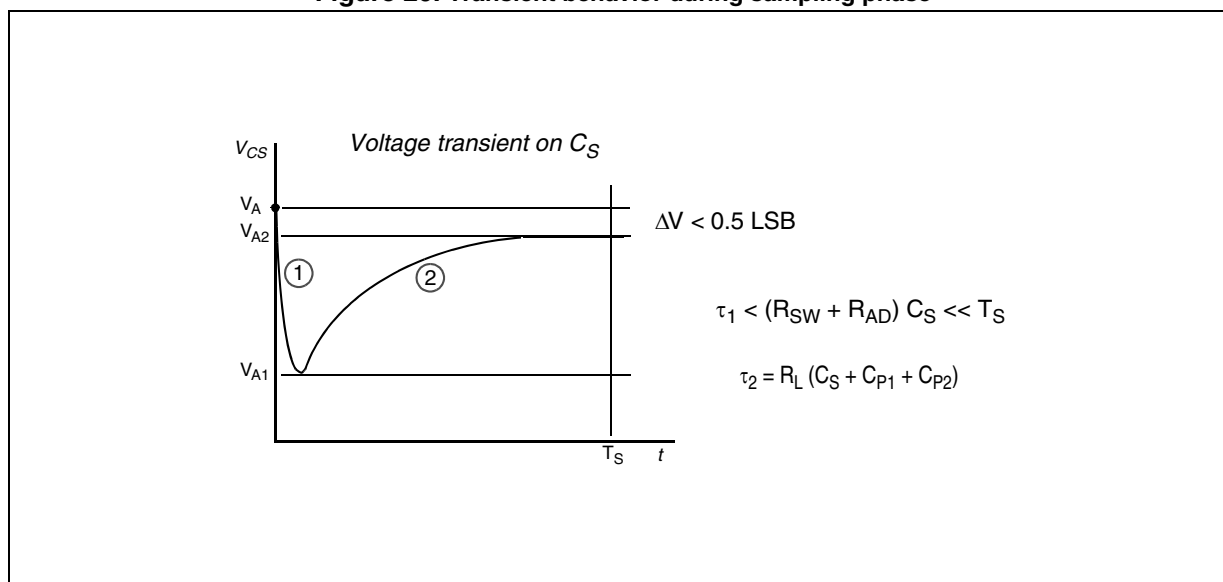


Figure 19. Input equivalent circuit (extended channels)



A second aspect involving the capacitance network shall be considered. Assuming the three capacitances  $C_F$ ,  $C_{P1}$  and  $C_{P2}$  are initially charged at the source voltage  $V_A$  (refer to the equivalent circuit in Figure 18): A charge sharing phenomenon is installed when the sampling phase is started (A/D switch close).

Figure 20. Transient behavior during sampling phase



In particular two different transient periods can be distinguished:

1. A first and quick charge transfer from the internal capacitance  $C_{P1}$  and  $C_{P2}$  to the sampling capacitance  $C_S$  occurs ( $C_S$  is supposed initially completely discharged): considering a worst case (since the time constant in reality would be faster) in which  $C_{P2}$  is reported in parallel to  $C_{P1}$  (call  $C_P = C_{P1} + C_{P2}$ ), the two capacitances  $C_P$  and  $C_S$  are in series, and the time constant is

**Eqn. 5**

$$\tau_1 = (R_{SW} + R_{AD}) \cdot \frac{C_P \cdot C_S}{C_P + C_S}$$

Equation 5 can again be simplified considering only  $C_S$  as an additional worst condition. In reality, the transient is faster, but the A/D converter circuitry has been designed to be robust also in the very worst case: the sampling time  $T_S$  is always much longer than the internal time constant:

**Eqn. 6**

$$\tau_1 < (R_{SW} + R_{AD}) \cdot C_S \ll T_S$$

The charge of  $C_{P1}$  and  $C_{P2}$  is redistributed also on  $C_S$ , determining a new value of the voltage  $V_{A1}$  on the capacitance according to Equation 7:

**Eqn. 7**

$$V_{A1} \cdot (C_S + C_{P1} + C_{P2}) = V_A \cdot (C_{P1} + C_{P2})$$

2. A second charge transfer involves also  $C_F$  (that is typically bigger than the on-chip capacitance) through the resistance  $R_L$ : again considering the worst case in which  $C_{P2}$  and  $C_S$  were in parallel to  $C_{P1}$  (since the time constant in reality would be faster), the time constant is:

**Eqn. 8**

$$\tau_2 < R_L \cdot (C_S + C_{P1} + C_{P2})$$

In this case, the time constant depends on the external circuit: in particular imposing that the transient is completed well before the end of sampling time  $T_S$ , a constraints on  $R_L$  sizing is obtained:

**Eqn. 9**

$$10 \cdot \tau_2 = 10 \cdot R_L \cdot (C_S + C_{P1} + C_{P2}) < T_S$$

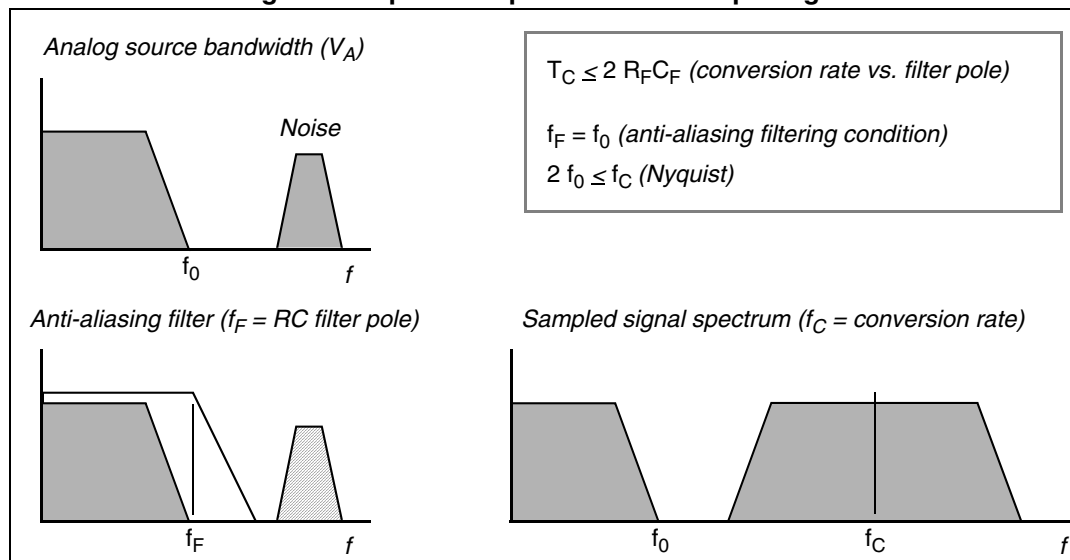
Of course,  $R_L$  shall be sized also according to the current limitation constraints, in combination with  $R_S$  (source impedance) and  $R_F$  (filter resistance). Being  $C_F$  definitively bigger than  $C_{P1}$ ,  $C_{P2}$  and  $C_S$ , then the final voltage  $V_{A2}$  (at the end of the charge transfer transient) will be much higher than  $V_{A1}$ . Equation 10 must be respected (charge balance assuming now  $C_S$  already charged at  $V_{A1}$ ):

**Eqn. 10**

$$V_{A2} \cdot (C_S + C_{P1} + C_{P2} + C_F) = V_A \cdot C_F + V_{A1} \cdot (C_{P1} + C_{P2} + C_S)$$

The two transients above are not influenced by the voltage source that, due to the presence of the  $R_F C_F$  filter, is not able to provide the extra charge to compensate the voltage drop on  $C_S$  with respect to the ideal source  $V_A$ ; the time constant  $R_F C_F$  of the filter is very high with respect to the sampling time ( $T_S$ ). The filter is typically designed to act as anti-aliasing.

Figure 21. Spectral representation of input signal



Calling  $f_0$  the bandwidth of the source signal (and as a consequence the cut-off frequency of the anti-aliasing filter,  $f_F$ ), according to the Nyquist theorem the conversion rate  $f_C$  must be at least  $2f_0$ ; it means that the constant time of the filter is greater than or at least equal to twice the conversion period ( $T_C$ ). Again the conversion period  $T_C$  is longer than the sampling time  $T_S$ , which is just a portion of it, even when fixed channel continuous conversion mode is selected (fastest conversion rate at a specific channel): in conclusion it is evident that the time constant of the filter  $R_F C_F$  is definitively much higher than the sampling time  $T_S$ , so the charge level on  $C_S$  cannot be modified by the analog signal source during the time in which the sampling switch is closed.

The considerations above lead to impose new constraints on the external circuit, to reduce the accuracy error due to the voltage drop on  $C_S$ ; from the two charge balance equations above, it is simple to derive Equation 11 between the ideal and real sampled voltage on  $C_S$ :

Eqn. 11

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when  $V_A$  is maximum, that is for instance 5 V), assuming to accept a maximum error of half a count, a constraint is evident on  $C_F$  value:

Eqn. 12

$$C_F > 2048 \cdot C_S$$

## 4.18.3 ADC electrical characteristics

Table 37. ADC input leakage current

Symbol		C	Parameter	Conditions		Value			Unit
						Min	Typ	Max	
I <sub>LKG</sub>	CC	C	Input leakage current	T <sub>A</sub> = −40 °C	No current injection on adjacent pin	—	1	—	nA
		C	T <sub>A</sub> = 25 °C	—		1	—		
		C	T <sub>A</sub> = 105 °C	—		8	200		
		P	T <sub>A</sub> = 125 °C	—		45	400		

Table 38. ADC conversion characteristics

Symbol		C	Parameter	Conditions <sup>1</sup>	Value			Unit
					Min	Typ	Max	
V <sub>SS_ADC</sub>	SR	—	Voltage on VSS_HV_ADC (ADC reference) pin with respect to ground (V <sub>SS</sub> ) <sup>2</sup>	—	−0.1	—	0.1	V
V <sub>DD_ADC</sub>	SR	—	Voltage on VDD_HV_ADC pin (ADC reference) with respect to ground (V <sub>SS</sub> )	—	V <sub>DD</sub> −0.1	—	V <sub>DD</sub> +0.1	V
V <sub>AINx</sub>	SR	—	Analog input voltage <sup>3</sup>	—	V <sub>SS_ADC</sub> −0.1	—	V <sub>DD_ADC</sub> +0.1	V
f <sub>ADC</sub>	SR	—	ADC analog frequency	—	6	—	32 + 4%	MHz
Δ <sub>ADC_SYS</sub>	SR	—	ADC digital clock duty cycle (ipg_clk)	ADCLKSEL = 1 <sup>4</sup>	45	—	55	%
I <sub>ADCPWD</sub>	SR	—	ADC0 consumption in power down mode	—	—	—	50	μs
I <sub>ADCRUN</sub>	SR	—	ADC0 consumption in running mode	—	—	—	4	ms
t <sub>ADC_PU</sub>	SR	—	ADC power up delay	—	—	—	1.5	μs
t <sub>ADC_S</sub>	CC	T	Sample time <sup>5</sup>	f <sub>ADC</sub> = 32 MHz, INPSAMP = 17	0.5	—		μs
				f <sub>ADC</sub> = 6 MHz, INPSAMP = 255	—	—	42	
t <sub>ADC_C</sub>	CC	P	Conversion time <sup>6</sup>	f <sub>ADC</sub> = 32 MHz, INPCMP = 2	0.625	—		μs
C <sub>S</sub>	CC	D	ADC input sampling capacitance	—	—	—	3	pF
C <sub>P1</sub>	CC	D	ADC input pin capacitance 1	—	—	—	3	pF



Table 38. ADC conversion characteristics (continued)

Symbol	C	D	Parameter	Conditions <sup>1</sup>	Value			Unit
					Min	Typ	Max	
C <sub>P2</sub>	CC	D	ADC input pin capacitance 2	—	—	—	1	pF
C <sub>P3</sub>	CC	D	ADC input pin capacitance 3	—	—	—	1	pF
R <sub>SW1</sub>	CC	D	Internal resistance of analog source	—	—	—	3	kΩ
R <sub>SW2</sub>	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
R <sub>AD</sub>	CC	D	Internal resistance of analog source	—	—	—	2	kΩ
I <sub>INJ</sub>	SR	—	Input current Injection	Current injection on one ADC input, different from the converted one	V <sub>DD</sub> = 3.3 V ± 10%	—	5	mA
					V <sub>DD</sub> = 5.0 V ± 10%	—	5	
INL	CC	T	Absolute value for integral non-linearity	No overload	—	0.5	1.5	LSB
DNL	CC	T	Absolute differential non-linearity	No overload	—	0.5	1.0	LSB
OFS	CC	T	Absolute offset error	—	—	0.5	—	LSB
GNE	CC	T	Absolute gain error	—	—	0.6	—	LSB
TUE <sub>p</sub>	CC	P	Total unadjusted error <sup>7</sup> for precise channels, input only pins	Without current injection	–2	0.6	2	LSB
		T		With current injection	–3		3	
TUE <sub>x</sub>	CC	T	Total unadjusted error <sup>7</sup> for extended channel	Without current injection	–3	1	3	LSB
		T		With current injection	–4		4	

<sup>1</sup> V<sub>DD</sub> = 3.3 V ± 10% / 5.0 V ± 10%, T<sub>A</sub> = –40 to 125 °C, unless otherwise specified.

<sup>2</sup> Analog and digital V<sub>SS</sub> **must** be common (to be tied together externally).

<sup>3</sup> V<sub>AINx</sub> may exceed V<sub>SS\_ADC</sub> and V<sub>DD\_ADC</sub> limits, remaining on absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

<sup>4</sup> Duty cycle is ensured by using system clock without prescaling. When ADCLKSEL = 0, the duty cycle is ensured by internal divider by 2.

<sup>5</sup> During the sample time the input capacitance C<sub>S</sub> can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t<sub>ADC\_S</sub>. After the end of the sample time t<sub>ADC\_S</sub>, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t<sub>ADC\_S</sub> depend on programming.

<sup>6</sup> This parameter does not include the sample time t<sub>ADC\_S</sub>, but only the time for determining the digital result and the time to load the result's register with the conversion result.

<sup>7</sup> Total Unadjusted Error: The maximum error that occurs without adjusting Offset and Gain errors. This error is a combination of Offset, Gain and Integral Linearity errors.

## 4.19 On-chip peripherals

### 4.19.1 Current consumption

Table 39. On-chip peripherals current consumption<sup>1</sup>

Symbol		C	Parameter	Conditions		Value	Unit
						Typ	
I <sub>DD_BV</sub> (CAN)	CC	T	CAN (FlexCAN) supply current on V <sub>DD_BV</sub>	500 Kbps	Total (static + dynamic) consumption: <ul style="list-style-type: none"><li>FlexCAN in loop-back mode</li><li>XTAL @ 8MHz used as CAN engine clock source</li><li>Message sending period is 580 μs</li></ul>	8 * f <sub>periph</sub> + 85	μA
				125 Kbps		8 * f <sub>periph</sub> + 27	
I <sub>DD_BV</sub> (eMIOS)	CC	T	eMIOS supply current on V <sub>DD_BV</sub>	Static consumption: <ul style="list-style-type: none"><li>eMIOS channel OFF</li><li>Global prescaler enabled</li></ul>		29 * f <sub>periph</sub>	
				Dynamic consumption: <ul style="list-style-type: none"><li>It does not change varying the frequency (0.003 mA)</li></ul>		3	
I <sub>DD_BV</sub> (SCI)	CC	T	SCI (LINFlex) supply current on V <sub>DD_BV</sub>	Total (static + dynamic) consumption: <ul style="list-style-type: none"><li>LIN mode</li><li>Baudrate: 20 Kbps</li></ul>		5 * f <sub>periph</sub> + 31	
I <sub>DD_BV</sub> (SPI)	CC	T	SPI (DSPI) supply current on V <sub>DD_BV</sub>	Ballast static consumption (only clocked)		1	
				Ballast dynamic consumption (continuous communication): <ul style="list-style-type: none"><li>Baudrate: 2 Mbit</li><li>Trasmission every 8 μs</li><li>Frame: 16 bits</li></ul>		16 * f <sub>periph</sub>	

Table 39. On-chip peripherals current consumption<sup>1</sup> (continued)

Symbol	C	Parameter	Conditions		Value	Unit
					Typ	
I <sub>DD_BV(ADC)</sub>	CC	ADC supply current on V <sub>DD_BV</sub>	V <sub>DD</sub> = 5.5 V	Ballast static consumption (no conversion)	41 * f <sub>periph</sub>	μA
			V <sub>DD</sub> = 5.5 V	Ballast dynamic consumption (continuous conversion)	5 * f <sub>periph</sub>	
I <sub>DD_HV_ADC(ADC)</sub>	CC	ADC supply current on V <sub>DD_HV_ADC</sub>	V <sub>DD</sub> = 5.5 V	Analog static consumption (no conversion)	2 * f <sub>periph</sub>	
			V <sub>DD</sub> = 5.5 V	Analog dynamic consumption (continuous conversion)	75 * f <sub>periph</sub> + 32	
I <sub>DD_HV(FLASH)</sub>	CC	T CFlash + DFlash supply current on V <sub>DD_HV_ADC</sub>	V <sub>DD</sub> = 5.5 V	—	8.21	mA
I <sub>DD_HV(PLL)</sub>	CC	T PLL supply current on V <sub>DD_HV</sub>	V <sub>DD</sub> = 5.5 V	—	3 * f <sub>periph</sub>	μA

<sup>1</sup> Operating conditions: T<sub>A</sub> = 25 °C, f<sub>periph</sub> = 8 MHz to 64 MHz

## 4.19.2 DSPI characteristics

Table 40. DSPI characteristics<sup>1</sup>

No.	Symbol	C		Parameter		DSPI0/DSPI1			DSPI2			Unit
						Min	Typ	Max	Min	Typ	Max	
1	t <sub>SCK</sub>	SR	D	SCK cycle time	Master mode (MTFE = 0)	125	—	—	333	—	—	ns
			D		Slave mode (MTFE = 0)	125	—	—	333	—	—	
			D		Master mode (MTFE = 1)	83	—	—	125	—	—	
			D		Slave mode (MTFE = 1)	83	—	—	125	—	—	
—	f <sub>DSPI</sub>	SR	D	DSPI digital controller frequency		—	—	f <sub>CPU</sub>	—	—	f <sub>CPU</sub>	MHz
—	Δt <sub>CSC</sub>	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->0	Master mode	—	—	130 <sup>2</sup>	—	—	15 <sup>3</sup>	ns
—	Δt <sub>ASC</sub>	CC	D	Internal delay between pad associated to SCK and pad associated to CSn in master mode for CSn1->1	Master mode	—	—	130 <sup>3</sup>	—	—	130 <sup>3</sup>	ns
2	t <sub>CSCext</sub> <sup>4</sup>	SR	D	CS to SCK delay	Slave mode	32	—	—	32	—	—	ns
3	t <sub>ASCext</sub> <sup>5</sup>	SR	D	After SCK delay	Slave mode	1/f <sub>DSPI</sub> + 5	—	—	1/f <sub>DSPI</sub> + 5	—	—	ns
4	t <sub>SDC</sub>	CC	D	SCK duty cycle	Master mode	—	t <sub>SCK</sub> /2	—	—	t <sub>SCK</sub> /2	—	ns
		SR	D		Slave mode	t <sub>SCK</sub> /2	—	—	t <sub>SCK</sub> /2	—	—	
5	t <sub>A</sub>	SR	D	Slave access time	Slave mode	—	—	1/f <sub>DSPI</sub> + 70	—	—	1/f <sub>DSPI</sub> + 130	ns
6	t <sub>DI</sub>	SR	D	Slave SOUT disable time	Slave mode	7	—	—	7	—	—	ns
9	t <sub>SUI</sub>	SR	D	Data setup time for inputs	Master mode	43	—	—	145	—	—	ns
					Slave mode	5	—	—	5	—	—	
10	t <sub>HI</sub>	SR	D	Data hold time for inputs	Master mode	0	—	—	0	—	—	ns
					Slave mode	2 <sup>6</sup>	—	—	2 <sup>6</sup>	—	—	

Because of an order from the United States International Trade Commission, BGA-packaged product lines and part numbers indicated here currently are not available from Freescale for import or sale in the United States prior to September 2010: MPC5604BxMG products in 208 MAPBGA packages

Table 40. DSPI characteristics<sup>1</sup> (continued)

No.	Symbol	C	D	Parameter		DSPI0/DSPI1			DSPI2			Unit
						Min	Typ	Max	Min	Typ	Max	
11	$t_{\text{SUO}}^7$	CC	D	Data valid after SCK edge	Master mode	—	—	32	—	—	50	ns
				Slave mode	—	—	52	—	—	160		
12	$t_{\text{HO}}^7$	CC	D	Data hold time for outputs	Master mode	0	—	—	0	—	—	ns
				Slave mode	8	—	—	13	—	—		

<sup>1</sup> Operating conditions:  $C_{out} = 10$  to  $50$  pF,  $Slew_{IN} = 3.5$  to  $15$  ns.

<sup>2</sup> Maximum value is reached when CSn pad is configured as SLOW pad while SCK pad is configured as MEDIUM. A positive value means that SCK starts before CSn is asserted. DSPI2 has only SLOW SCK available.

<sup>3</sup> Maximum value is reached when CSn pad is configured as MEDIUM pad while SCK pad is configured as SLOW. A positive value means that CSn is deasserted before SCK. DSPI0 and DSPI1 have only MEDIUM SCK available.

<sup>4</sup> The  $t_{CSC}$  delay value is configurable through a register. When configuring  $t_{CSC}$  (using PCSSCK and CSSCK fields in DSPI\_CTARx registers), delay between internal CS and internal SCK must be higher than  $\Delta t_{CSC}$  to ensure positive  $t_{CSC_{ext}}$ .

<sup>5</sup> The  $t_{ASC}$  delay value is configurable through a register. When configuring  $t_{ASC}$  (using PASC and ASC fields in DSPI\_CTARx registers), delay between internal CS and internal SCK must be higher than  $\Delta t_{ASC}$  to ensure positive  $t_{ASC_{ext}}$ .

<sup>6</sup> This delay value corresponds to SMPL\_PT = 00b which is bit field 9 and 8 of DSPI\_MCR register.

<sup>7</sup> SCK and SOUT configured as MEDIUM pad

Figure 22. DSPI classic SPI timing – master, CPHA = 0

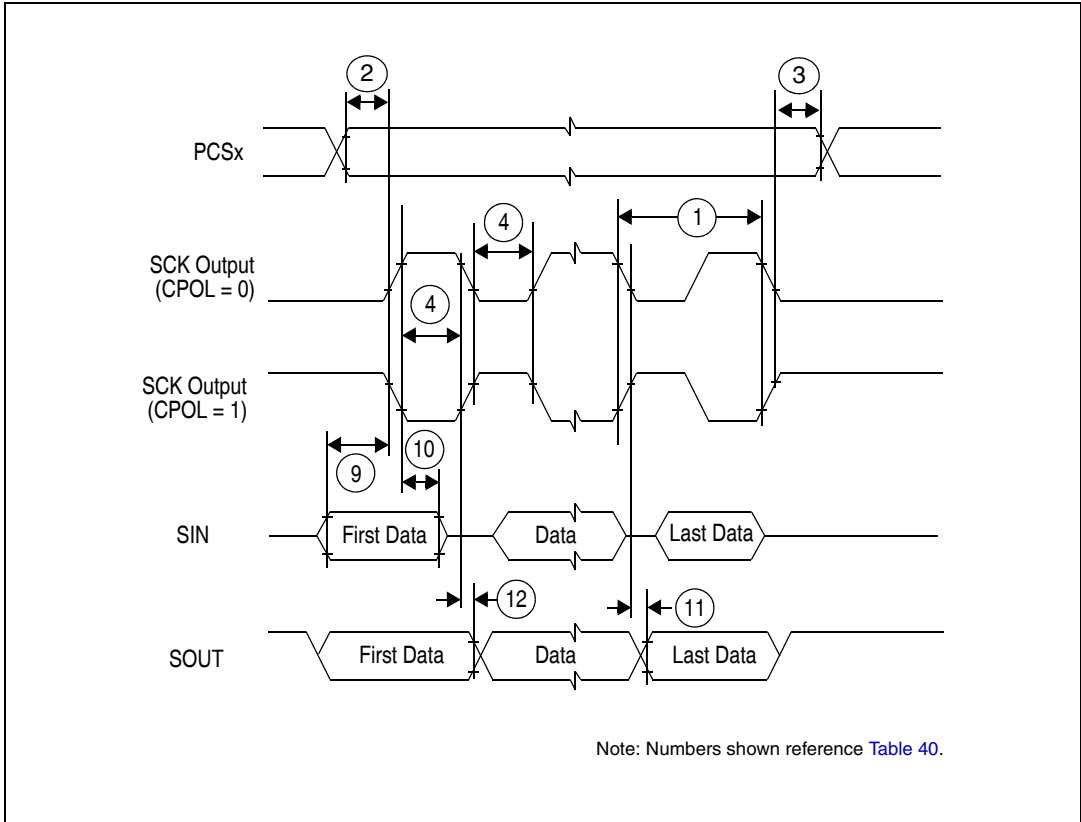


Figure 23. DSPI classic SPI timing – master, CPHA = 1

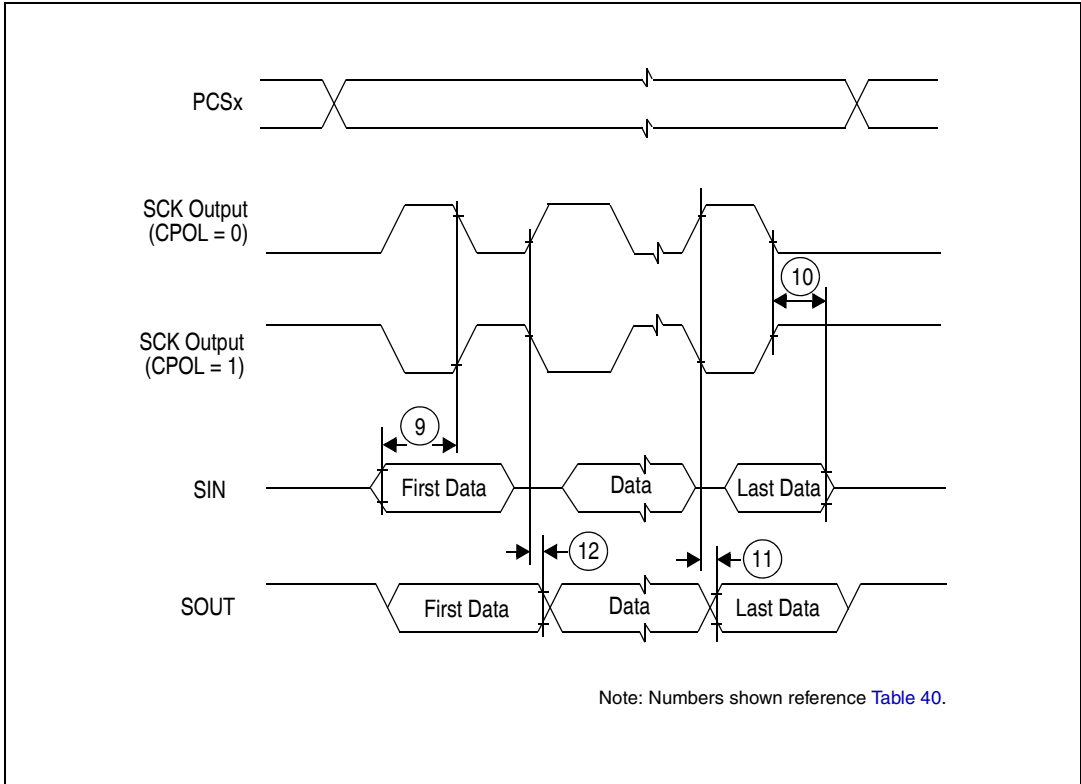


Figure 24. DSPI classic SPI timing – slave, CPHA = 0

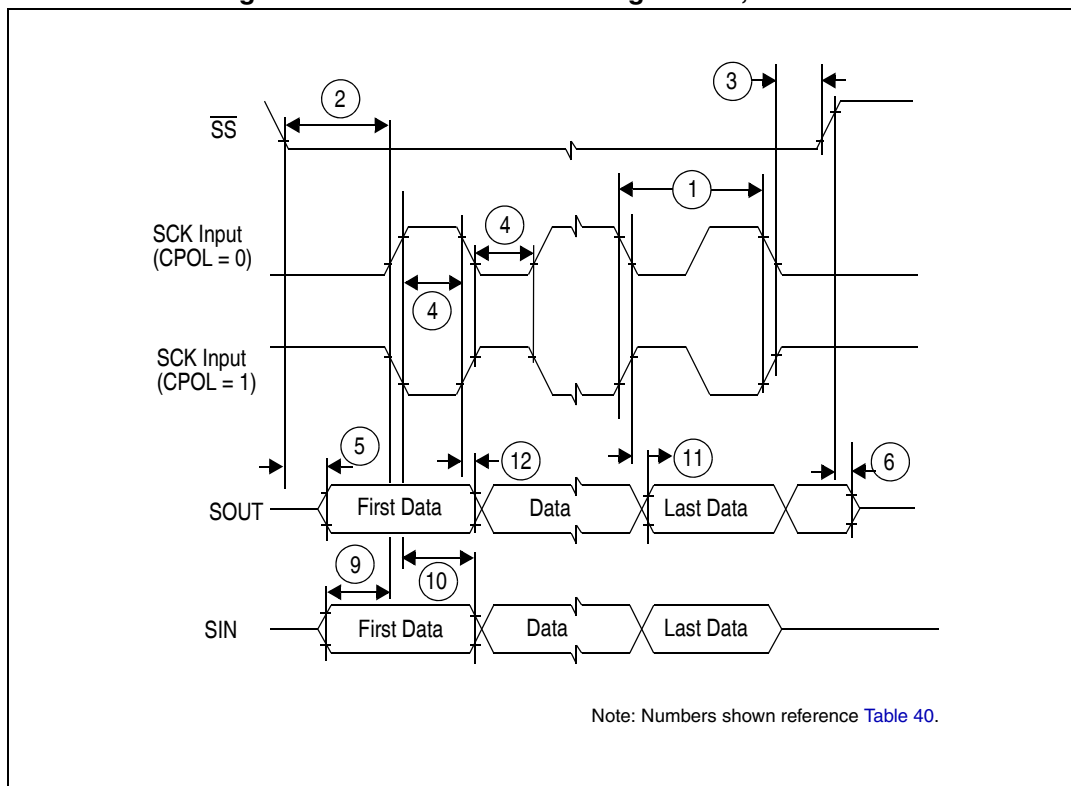


Figure 25. DSPI classic SPI timing – slave, CPHA = 1

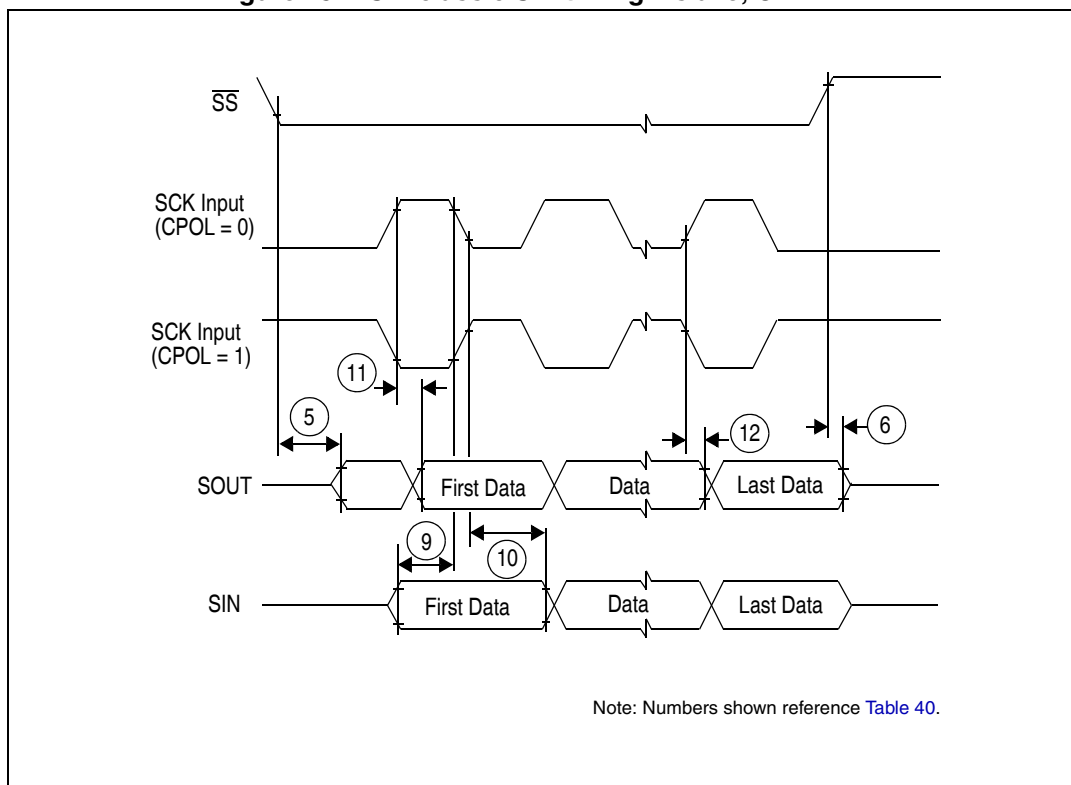


Figure 26. DSPI modified transfer format timing – master, CPHA = 0

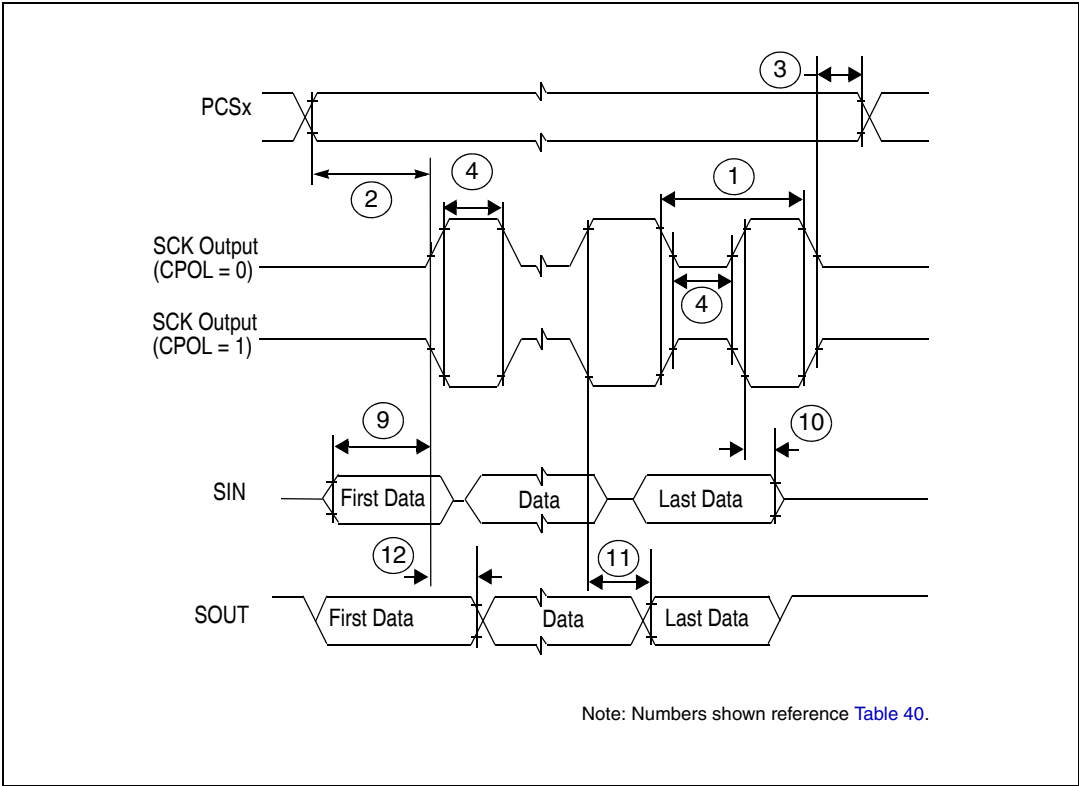
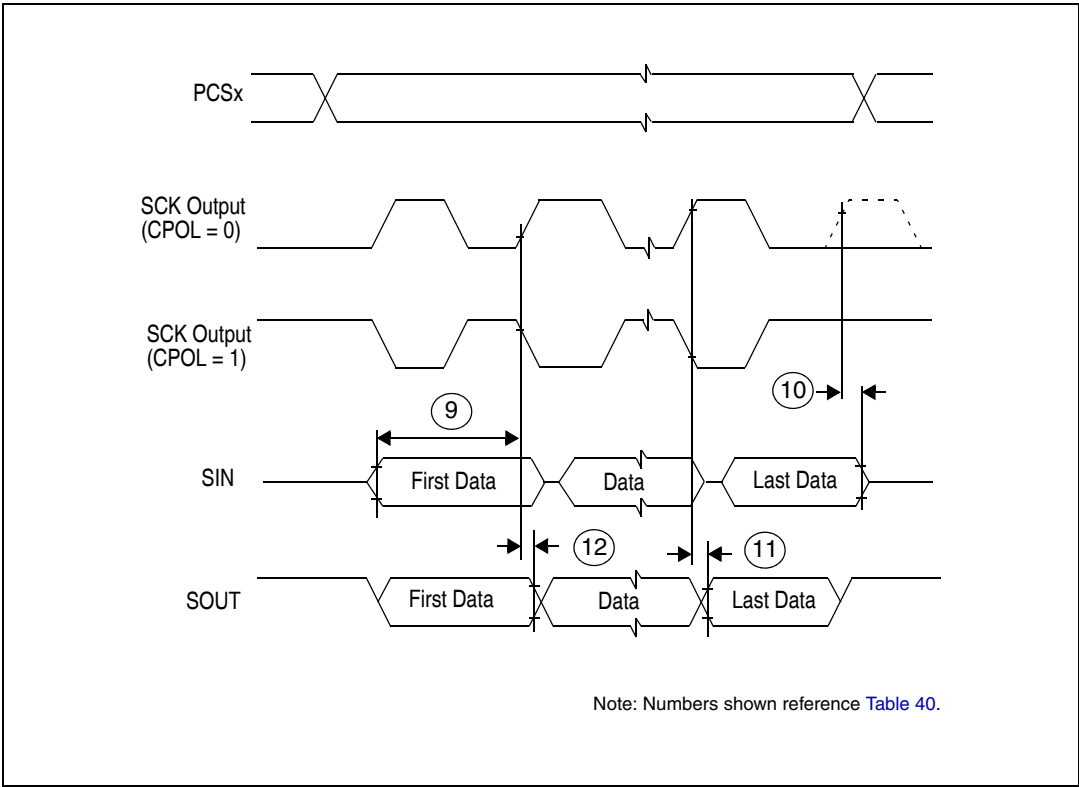
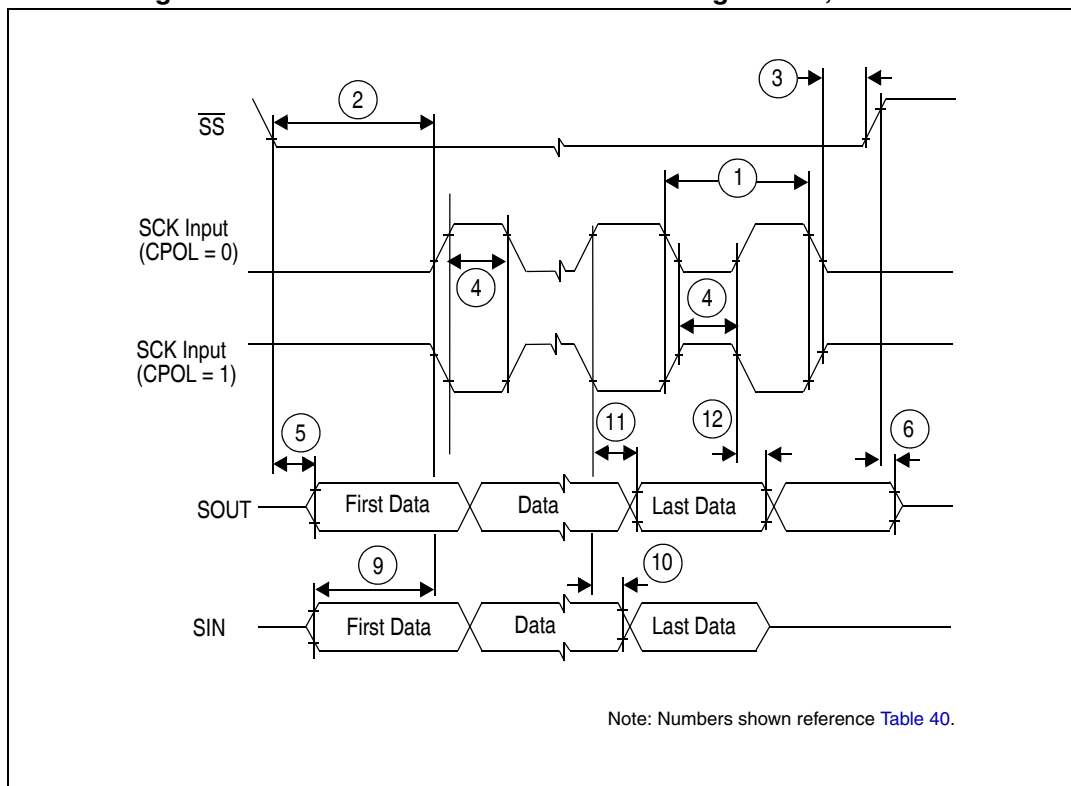
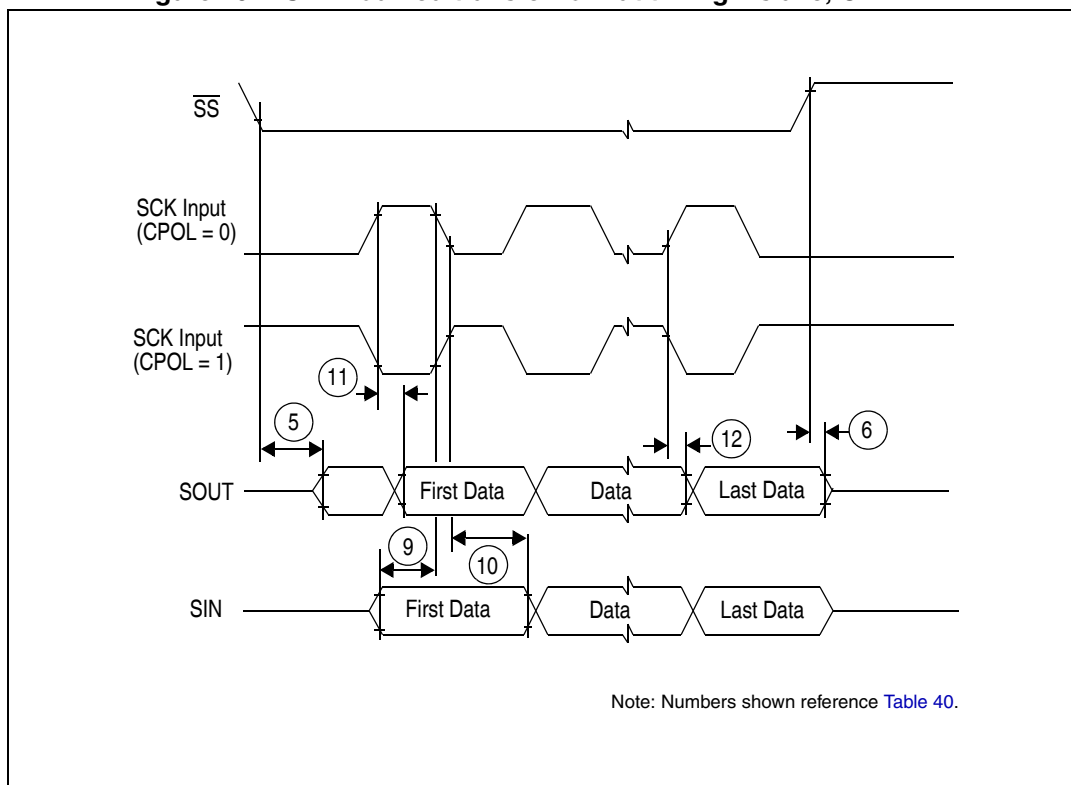


Figure 27. DSPI modified transfer format timing – master, CPHA = 1





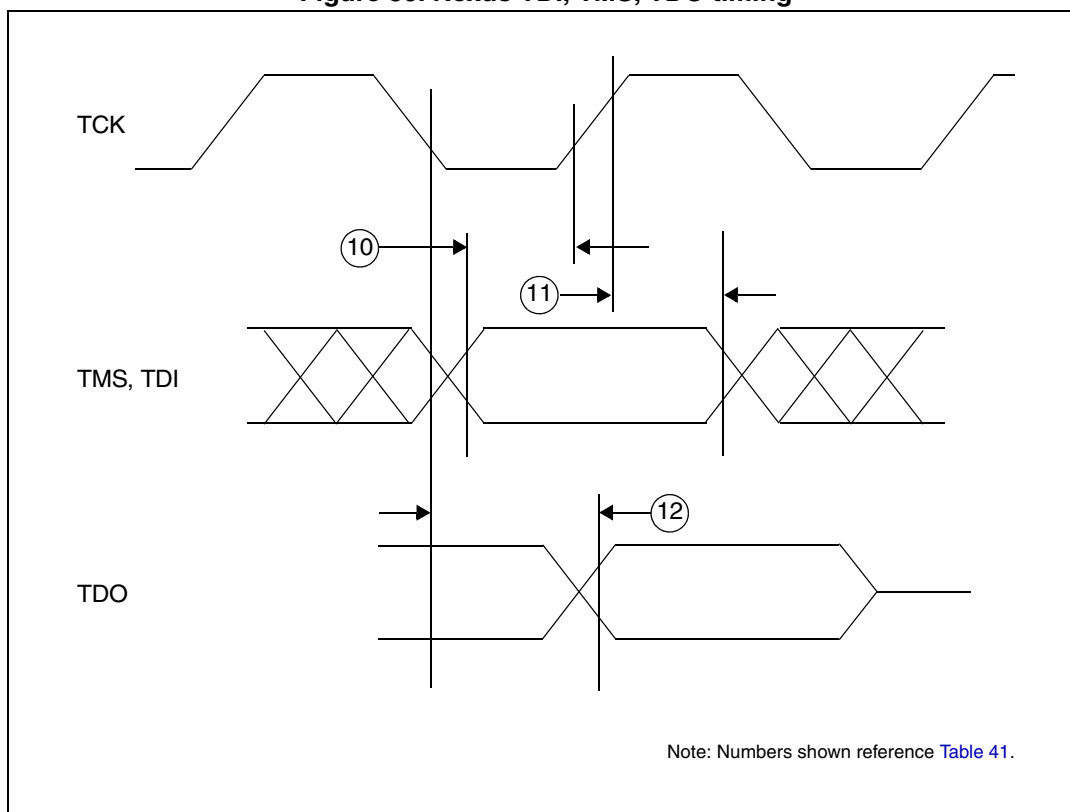
**Figure 28. DSPI modified transfer format timing – slave, CPHA = 0****Figure 29. DSPI modified transfer format timing – slave, CPHA = 1**

### 4.19.3 Nexus characteristics

Table 41. Nexus characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t <sub>TCYC</sub>	CC	D	TCK cycle time	64	—	—	ns
2	t <sub>MCYC</sub>	CC	D	MCKO cycle time	32	—	—	ns
3	t <sub>MDOV</sub>	CC	D	MCKO low to MDO data valid	—	—	8	ns
4	t <sub>MSEOV</sub>	CC	D	MCKO low to MSEO_b data valid	—	—	8	ns
5	t <sub>EVTOV</sub>	CC	D	MCKO low to EVTO data valid	—	—	8	ns
10	t <sub>NTDIS</sub>	CC	D	TDI data setup time	15	—	—	ns
	t <sub>NTMSS</sub>	CC	D	TMS data setup time	15	—	—	ns
11	t <sub>NTDIH</sub>	CC	D	TDI data hold time	5	—	—	ns
	t <sub>NTMSH</sub>	CC	D	TMS data hold time	5	—	—	ns
12	t <sub>TDOV</sub>	CC	D	TCK low to TDO data valid	35	—	—	ns
13	t <sub>TDOI</sub>	CC	D	TCK low to TDO data invalid	6	—	—	ns

Figure 30. Nexus TDI, TMS, TDO timing

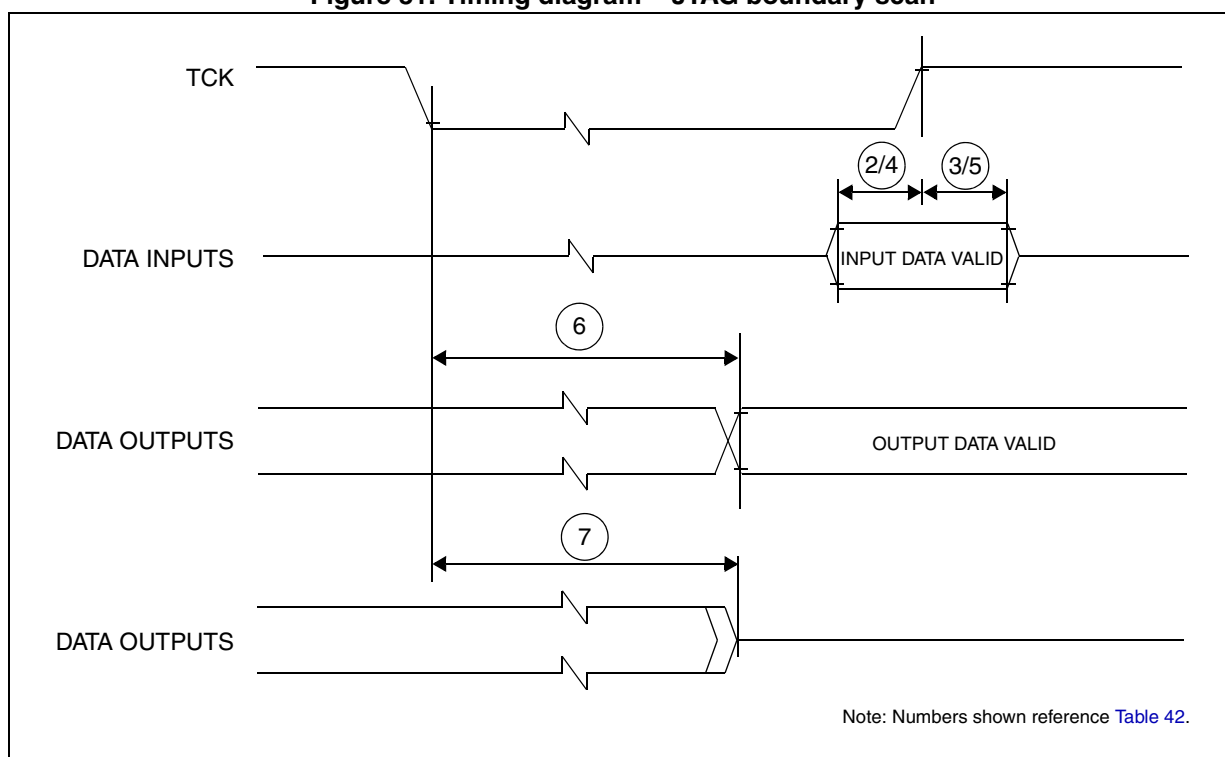


## 4.19.4 JTAG characteristics

Table 42. JTAG characteristics

No.	Symbol		C	Parameter	Value			Unit
					Min	Typ	Max	
1	t <sub>JCYC</sub>	CC	D	TCK cycle time	64	—	—	ns
2	t <sub>TDIS</sub>	CC	D	TDI setup time	15	—	—	ns
3	t <sub>TDIH</sub>	CC	D	TDI hold time	5	—	—	ns
4	t <sub>TMSS</sub>	CC	D	TMS setup time	15	—	—	ns
5	t <sub>TMSh</sub>	CC	D	TMS hold time	5	—	—	ns
6	t <sub>TDOV</sub>	CC	D	TCK low to TDO valid	—	—	33	ns
7	t <sub>TDOI</sub>	CC	D	TCK low to TDO invalid	6	—	—	ns

Figure 31. Timing diagram – JTAG boundary scan



## 5 Package characteristics

### 5.1 Package mechanical data

5.1.1 64 LQFP

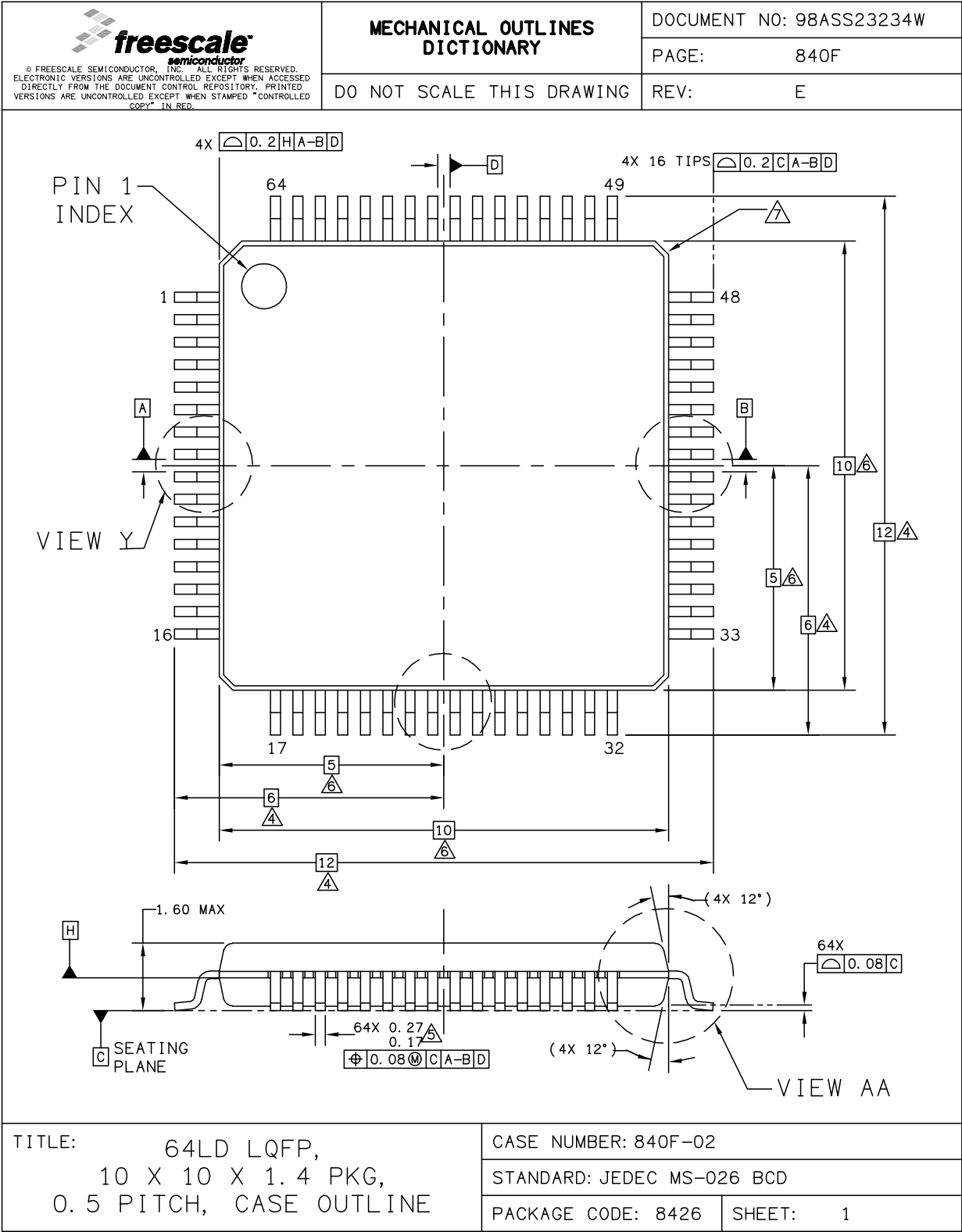


Figure 32. 64 LQFP package mechanical drawing (1 of 3)

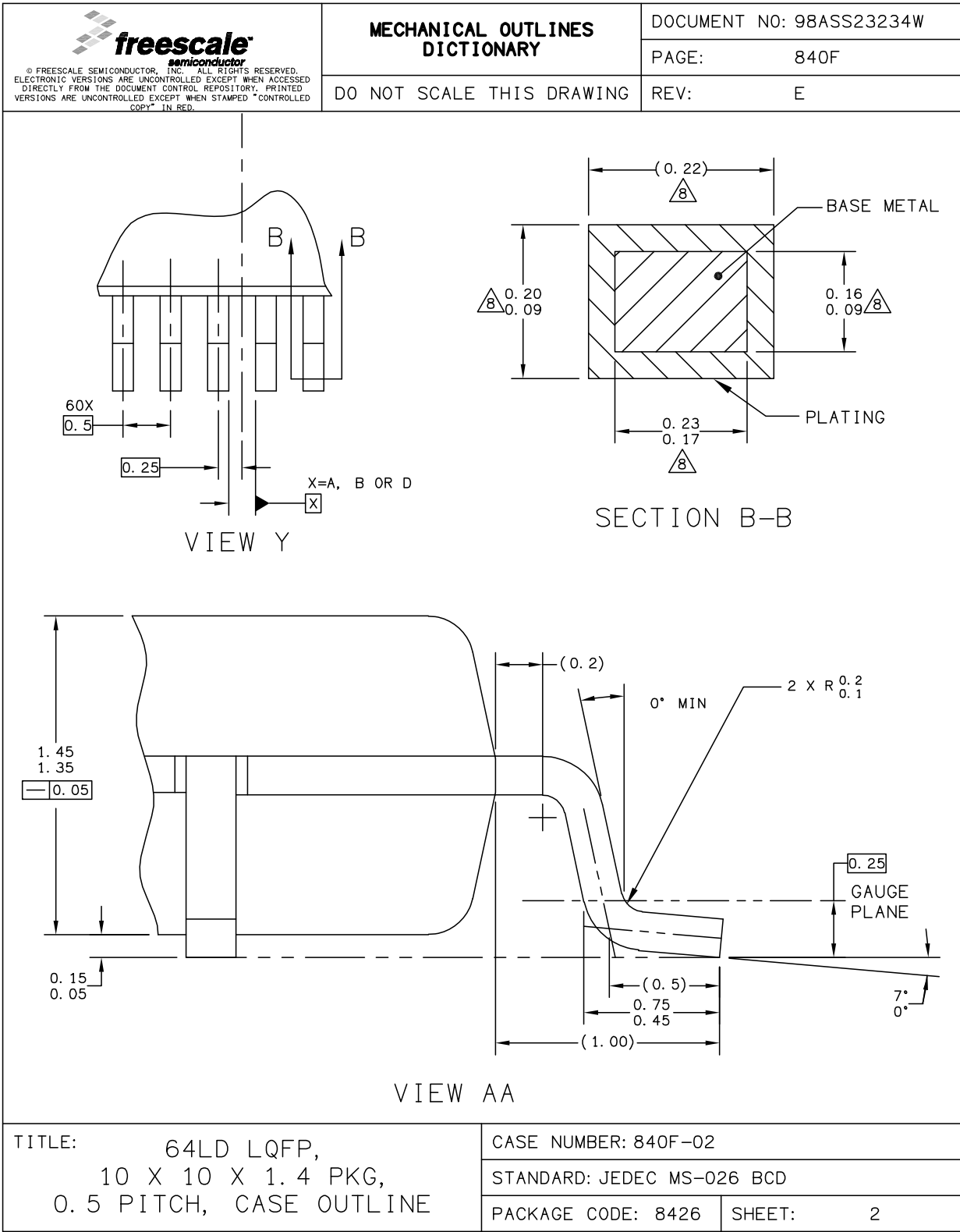



Figure 33. 64 LQFP package mechanical drawing (2 of 3)

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	DO NOT SCALE THIS DRAWING		PAGE: 840F							
			REV: E							
<p>NOTES:</p> <ol style="list-style-type: none"> <li>1. DIMENSIONS ARE IN MILLIMETERS.</li> <li>2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.</li> <li>3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.</li> <li>4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.</li> <li>5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.</li> <li>6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.</li> <li>7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.</li> <li>8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.</li> </ol>										
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE		<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td colspan="2" style="padding: 2px;">CASE NUMBER: 840F-02</td> </tr> <tr> <td colspan="2" style="padding: 2px;">STANDARD: JEDEC MS-026 BCD</td> </tr> <tr> <td style="padding: 2px;">PACKAGE CODE: 8426</td> <td style="padding: 2px;">SHEET: 3</td> </tr> </table>			CASE NUMBER: 840F-02		STANDARD: JEDEC MS-026 BCD		PACKAGE CODE: 8426	SHEET: 3
CASE NUMBER: 840F-02										
STANDARD: JEDEC MS-026 BCD										
PACKAGE CODE: 8426	SHEET: 3									

**Figure 34. 64 LQFP package mechanical drawing (3 of 3)**

5.1.2 100 LQFP

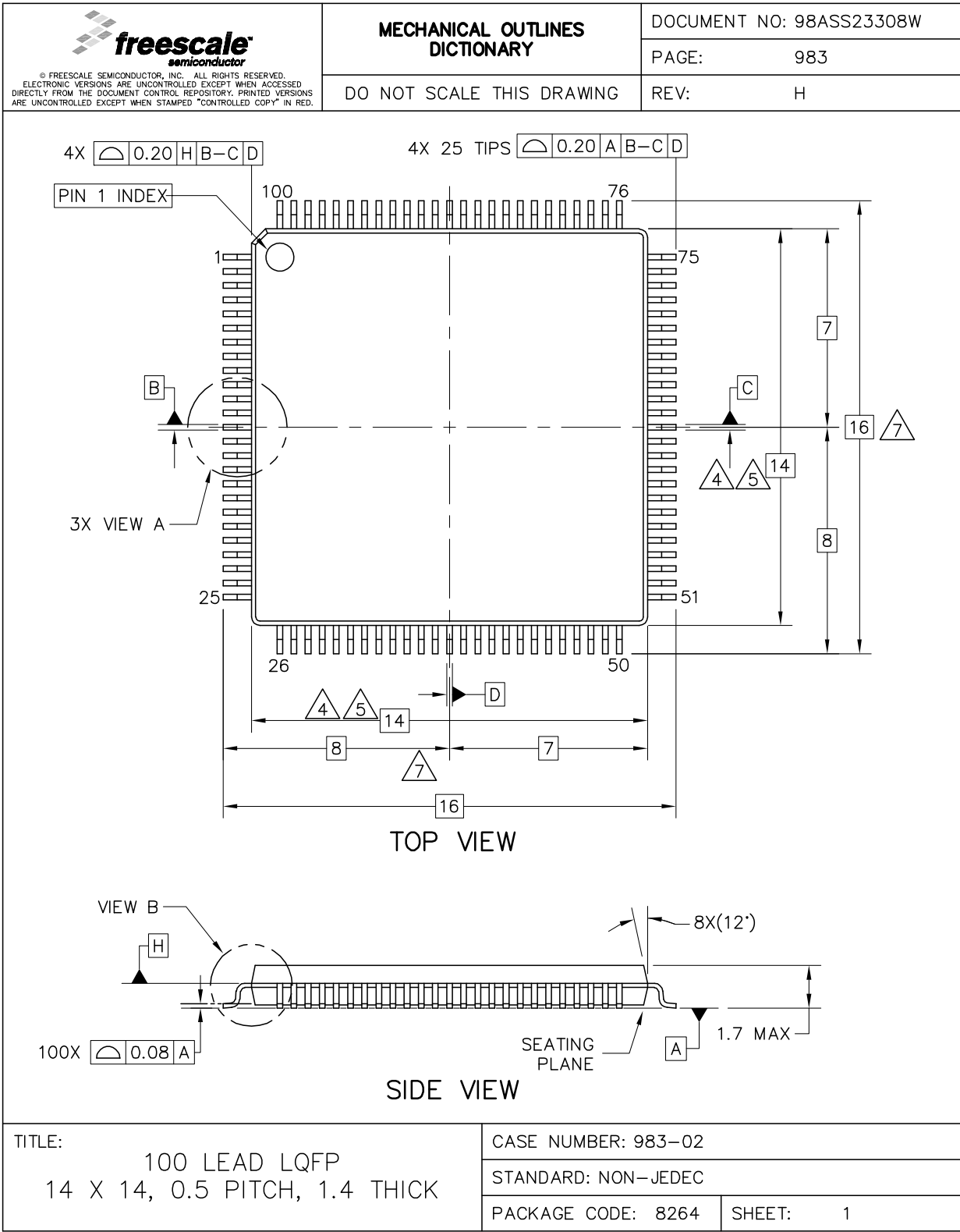


Figure 35. 100 LQFP package mechanical drawing (1 of 3)



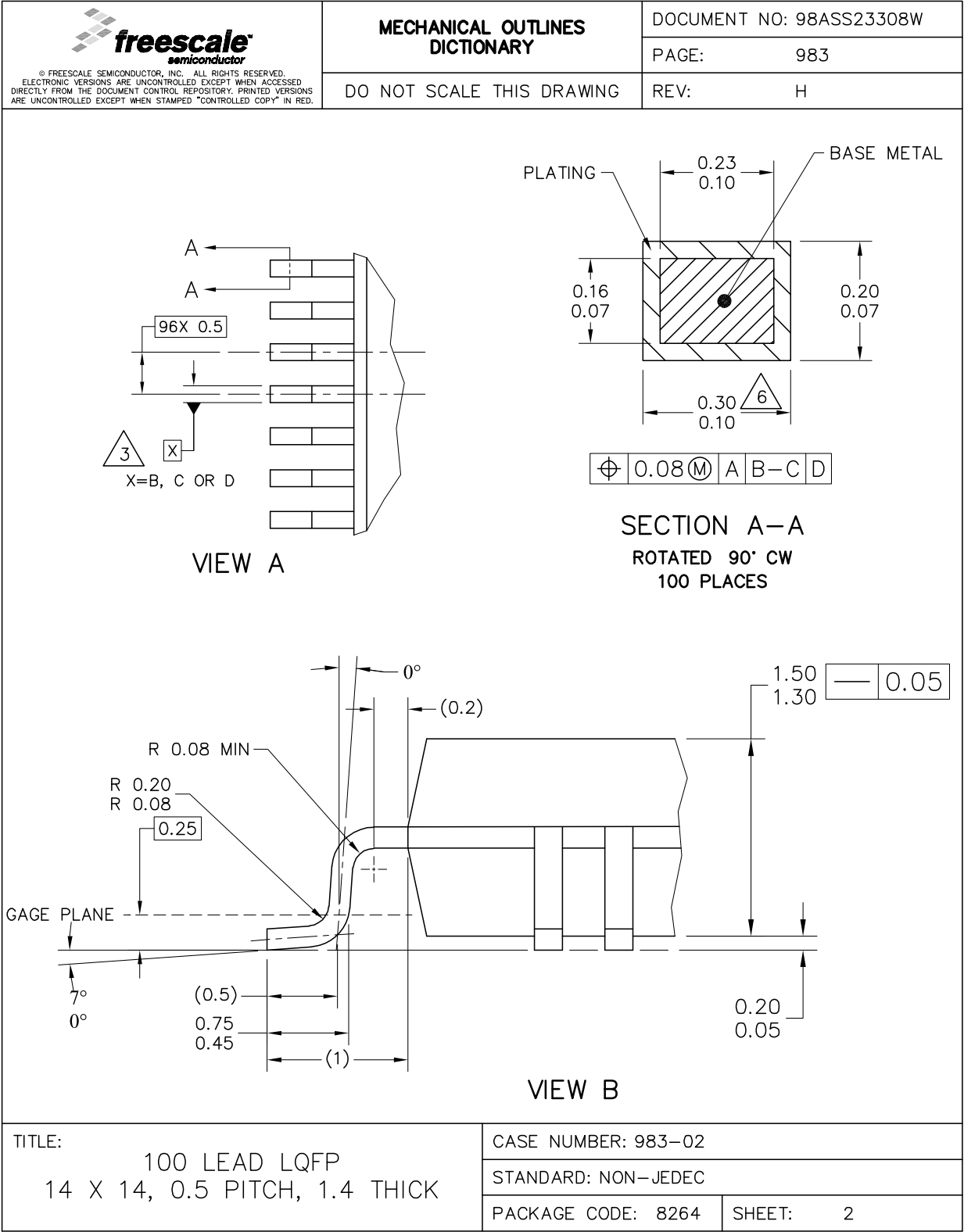


Figure 36. 100 LQFP package mechanical drawing (2 of 3)


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		PAGE:	983
	DO NOT SCALE THIS DRAWING	REV:	H
<p>NOTES:</p> <ol style="list-style-type: none"> <li>1. ALL DIMENSIONS ARE IN MILLIMETERS.</li> <li>2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.</li> <li>3. DATUMS B, C AND D TO BE DETERMINED AT DATUM PLANE H.</li> <li>4. THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE SIZE BY A MAXIMUM OF 0.1 MM.</li> <li>5. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSIONS. THE MAXIMUM ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THE DIMENSIONS ARE MAXIMUM BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.</li> <li>6. DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION. PROTRUSIONS SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.35. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD SHALL BE 0.07 MM.</li> <li>7. DIMENSIONS ARE DETERMINED AT THE SEATING PLANE, DATUM A.</li> </ol>			
TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK		CASE NUMBER: 983–02	
		STANDARD: NON–JEDEC	
		PACKAGE CODE: 8264	SHEET: 3

Figure 37. 100 LQFP package mechanical drawing (3 of 3)

5.1.3 144 LQFP

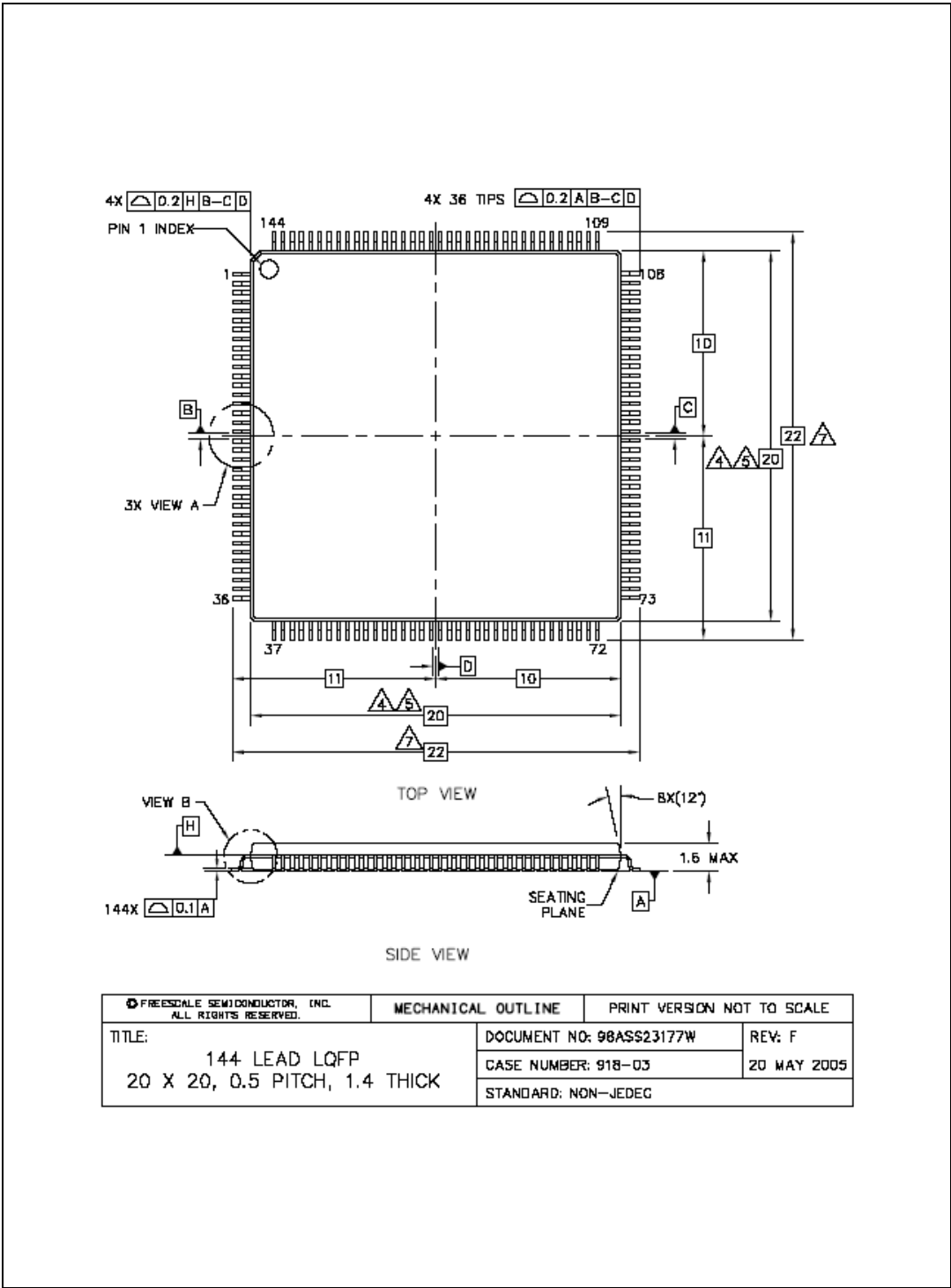


Figure 38. 144 LQFP package mechanical drawing (1 of 2)

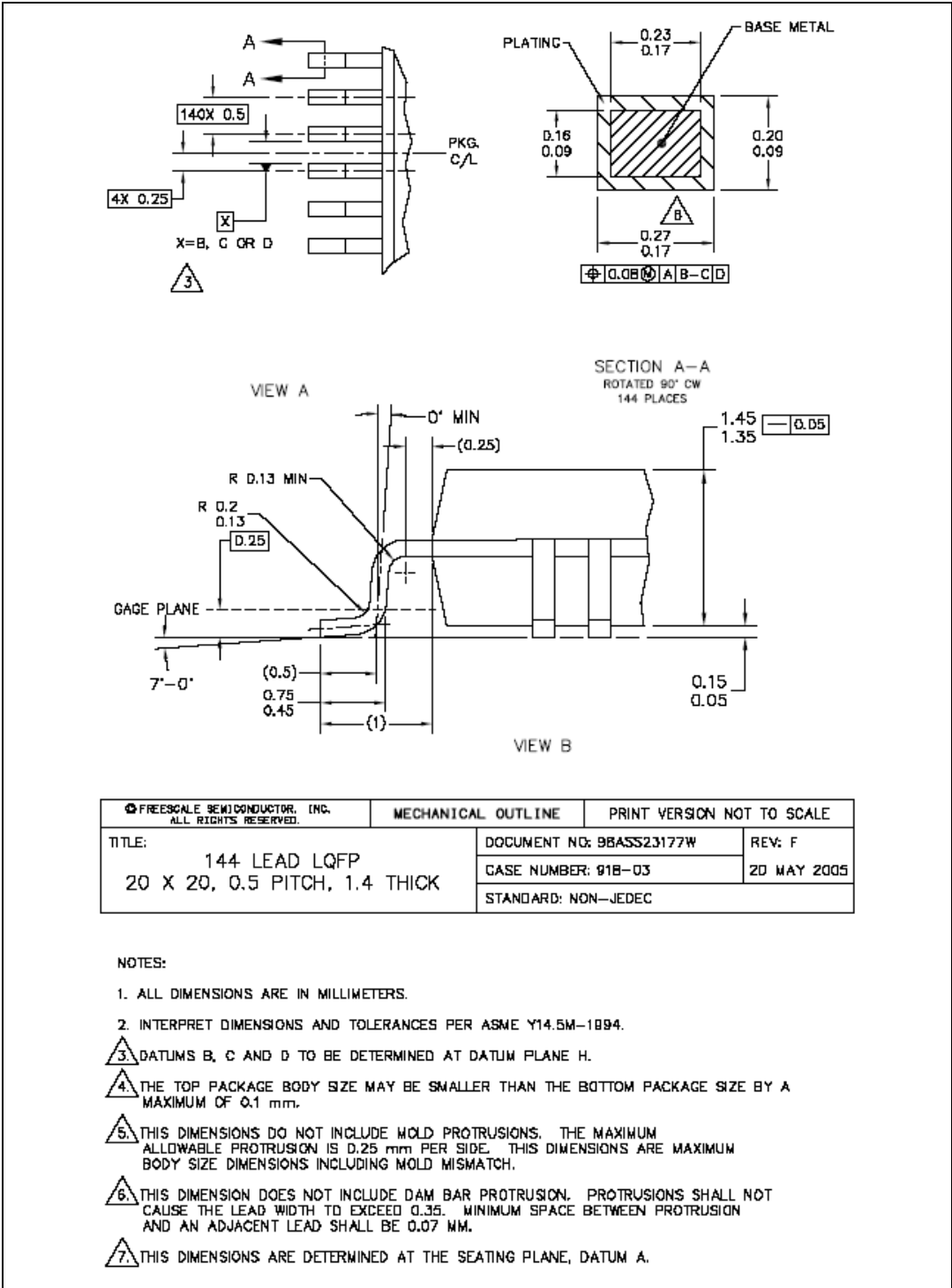


Figure 39. 144 LQFP package mechanical drawing (2 of 2)

5.1.4 208 MAPBGA

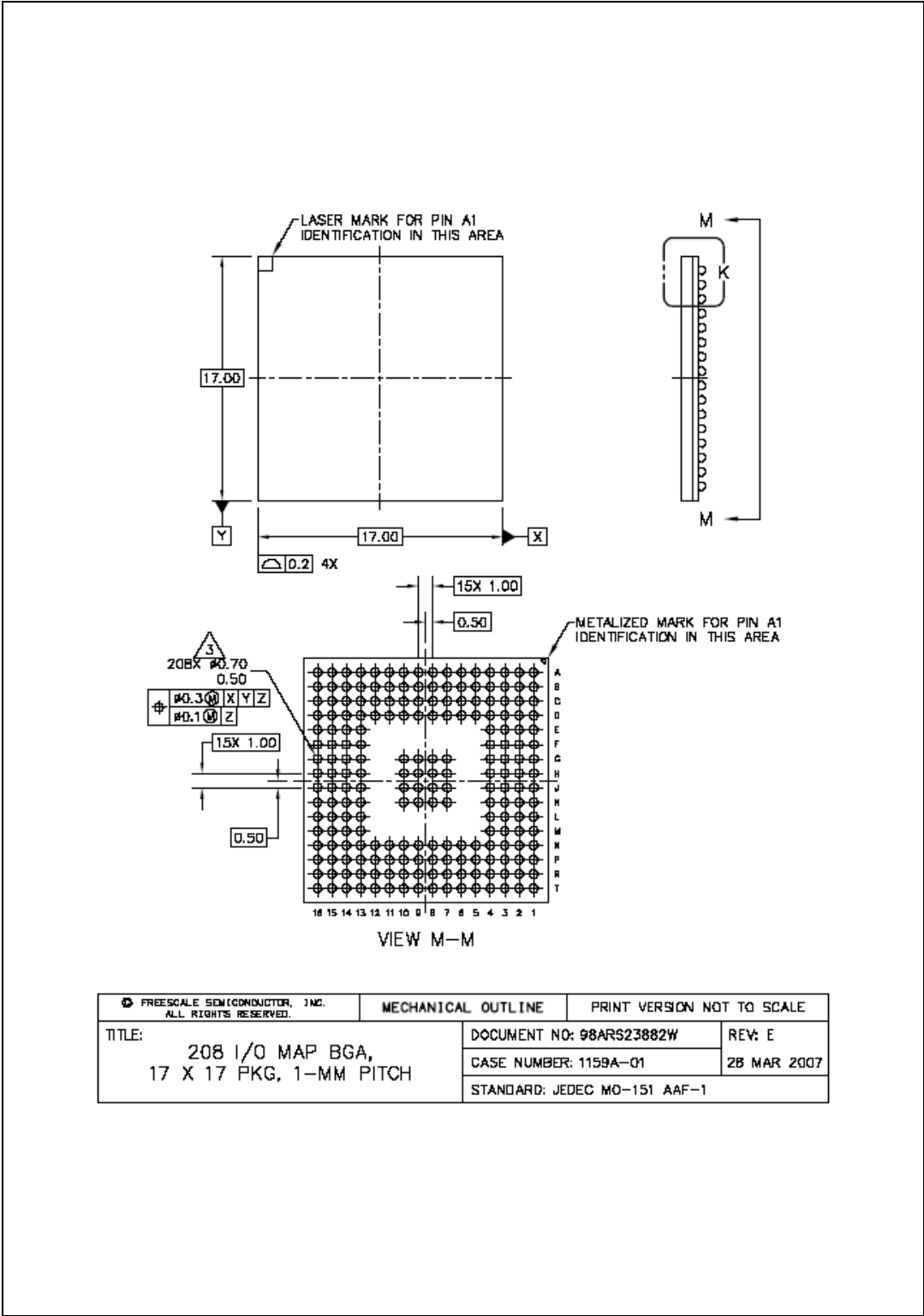


Figure 40. 208 MAPBGA package mechanical drawing (1 of 2)

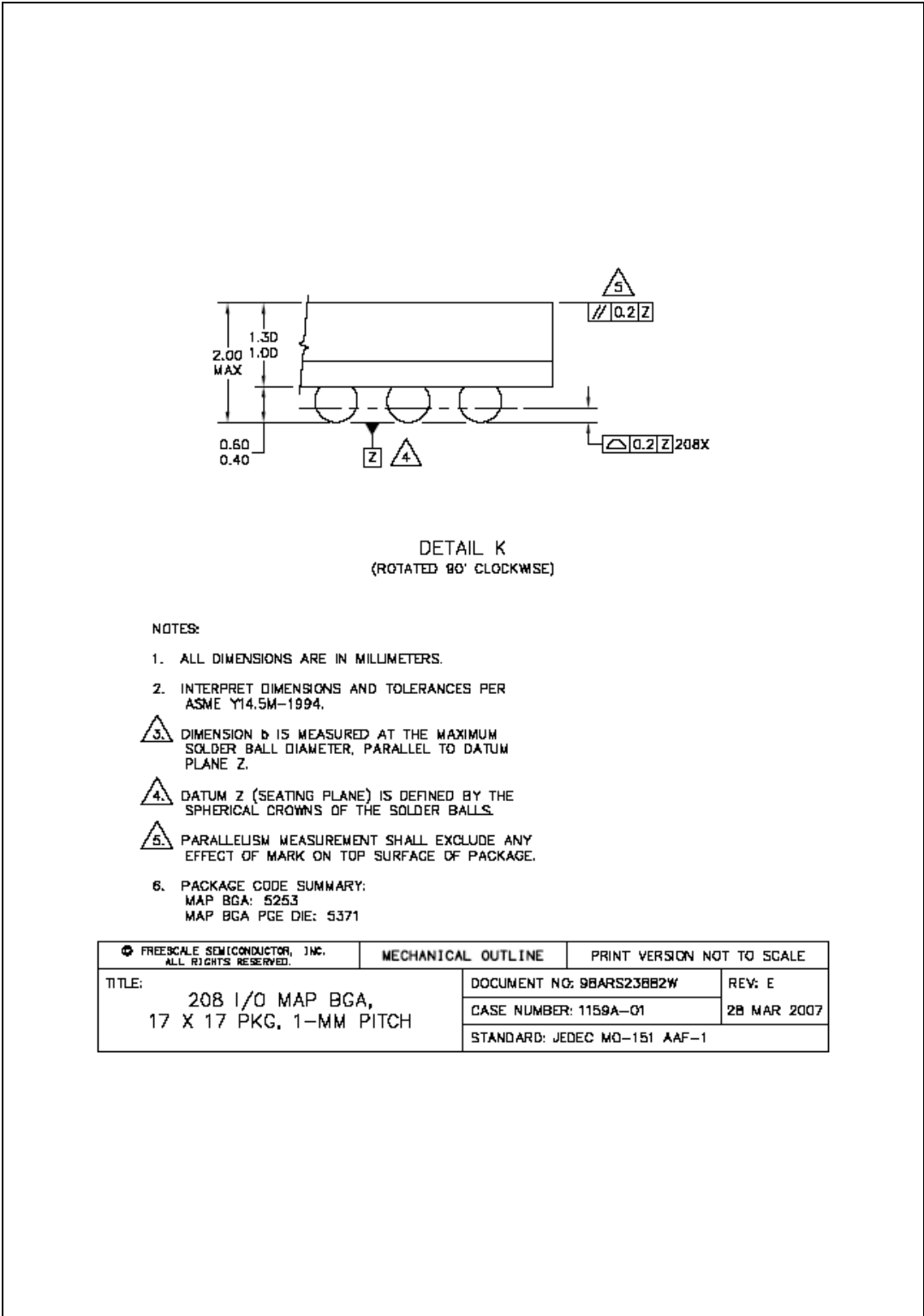
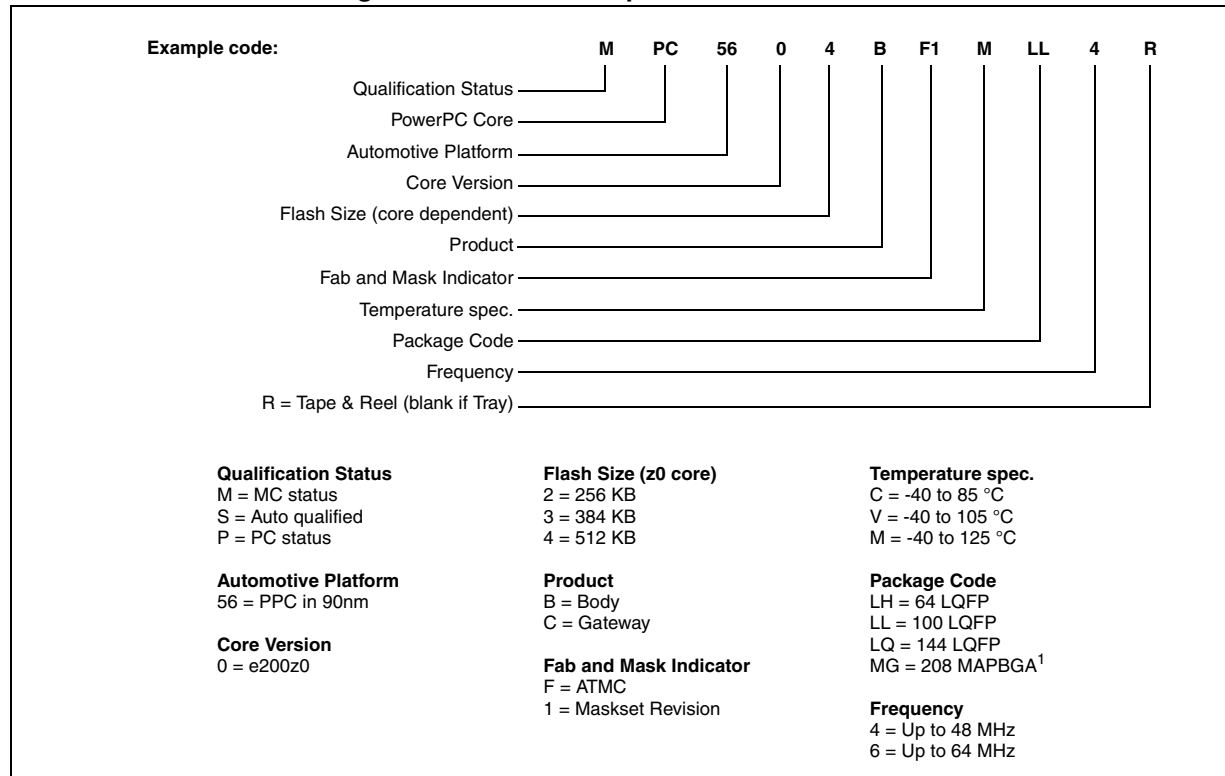


Figure 41. 208 MAPBGA package mechanical drawing (2 of 2)

## 6 Ordering information

Figure 42. Commercial product code structure



<sup>1</sup> 208 MAPBGA available only as development package for Nexus2+

## 7 Document revision history

Table 43 summarizes revisions to this document.

Table 43. Revision history

Revision	Date	Description of Changes
1	04-Apr-2008	Initial release.

Table 43. Revision history (continued)

Revision	Date	Description of Changes
2	06-Mar-2009	<p>Made minor editing and formatting changes to improve readability</p> <p>Harmonized oscillator naming throughout document</p> <p>Features:</p> <ul style="list-style-type: none"> <li>—Replaced 32 KB with 48 KB as max SRAM size</li> <li>—Updated description of INTC</li> <li>—Changed max number of GPIO pins from 121 to 123</li> </ul> <p>Updated <a href="#">Section 1.2, "Description"</a></p> <p>Updated <a href="#">Table 2</a></p> <p>Added <a href="#">Section 2, "Block diagram"</a></p> <p><a href="#">Section 3, "Package pinouts and signal descriptions"</a>: Removed signal descriptions (these are found in the device reference manual)</p> <p>Updated <a href="#">Figure 5</a>:</p> <ul style="list-style-type: none"> <li>—Replaced VPP with VSS_HV on pin 18</li> <li>—Added MA[1] as AF3 for PC[10] (pin 28)</li> <li>—Added MA[0] as AF2 for PC[3] (pin 116)</li> <li>—Changed description for pin 120 to PH[10] / GPIO[122] / TMS</li> <li>—Changed description for pin 127 to PH[9] / GPIO[121] / TCK</li> <li>—Replaced NMI[0] with NMI on pin 11</li> </ul> <p>Updated <a href="#">Figure 4</a>:</p> <ul style="list-style-type: none"> <li>—Replaced VPP with VSS_HV on pin 14</li> <li>—Added MA[1] as AF3 for PC[10] (pin 22)</li> <li>—Added MA[0] as AF2 for PC[3] (pin 77)</li> <li>—Changed description for pin 81 to PH[10] / GPIO[122] / TMS</li> <li>—Changed description for pin 88 to PH[9] / GPIO[121] / TCK</li> <li>—Removed E1UC[19] from pin 76</li> <li>—Replaced [11] with WKUP[11] for PB[3] (pin 1)</li> <li>—Replaced NMI[0] with NMI on pin 7</li> </ul> <p>Updated <a href="#">Figure 6</a>:</p> <ul style="list-style-type: none"> <li>—Changed description for ball B8 from TCK to PH[9]</li> <li>—Changed description for ball B9 from TMS to PH[10]</li> <li>—Updated descriptions for balls R9 and T9</li> </ul> <p>Added <a href="#">Section 4.2, "Parameter classification"</a> and tagged parameters in tables where appropriate</p> <p>Added <a href="#">Section 4.3, "NVUSRO register"</a></p> <p>Updated <a href="#">Table 5</a></p> <p><a href="#">Section 4.5, "Recommended operating conditions"</a>: Added note on RAM data retention to end of section</p> <p>Updated <a href="#">Table 6</a> and <a href="#">Table 7</a></p> <p>Added <a href="#">Section 4.6.1, "Package thermal characteristics"</a></p> <p>Updated <a href="#">Section 4.6.2, "Power considerations"</a></p> <p>Updated <a href="#">Figure 7</a></p> <p>Updated <a href="#">Table 9</a>, <a href="#">Table 10</a>, <a href="#">Table 11</a>, <a href="#">Table 12</a> and <a href="#">Table 13</a></p> <p>Added <a href="#">Section 4.7.4, "Output pin transition times"</a></p> <p>Updated <a href="#">Table 16</a></p> <p>Updated <a href="#">Figure 8</a></p> <p>Updated <a href="#">Table 18</a></p> <p><a href="#">Section 4.9.1, "Voltage regulator electrical characteristics"</a>: Amended description of LV_PLL</p> <p><a href="#">Figure 10</a>: Exchanged position of symbols C<sub>DEC1</sub> and C<sub>DEC2</sub></p> <p>Updated <a href="#">Table 19</a></p>



Table 43. Revision history (continued)

Revision	Date	Description of Changes
2	06-Mar-2009	<p>Added <a href="#">Figure 11</a>  Updated <a href="#">Table 20</a> and <a href="#">Table 21</a>  Updated <a href="#">Section 4.11</a>, “Flash memory electrical characteristics”  Added <a href="#">Section 4.12</a>, “Electromagnetic compatibility (EMC) characteristics”  Updated <a href="#">Section 4.13</a>, “Fast external crystal oscillator (4 to 16 MHz) electrical characteristics”  Updated <a href="#">Section 4.14</a>, “Slow external crystal oscillator (32 kHz) electrical characteristics”  Updated <a href="#">Table 34</a>, <a href="#">Table 35</a> and <a href="#">Table 36</a>  Added <a href="#">Section 4.19</a>, “On-chip peripherals”  Added <a href="#">Table 37</a>  Updated <a href="#">Table 38</a>  Updated <a href="#">Table 47</a>  Added <a href="#">Section Appendix A</a>, “Abbreviations”</p>
4	06-Aug-2009	<p>Updated <a href="#">Figure 6</a>  <a href="#">Table 5</a>  <ul style="list-style-type: none"> <li>• <math>V_{DD\_ADC}</math>: changed min value for “relative to <math>V_{DD}</math>” condition</li> <li>• <math>V_{IN}</math>: changed min value for “relative to <math>V_{DD}</math>” condition</li> <li>• <math>I_{CORELV}</math>: added new row</li> </ul> <a href="#">Table 7</a>  <ul style="list-style-type: none"> <li>• <math>T_A</math> C-Grade Part, <math>T_J</math> C-Grade Part, <math>T_A</math> V-Grade Part, <math>T_J</math> V-Grade Part, <math>T_A</math> M-Grade Part, <math>T_J</math> M-Grade Part: added new rows</li> <li>• Changed capacitance value in footnote</li> </ul> <a href="#">Table 14</a>  <ul style="list-style-type: none"> <li>• MEDIUM configuration: added condition for <math>PAD3V5V = 0</math></li> </ul> Updated <a href="#">Figure 10</a>  <a href="#">Table 19</a>  <ul style="list-style-type: none"> <li>• <math>C_{DEC1}</math>: changed min value</li> <li>• <math>I_{MREG}</math>: changed max value</li> <li>• <math>I_{DD\_BV}</math>: added max value footnote</li> </ul> <a href="#">Table 20</a>  <ul style="list-style-type: none"> <li>• <math>V_{LVDHV3H}</math>: changed max value</li> <li>• <math>V_{LVDHV3L}</math>: added max value</li> <li>• <math>V_{LVDHV5H}</math>: changed max value</li> <li>• <math>V_{LVDHV5L}</math>: added max value</li> </ul> Updated <a href="#">Table 21</a>  <a href="#">Table 23</a>  <ul style="list-style-type: none"> <li>• Retention: deleted min value footnote for “Blocks with 100,000 P/E cycles”</li> </ul> <a href="#">Table 31</a>  <ul style="list-style-type: none"> <li>• <math>I_{FXOSC}</math>: added typ value</li> </ul> <a href="#">Table 33</a>  <ul style="list-style-type: none"> <li>• <math>V_{SXOSC}</math>: changed typ value</li> <li>• <math>T_{SXOSCU}</math>: added max value footnote</li> </ul> <a href="#">Table 34</a>  <ul style="list-style-type: none"> <li>• <math>\Delta t_{LTJIT}</math>: added max value</li> </ul> Updated <a href="#">Figure 36</a></p>

Table 43. Revision history (continued)

Revision	Date	Description of Changes
5	02-Nov-2009	<p>Table: "MPC5604B/C series block summary"</p> <p>Added a new row</p> <p>Table: "Absolute maximum ratings"</p> <ul style="list-style-type: none"> <li>• <math>V_{DD\_BV}</math>, <math>V_{DD\_ADC}</math>, <math>V_{IN}</math>: changed max value</li> </ul> <p>Table: "Recommended operating conditions (3.3 V)"</p> <ul style="list-style-type: none"> <li>• <math>TV_{DD}</math>: deleted min value</li> </ul> <p>Table: "Reset electrical characteristics"</p> <ul style="list-style-type: none"> <li>• Changed footnotes 3 and 5</li> </ul> <p>Table: "Voltage regulator electrical characteristics"</p> <ul style="list-style-type: none"> <li>• <math>C_{REGn}</math>: changed max value</li> <li>• <math>C_{DEC1}</math>: split into 2 rows</li> <li>• Updated voltage values in footnote 4</li> </ul> <p>Table: "Low voltage monitor electrical characteristics"</p> <ul style="list-style-type: none"> <li>• Updated column Conditions</li> <li>• <math>V_{LVDLVCORL}</math>, <math>V_{LVDLVBKPL}</math>: changed min/max value</li> </ul> <p>Table: "Program and erase specifications"</p> <ul style="list-style-type: none"> <li>• <math>T_{dwprom}</math>: added initial max value</li> </ul> <p>Table: "Flash module life"</p> <ul style="list-style-type: none"> <li>• Retention: changed min value for blocks with 100K P/E cycles</li> </ul> <p>Table: "Flash power supply DC electrical characteristics"</p> <ul style="list-style-type: none"> <li>• <math>I_{FREAD}</math>, <math>I_{FMODE}</math>: added typ value</li> <li>• Added footnote 1</li> </ul> <p>Added Section: "NVUSRO[WATCHDOG_EN] field description"</p> <p>Section 4.18: "ADC electrical characteristics" has been moved up in hierarchy (it was Section 4.18.5).</p> <p>Table: "ADC conversion characteristics"</p> <ul style="list-style-type: none"> <li>• <math>R_{AD}</math>: changed initial max value</li> </ul> <p>Table: "On-chip peripherals current consumption"</p> <ul style="list-style-type: none"> <li>• Removed min/max from the heading</li> <li>• Changed unit of measurement and consequently rounded the values</li> </ul>

Table 43. Revision history (continued)

Revision	Date	Description of Changes
6	15-Mar-2010	<p><i>Section "Introduction"</i></p> <ul style="list-style-type: none"> <li>Relocated a note</li> </ul> <p><i>Table: "MPC5604B/C device comparison"</i></p> <ul style="list-style-type: none"> <li>Added footnote regarding SCI and CAN</li> </ul> <p><i>Table: "Absolute maximum ratings"</i></p> <ul style="list-style-type: none"> <li>Removed the min value of <math>V_{IN}</math> relative to <math>V_{DD}</math></li> </ul> <p><i>Table "Recommended operating conditions (3.3 V)"</i></p> <ul style="list-style-type: none"> <li><math>T_A</math> C-Grade Part, <math>T_J</math> C-Grade Part, <math>T_A</math> V-Grade Part, <math>T_J</math> V-Grade Part, <math>T_A</math> M-Grade Part, <math>T_J</math> M-Grade Part: added new rows</li> <li><math>T_{VDD}</math>: made single row</li> </ul> <p><i>Table: "LQFP thermal characteristics"</i></p> <ul style="list-style-type: none"> <li>Added more rows</li> </ul> <p><i>Removed table "208 MAPBGA thermal characteristics"</i></p> <p><i>Table "I/O consumption"</i></p> <ul style="list-style-type: none"> <li>Removed <math>I_{DYNSEG}</math> row</li> <li>Added "I/O weight" table</li> </ul> <p><i>Table "Voltage regulator electrical characteristics"</i></p> <ul style="list-style-type: none"> <li>Updated the values</li> <li>Removed <math>I_{VREGREF}</math> and <math>I_{VREDLVD12}</math></li> <li>Added a note about <math>I_{DD\_BC}</math></li> </ul> <p><i>Table "Low voltage monitor electrical characteristics"</i></p> <ul style="list-style-type: none"> <li>Updated <math>V_{PORH}</math> values</li> <li>Updated <math>V_{LVDLVCORL}</math> value</li> </ul> <p><i>Table "Low voltage power domain electrical characteristics"</i></p> <ul style="list-style-type: none"> <li>Entirely updated</li> </ul> <p><i>Table "Program and erase specifications"</i></p> <ul style="list-style-type: none"> <li>Inserted <math>T_{eslat}</math> row</li> </ul> <p><i>Table "Flash power supply DC electrical characteristics"</i></p> <ul style="list-style-type: none"> <li>Entirely updated</li> </ul> <p><i>Table "Start-up time/Switch-off time"</i></p> <ul style="list-style-type: none"> <li>Entirely updated</li> </ul> <p><i>Figures "Crystal oscillator and resonator connection scheme"</i></p> <ul style="list-style-type: none"> <li>Relocated a note</li> </ul> <p><i>Table "Slow external crystal oscillator (32 kHz) electrical characteristics"</i></p> <ul style="list-style-type: none"> <li>Removed <math>g_{mSXOSC}</math> row</li> <li>Inserted values of <math>I_{SXOSCBias}</math></li> </ul> <p><i>Table "Fast internal RC oscillator (16 MHz) electrical characteristics"</i></p> <ul style="list-style-type: none"> <li>Entirely updated.</li> </ul> <p><i>table "ADC conversion characteristics"</i></p> <ul style="list-style-type: none"> <li>updated the description of the conditions of <math>t_{ADC\_PU}</math> and <math>t_{ADC\_S}</math>.</li> </ul> <p><i>Table "DSPI characteristics"</i></p> <ul style="list-style-type: none"> <li>Entirely updated.</li> </ul> <p><i>Table "Orderable part number summary"</i></p> <ul style="list-style-type: none"> <li>modified some orderable part number.</li> </ul> <p><i>Figure "Commercial product code structure"</i></p> <ul style="list-style-type: none"> <li>Updated</li> </ul> <p><i>Removed the note about the condition from "Flash read access timing" table</i></p> <p><i>Removed the notes that assert the values need to be confirmed before validation</i></p> <p><i>Exchanged the order of "LQFP 100-pin configuration" and "LQFP 144-pin configuration"</i></p> <p><i>Exchanged the order of "LQFP 100-pin package mechanical drawing" and "LQFP 144-pin package mechanical drawing"</i></p>

Table 43. Revision history (continued)

Revision	Date	Description of Changes
7	05-Jul-2010	<p>Added 64 LQFP package information</p> <p>Updated the "Features" section.</p> <p>Removed alternate function information from "LQFP 100-pin configuration" and "LQFP 100-pin configuration" figures.</p> <p>Added "Functional port pin descriptions" table</p> <p>Added eDMA block in the "MPC5604B/C series block diagram" figure</p> <p>Deleted the "NVUSRO[WATCHDOG_EN] field description" section</p> <p>Table "Recommended operating conditions (3.3 V)" and "Recommended operating conditions (5.0 V)": deleted the conditions of <math>T_A</math> C-Grade Part, <math>T_A</math> V-Grade Part, <math>T_A</math> M-Grade Part</p> <p>Table "LQFP thermal characteristics": rounded the values</p> <p>Replaced "nRSTIN" with "RESET" in the "RESET electrical characteristics" section.</p> <p>Table "I/O input DC electrical characteristics"</p> <ul style="list-style-type: none"> <li>• <math>W_{FI}</math>: inserted a footnote</li> <li>• <math>W_{NFI}</math>: inserted a footnote</li> </ul> <p>Table: "Low voltage monitor electrical characteristics"</p> <ul style="list-style-type: none"> <li>• changed min value <math>V_{LVDHV3L}</math>, from 2.7 to 2.6</li> <li>• Inserted max value of <math>V_{LVDLVCORL}</math></li> </ul> <p>Table "FMPLL electrical characteristics": rounded the values of <math>f_{VCO}</math></p> <p>Table "DSPI characteristics":</p> <ul style="list-style-type: none"> <li>• Added <math>\Delta t_{ASC}</math> row</li> <li>• Update values of <math>t_A</math></li> </ul> <p>Added "<math>I_{ADCPWD}</math>" and "<math>I_{ADCRUN}</math>" rows within "ADC conversion characteristics" table.</p> <p>Removed "Orderable part number summary" table.</p>

## Appendix A Abbreviations

Table 44 lists abbreviations used but not defined elsewhere in this document.

**Table 44. Abbreviations**

Abbreviation	Meaning
CMOS	Complementary metal–oxide–semiconductor
CPHA	Clock phase
CPOL	Clock polarity
CS	Peripheral chip select
EVTO	Event out
MCKO	Message clock out
MDO	Message data out
MSEO	Message start/end out
MTFE	Modified timing format enable
SCK	Serial communications clock
SOUT	Serial data out
TBD	To be defined
TCK	Test clock input
TDI	Test data input
TDO	Test data output
TMS	Test mode select

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