DTUsat

Interboard Communication

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1 Introduction

This paper summarizes the interboard communication for the DTUsat satellite as defined on a meeting of hardware groups on January 18th, 2002. It is available from the DTUsat homepage at www.dtusat.dtu.dk

1.1 Conventions

Input and output directions are defined relative to boards that connect to the Onboard Computer (OBC).

- *Input lines* are inputs to the local board and outputs from the OBC
- *Output lines* are outputs from the local board and inputs to the OBC

2 Interconnection Overview

The board communication interconnections consists of three logical separate parts.

- Dedicated lines
- UART (Universal Asynchronous Receive and Transmit) lines
- SPI (Serial Peripheral Interface) bus

The interconnections are shown in a block diagram on page 3.

2.1 Dedicated Lines

These lines are 1 line wide and have board specific functionality and can be either input or output. In the present design there are only input lines.

2.2 UART Lines

For word based, asynchronous communication UART communication connects the OBC to the Radio, Camera and Harness boards. The UART connection is 2 line wide (1 RX / 1 TX). The Radio has a dedicated UART on the OBC, while Camera and Harness share a single OBC UART that is multiplexed. The OBC handles all aspects of the multiplexing.

2.3 SPI Bus

For word based, synchronous communication an SPI bus connects the Power, Radio, Attitude Control and Tether boards to the OBC. The main purpose of the SPI bus is to allow access from the OBC to ADCs and DACs on other boards.

Each board connected to the SPI bus has 5 input lines as follows

- *Master Out Slave In (MOSI)* – data input
- *Master In Slave Out (MISO)* – data output
- *Serial Clock SCLK* – clock input
- *Slave Select A SS_A* – enable slave A, input
- *Slave Select B SS_B* – enable slave B, input

The presence of 2 Slave Select (SS) lines allows two SPI slaves to be implemented on a board. The OBC board has 11 lines, MOSI, MISO, SCLK and 8 SS lines.

3 Electrical Considerations

The electrical implementation of the interboard communication is work in progress, and the below is far from complete.

3.1 Dedicated Lines

To avoid damage when both circuits on each end of a line try to drive the line, a serial resistance should be included to limit the current on the lines whenever feasible.

3.2 UART Lines

Nothing so far.

3.3 SPI

To avoid damage when more than one circuit on a line tries to drive that line, a serial resistance should be included at inputs to limit the current on the lines whenever feasible.

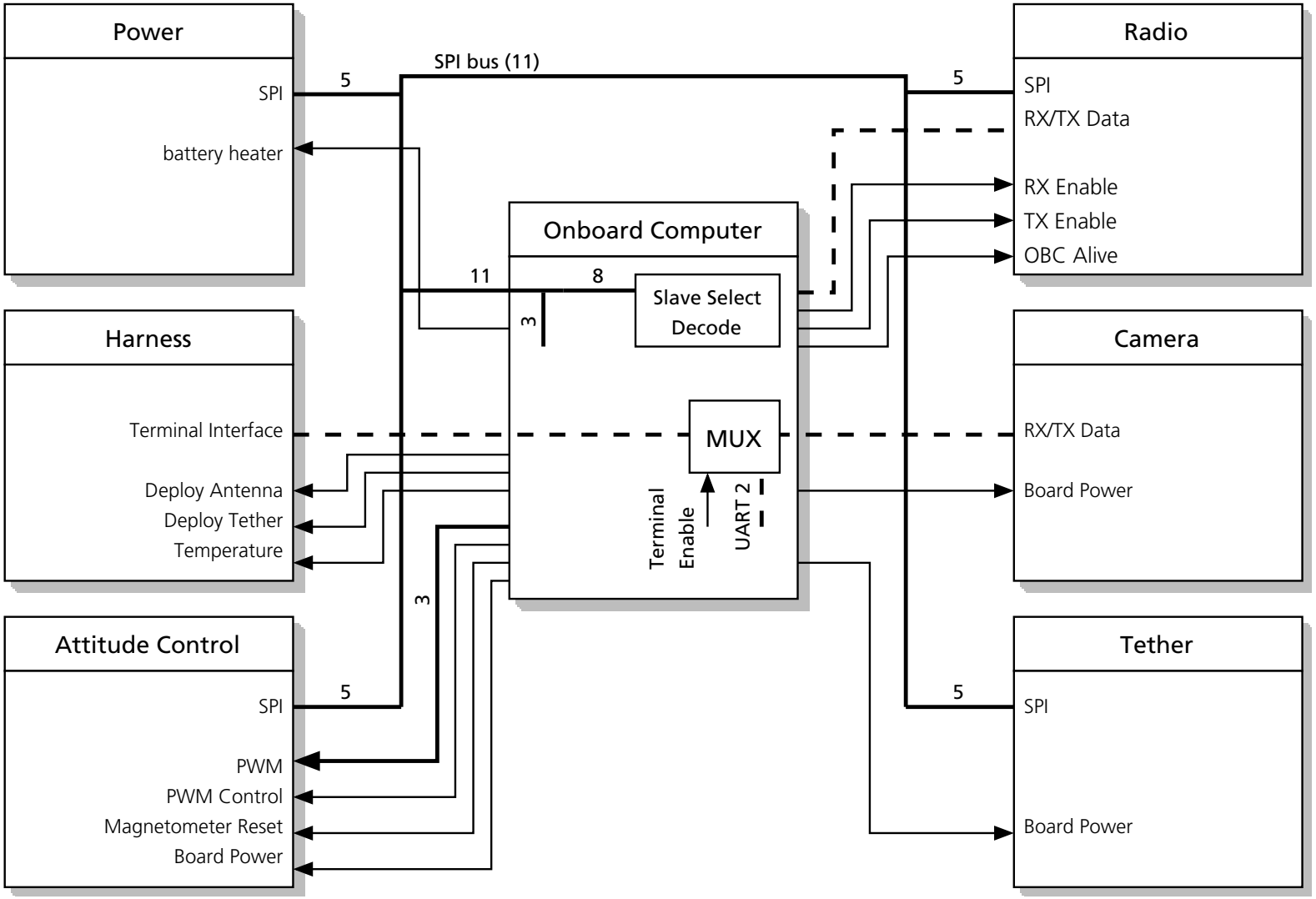

Figure 1: Block diagram of the boards showing their communication interconnections