Technical Report
on

Band-Gap Reference

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Contents

List of Figures

Band-Gap Reference Circuit

Voltage Reference circuits provide constant, stable voltage irrespective of variations in temperature, supply voltage and process parameters. It is a vital analog building block used in many applications like Low Dropout voltage regulators, Analog to digital converter, Digital to analog converter, Buck converters etc. Compared to a voltage regulator, reference circuit lack current driving capability.

As per industry standards, range of variation in temperature is considered as from -40^0C to 125^0C. Range of supply variation depends on applications, typically 10% to 20% from the typical value of voltage supply.

To design a reference circuit, first the temperature dependency behavior of electronic devices has to be analyzed.

1 Device response to temperature variations

All electronic devices are sensitive to temperature variations. If voltage across a device increases with the increase in temperature, then such devices are called PTAT [Proportional to Absolute Temperature]. If voltage decreases with the increase in temperature then such devices are called CTAT [Complementary to Absolute Temperature].

Consider Fig. 1 (a), where typical response of PTAT and CTAT voltages are given. If we add PTAT and CTAT voltages we get the response as shown in Fig. 1 (b). Though the Response is not that of a voltage reference, we can achieve it by multiplying PTAT and CTAT voltages with suitable constants. Fig. 2 forms the basic idea behind the band-gap reference.

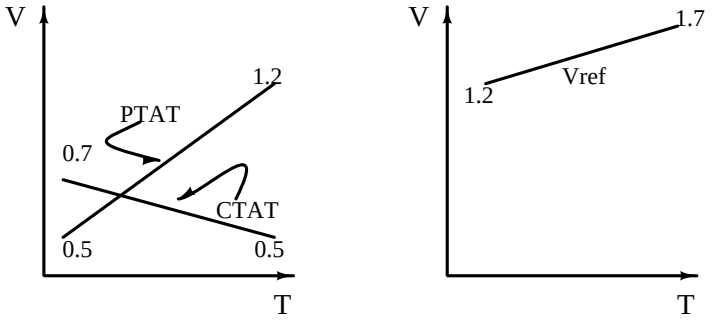

Fig. 1: (a) PTAT and CTAT responses (b) Response of voltage reference

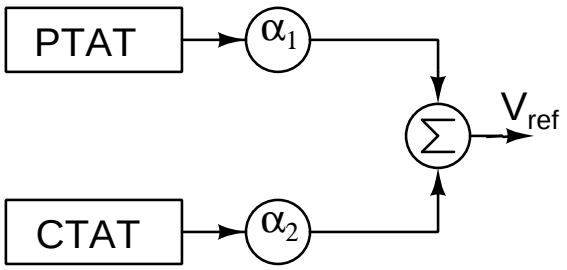

Fig. 2: Generation of V_{ref} voltage

2 CTAT

CTAT voltage can be obtained from a diode if a constant current I_O is passed through it as shown in Fig. 3.

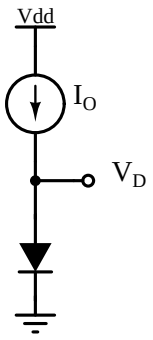

Fig. 3: Diode biased using constant current I_O

The voltage across diode V_D is given by

$$\boxed{V_D = V_T ln(\frac{I_O}{I_S})} \tag{1}$$

where $V_T = \frac{kT}{q}$ is a PTAT with $\frac{\partial V_D}{\partial T} = \frac{k}{q}$. The reverse saturation current I_S is given by

$$\boxed{I_S = bT^{4+m} exp(\frac{-E_g}{kT})} \tag{2}$$

Where b is a constant and m=-1.5 and E_g is energy gap between conductance band and valence band of silicon.

V_D has two temperature dependent components V_T and I_S. Let us first find, Dependency of I_S on temperature,

$$\begin{aligned}\frac{\partial I_S}{\partial T} &= b\{T^{4+m} exp(\frac{-E_g}{kT})\frac{E_g}{kT^2} + exp(\frac{-E_g}{kT})(4+m)T^{3+m}\} \\ &= exp(\frac{-E_g}{kT}) bT^{4+m}[\frac{E_g}{kT^2} + (4+m)T^{-1}]\end{aligned}$$

$$\boxed{\frac{\partial I_S}{\partial T} = I_S[\frac{4+m}{T} + \frac{E_g}{kT^2}]} \tag{3}$$

Now to find the temperature dependency of V_D on temperature, equation 1 is differentiated w.r.t temperature.

$$\begin{aligned}\frac{\partial V_D}{\partial T} &= \frac{\partial V_T}{\partial T} ln\frac{I_O}{I_S} + V_T \frac{\partial}{\partial T}(ln\frac{I_O}{I_S}) \\ &= \frac{\partial V_T}{\partial T} ln\frac{I_O}{I_S} + V_T \frac{I_S}{I_O}\frac{-I_O}{I_S^2}\frac{\partial I_S}{\partial T} \\ &= \frac{V_T}{T} ln\frac{I_O}{I_S} - \frac{V_T}{T}(4+m) - \frac{V_T E_g}{kT^2} \\ &= \frac{V_D}{T} - \frac{V_T}{T}(4+m) - \frac{E_g}{qT}\end{aligned}$$

$$\boxed{\frac{\partial V_D}{\partial T} = \frac{1}{T}[V_D - (4+m)V_T - \frac{E_g}{q}]} \tag{4}$$

If we substitute all values,

$$\frac{\partial V_D}{\partial T} = \frac{1}{300}[0.7 - (4+1.5)26m - 1.2] = -1.88mV/^0K$$

This proves the voltage across a diode when biased using constant current source, is a CTAT with the slope of $-1.88mV/^0K$.

3 Diodes in standard CMOS process

Diodes in standard CMOS process can be constructed by simply cascading p-sub and n+ region as shown in Fig. 4(a). However p-sub is always connected to ground. Hence anode is always grounded and can not be used for CTAT generation. A parasitic pnp BJT can be constructed as shown in Fig. 4(b), in that a pn junction can be used as diode. But a small base current (Anode) can cause a large substrate current i.e collector terminal of pnp. Since substrate is common for all devices, it disturbs operation of other devices. An improved vertical parasitic pnp transistor can be constructed as shown in Fig. 5. In which an extra p+ region is created and used as collector. Thus p-sub is separated.

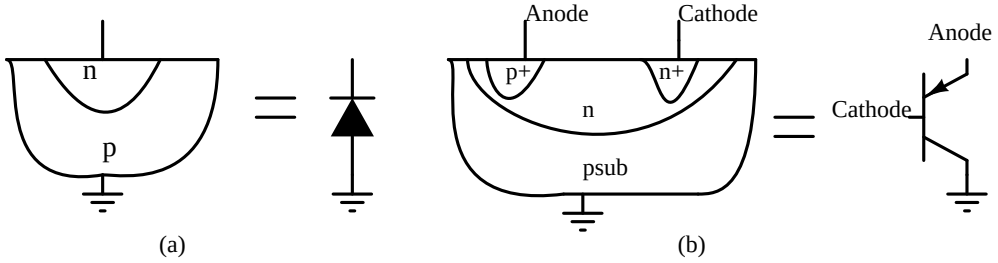

Fig. 4: (a)Diode (b)PNP in CMOS process

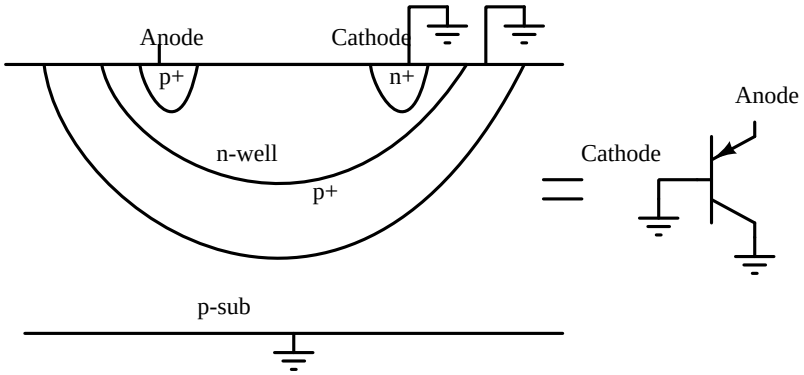

Fig. 5: Improved PNP structure in CMOS process

4 PTAT

Though voltage across a diode is a CTAT, actually it has two components one is V_T which is a PTAT and other is $ln\frac{I_O}{I_S}$ which is a CTAT. Since the latter is dominant, finally voltage across diode will be a CTAT. However if we extract V_T from the above, a PTAT voltage can be constructed.

Consider the two circuits shown in Fig. 6.

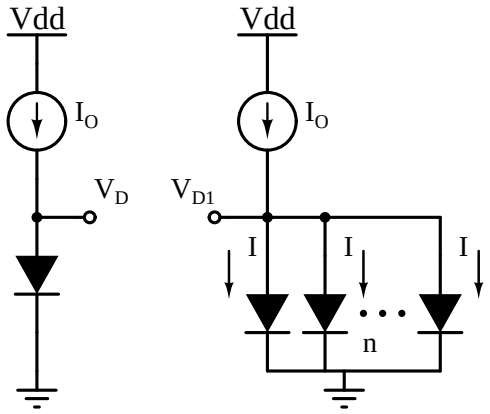

Fig. 6: Single diode and multiple diodes biased using constant current

The current in multiple diodes circuit is given by

$$\begin{aligned} I_O &= nI \\ &= nI_S exp(\frac{V_{D1}}{V_T}) \end{aligned}$$

Hence voltage across parallel diodes is,

$$V_{D1} = V_T ln(\frac{I_O}{nI_S})$$

If we subtract voltage across single diode and volatge across paralle diodes,

$$V_D - V_{D1} = V_T(ln\frac{I_O}{I_S} - ln\frac{I_O}{nI_S})$$

$$\boxed{V_D - V_{D1} = V_T ln(n)} \tag{5}$$

The equation 5 shows that the difference of voltage across a single diode and multiple diodes is PTAT in nature.

The difference of voltages can be obtained as shown in Fig 7 using a resistor R_1 and forcing $V_D = V_2$. Then

$$\begin{aligned} V_D &= I_O R_1 + V_{D1} \\ I_O R_1 &= V_D - V_{D1} = V_T ln(n) \end{aligned}$$

Thus voltage across R_1 is a PTAT voltage.

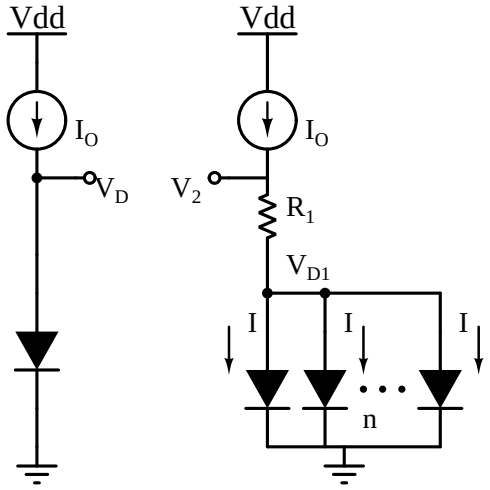

Fig. 7: PTAT circuit

So far we have assumed two things-

1. I_O is constant
2. $V_D = V_2$

To achieve these, either a current mirror or an op-amp can be used. Fig. 8 illustrates how a current mirror can be used for PTAT generation.

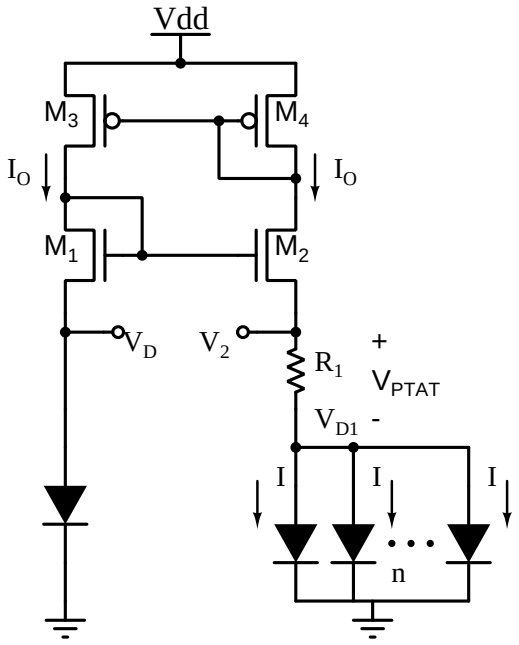

Fig. 8: A current mirror based PTAT circuit

The current flowing through M_1 and M_2 are given by

$$I_{D1} = \frac{K_n}{2}\frac{W}{L}(V_{GS1} - V_{th})^2$$
$$I_{D2} = \frac{K_n}{2}\frac{W}{L}(V_{GS2} - V_{th})^2$$

From the current mirror property $I_{D1} = I_{D2}$, Hence

$$(V_{GS1} - V_{th})^2 = (V_{GS2} - V_{th})^2$$
$$V_{GS1} = V_{GS2}$$
$$V_G - V_D = V_G - V_2$$
$$V_D = V_2$$

Voltage across R_1 gives a PTAT voltage. PTAT voltage can be separated into another branch. Fig. 9 shows final circuit for PTAT. The voltage across R_2 is a PTAT voltage which is given by equation (6).

$$\boxed{V_{R2} = I_O R_2 = V_T ln(n)\frac{R_2}{R_1}} \tag{6}$$

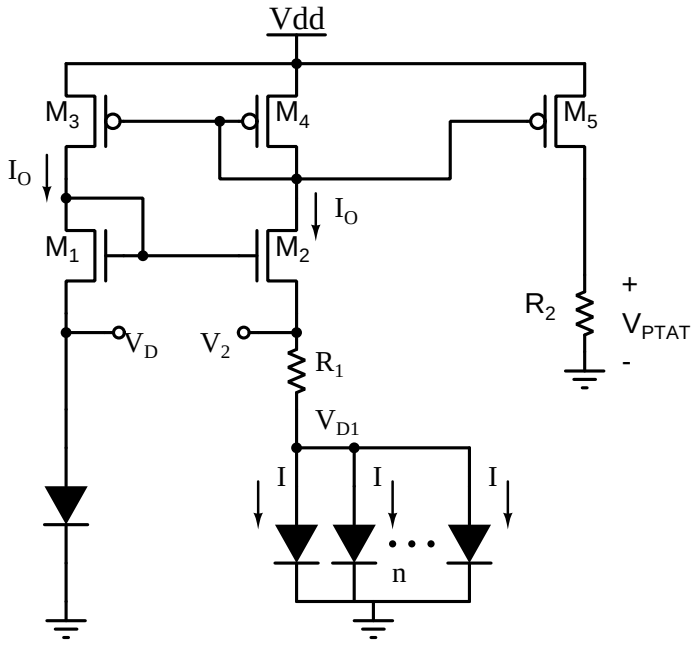

Fig. 9: PTAT circuit

5 Adding PTAT and CTAT

As mentioned in Fig. 2, a reference voltage response can be obtained by adding PTAT and CTAT voltages with suitable constants multiplied to each. For the circuit design perspective, two voltages can be added by connecting them in series. Fig. 10 shows voltage reference circuit where CTAT and PTAT voltages are connected in series.

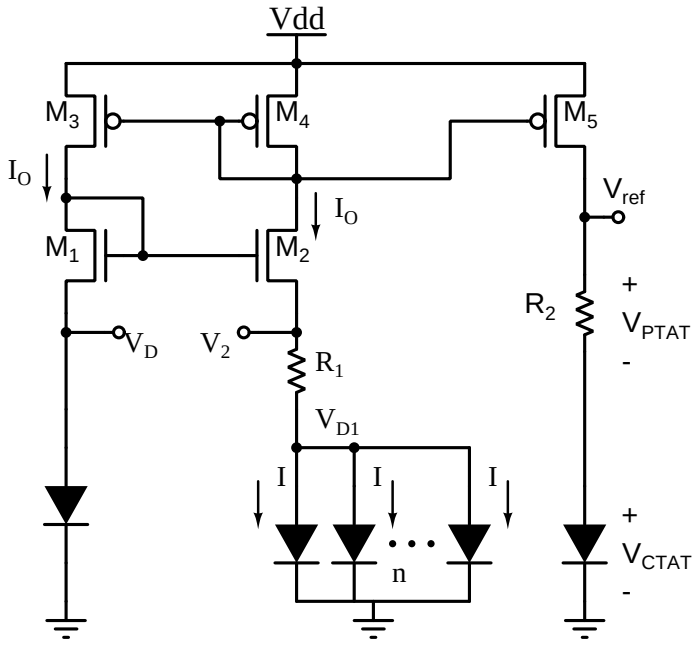

Fig. 10: Reference circuit in which PTAT and CTAT voltages are added

However there are three main issues with the above circuit,

1. Response to supply variations is not analyzed.

2. The current passing through CTAT diode is not a constant, is a PTAT.

3. Values of α_1 and α_2 are not derived.

5.1 Supply variations

The circuit i.e current mirror or op-amp which forces $V_D = V_2$ must reject any variations present in supply. So Immunity to supply variations depend on robustness of current mirror or op-amp.

5.2 Current through CTAT diode

The current passing through CTAT diode in Fig. 10 is given by

$$I_O = \frac{V_T ln(n)}{R_1}$$

So I_O is a PTAT but when we designed CTAT voltage, we considered a constant current I_O. We must now investigate whether it has any effect on voltage across diode.

$$\begin{aligned}\frac{\partial V_D}{\partial T} &= \frac{\partial}{\partial T}(V_T ln\frac{I_O}{I_S}) \\ &= \frac{\partial}{\partial T}[V_T(lnI_O - lnI_S)]\end{aligned}$$

$$\frac{\partial V_D}{\partial T} = V_T(\frac{1}{I_O}\frac{\partial I_O}{\partial T} - \frac{1}{I_S}\frac{\partial I_S}{\partial T}) + (lnI_O - lnI_S)\frac{\partial V_T}{\partial T} \tag{7}$$

Let us first find $\frac{\partial I_O}{\partial T}$

$$\begin{aligned}\frac{\partial I_O}{\partial T} &= \frac{ln(n)}{R_1}\frac{\partial V_T}{\partial T} \\ &= \frac{ln(n)}{R_1}\frac{V_T}{T}\end{aligned}$$

$$\frac{\partial I_O}{\partial T} = \frac{I_O}{T} \tag{8}$$

Substituting equation 3 and 8 in 7 we get,

$$\begin{aligned}\frac{\partial V_D}{\partial T} &= V_T[\frac{1}{I_O}\frac{I_O}{T} - \frac{1}{I_S}I_S(\frac{4+m}{T} + \frac{E_g}{kT^2})] + \frac{V_T}{T}(lnI_O - lnI_S) \\ &= V_T[\frac{1}{T} - \frac{4+m}{T} - \frac{E_g}{kT^2}] + \frac{V_T}{T}ln\frac{I_O}{I_S} \\ &= V_T[\frac{m+3}{T} - \frac{E_g}{kT^2}] + \frac{V_D}{T} \\ &= \frac{V_D - (m+3)V_T - \frac{E_g}{q}}{T} \\ &\approx \frac{0.7X(3-1.5)26m - 1.2}{300} \approx -1.79mV/^0K\end{aligned}$$

It shows that, though a PTAT current is passed through a diode, voltage across it is still a CTAT with slightly lower slope when compared to diode biased using constant current.

5.3 Design of α_1 and α_2

The α_1 and α_2 values have to be chosen such that when $V_{ref} = \alpha_1 PTAT + \alpha_2 CTAT$ is differentiated w.r.t. temperature, $\frac{\partial V_{ref}}{\partial T}$ must be zero. In the above reference circuit, PTAT is V_T and CTAT is V_D. We also know that PTAT slope is $+85\mu V/^0K$ and CTAT slope is $-1.6mV/^0K$.

$$\begin{aligned} V_{ref} &= \frac{R_2}{R_1} ln(n) V_T + V_D \\ &= \alpha_1 V_T + \alpha_2 V_D \end{aligned}$$

To make $\frac{\partial V_{ref}}{\partial T} = 0$,

$$\begin{aligned} \frac{\partial V_{ref}}{\partial T} &= \alpha_1 \frac{\partial V_T}{\partial T} + \alpha_2 \frac{\partial V_D}{\partial T} = 0 \\ 0 &= \alpha_1 (86\mu V) + \alpha_2 (-1.6mV) \end{aligned}$$

It is not practical to reduce α_2, rather α_1 can be increased to satisfy the above equation. Hence α_2 is taken as 1. This gives $\alpha_1 = 18.82$. Now V_{ref} can be written as

$$\begin{aligned} V_{ref} &= 18.82 V_T + V_D \\ &\approx 18.81 X 26m + 0.7 \\ &\approx 1.2V \end{aligned}$$

Since resulting V_{ref} is nearly equal to 1.2 which is band-gap value of silicon, the reference circuit is known as **Band-Gap** reference.

Design example

Design steps-

1. Choose a current value for biasing [I_O]
   Select $I_O = 5\mu A$

2. Derive R_1 value from following expression

$$R_1 = \frac{V_T ln(n)}{I_O}$$

$$R_1 = \frac{0.026 ln(2)}{5\mu} = 3.6k\Omega$$

3. Derive R_2 from the α_1 expression

$$\alpha_1 = \frac{R_2}{R_1} ln(n)$$

$$R_2 = \frac{\alpha_1 R_1}{ln(n)} = \frac{18.82 X 3600}{ln2} = 97.7k\Omega$$

4. Select large W and L values for MOSFETs of current mirror, so that process variation effects are reduced.
   Select $W/L = 40\mu m/10\mu m$ [CMOS Technology -180nm]

The band-gap reference circuit is designed in 180nm CMOS process, with PTM BSIM v3.2 MOS model. The reference circuit is simulated using spice opus tool. Spice code is given below-

```
*Spice Code for BGR
M1 n1 n1 n3 0 NMOS L=10U W=40U
M2 n2 n1 n4 0 NMOS L=10U W=40U
M3 n1 n2 vdd vdd PMOS L=10U W=40U
M4 n2 n2 vdd vdd PMOS L=10U W=40U
M5 ref n2 vdd vdd PMOS L=10U W=40U
Q1 0 0 n3 PNP
Q2 0 0 n5 PNP
Q3 0 0 n5 PNP
Q4 0 0 ctat PNP
R1 n5 n4 3.6k
R2 ctat ref 96.9k
Vdd vdd 0 DC 1.8
.include PTM.lib
.control
op
dc @@@temp -40 125 1
let ptat=ref-ctat
plot v(ref) v(ptat) v(ctat)
dc vdd 1.6 2 0.01
plot v(ref)
.endc
.end
```

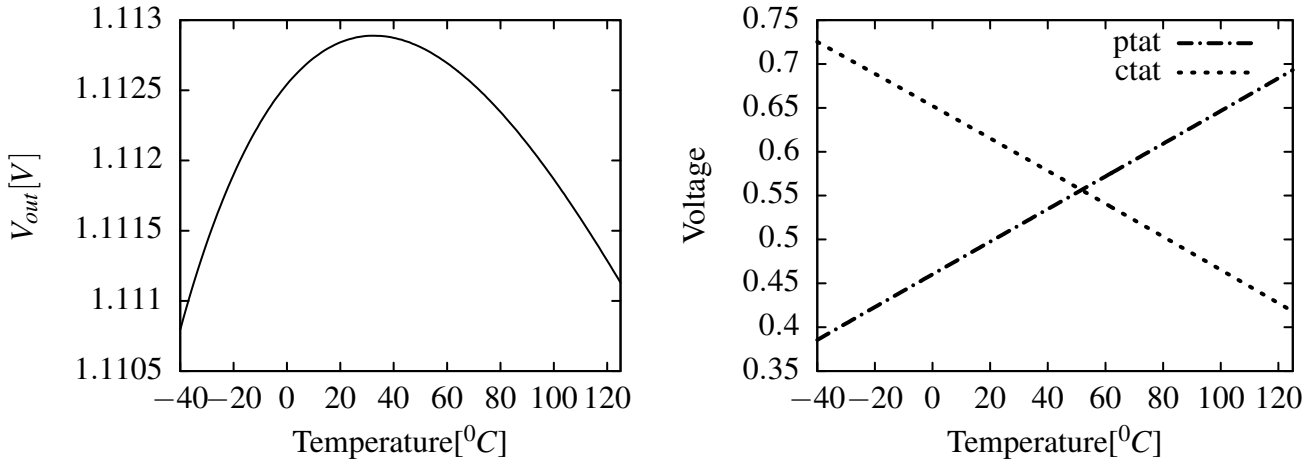

Fig. 11: Response of voltage reference

Fig. 11 shows the response of band-gap voltage reference and response of CTAT and PTAT voltages. When input supply voltage is varied from 1.6 V to 2 V, the change in reference voltage is plotted in Fig. 12.

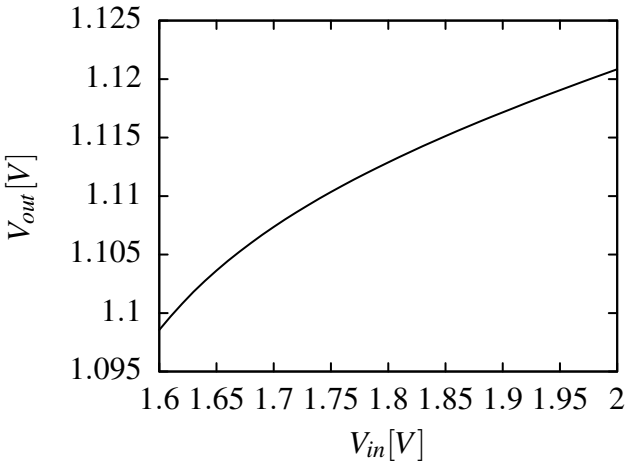

Fig. 12: Response to supply variations

6 BGR with Op-amp

Fig. 12 shows that reference response to supply variations is not good. The reason is the current mirror used in the design is not able to make V_D is exactly equal to V_2. To achieve this an Op-amp in negative feed-back can be used. By connecting V_D and V_2 to the input terminal of an Op-amp in negative feed-back, both can be kept at same potential. Fig. 13 shows the band-gap reference using an Op-amp.

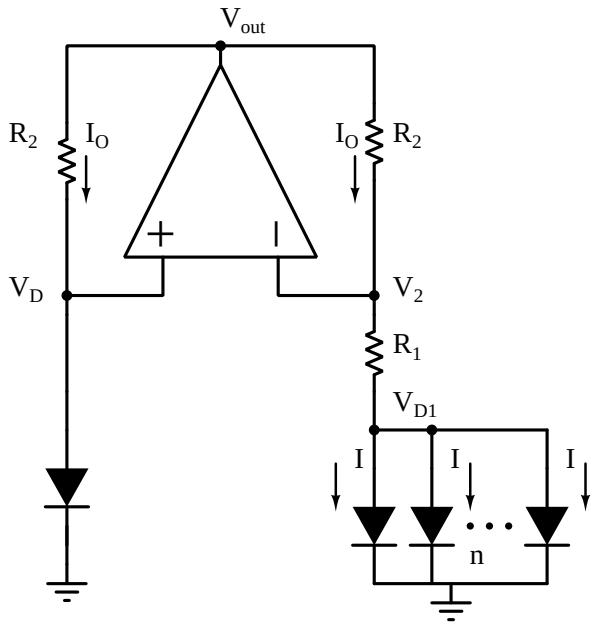

Fig. 13: Band-gap reference using Op-amp

The reference voltage is given by

$$\begin{aligned} V_{ref} &= V_{R2} + V_D \\ &= V_{PTAT} + V_{CTAT} \end{aligned}$$

However above circuit has main two demerits as listed below

1. Current is supplied by Op-amp not by input supply.

2. Usually Operational Trans-conductance is used as Op-amp which can drive only capacitive loads not resistive loads.

To overcome above mentioned ill effects, the topology shown in Fig. 14 is used for generating band-gap reference voltage. The topology resembles circuit shown in Fig. 10 but instead of NMOS current mirror, op-amp is used. Hence the CTAT, PTAT and band-gap reference voltage equations and coefficients remain same for this also.

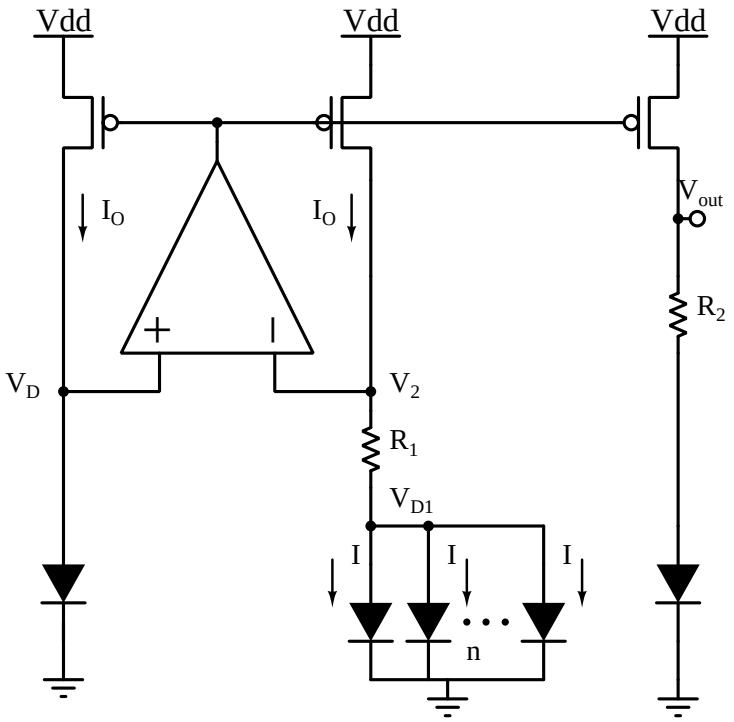

Fig. 14: Band-gap reference using Op-amp

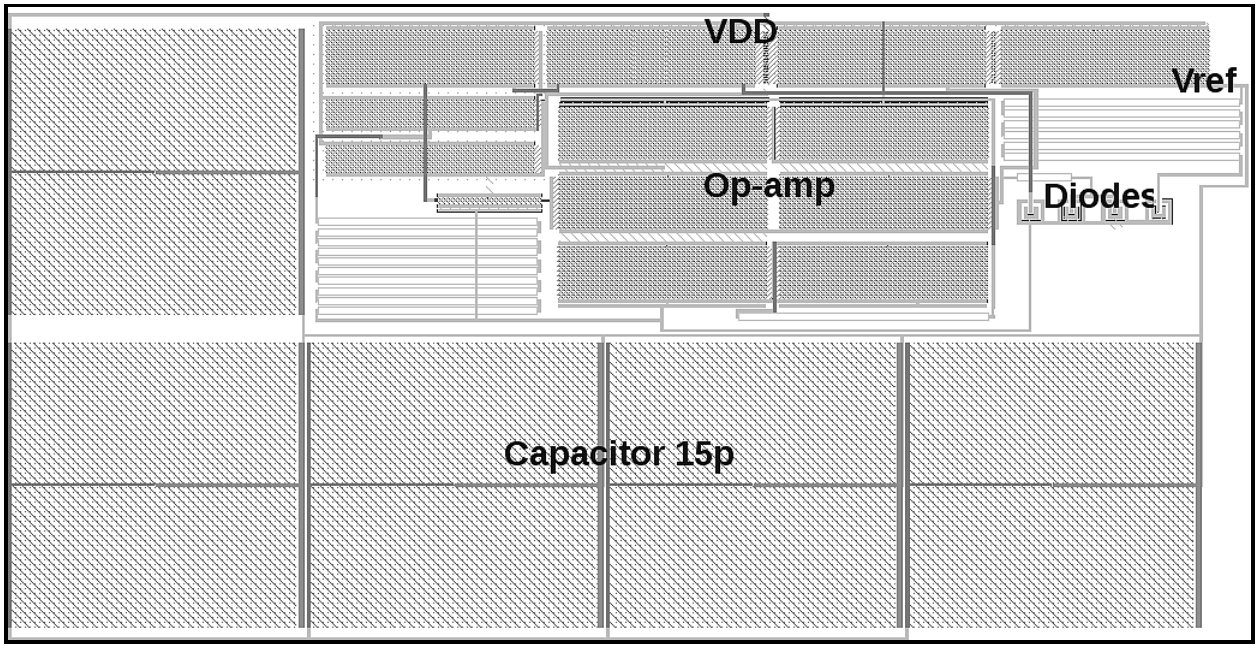

Fig. 15: Layout of Band-gap reference

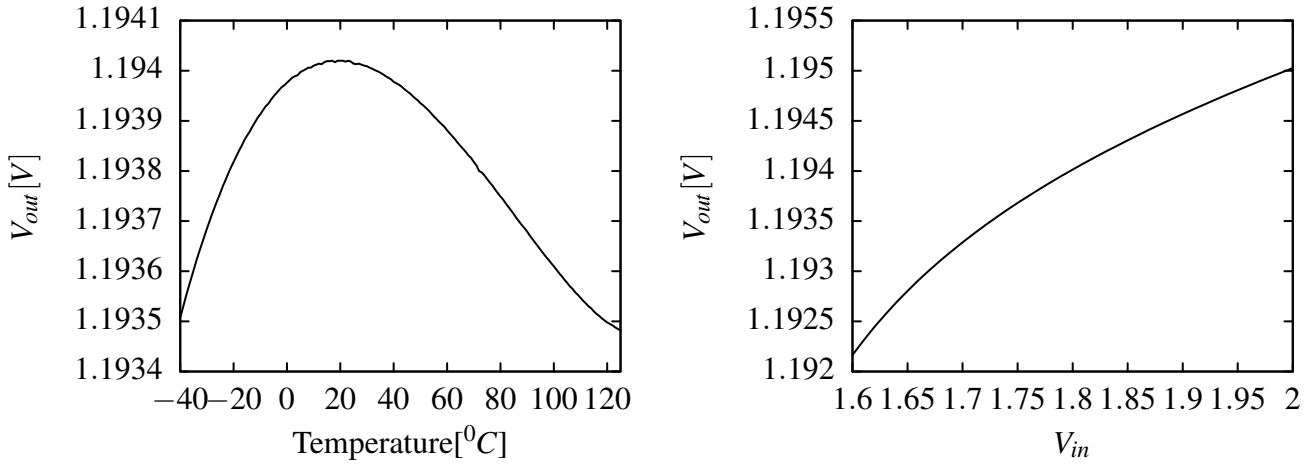

Fig. 16: Post-layout simulation Results of band-gap reference