Guruprasad
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Professional Summary

Analog / AMS Design Engineer with hands-on experience in LDO and power-management circuits in TI CMOS processes. Worked on Texas Instruments client projects involving block-level LDO design support and verification, PVT and Monte-Carlo analysis, trimming, aging, and post-layout simulations. Experienced in silicon/IP-level verification and characterization of non-volatile memories, VCO, HVGEN, and EEPROM IPs, including testbench development without data sheets. Strong background in analog fundamentals, PMIC blocks, and Cadence Spectre-based design flow.

Core Skills

Analog Blocks: LDO, Bandgap, Op-Amps, Comparators, POR, Voltage References
PMIC Concepts: Stability, PSRR, Load Transient, Compensation, Trimming
Verification: PVT, Monte-Carlo, Aging, Burn-in, Corner Analysis
Simulation & Analysis: AC, Transient, Noise, Stability analysis
EDA Tools: Cadence Virtuoso, Spectre, ADE
Technology: TI lbc9 / lbc10 / lbc10lv / lbc10mv

Texas Instruments – Client Projects (via KarMic Design)

Technology nodes: lbc9, lbc10, lbc10lv, lbc10mv
Role: Analog / AMS Design & Verification Engineer

1. **1.8 V NMOS LDO – BEANIE Project (lbc10lv)**
   - Bias circuit modification and block-level design support and verification of NMOS LDO
   - PVT, Monte-Carlo, aging, and burn-in simulations
   - Line/load regulation, PSRR, stability, startup, and load transient analysis
   - Resistor trimming and post-layout simulation support
2. **Embedded Memory & NVM IP Characterization**
   - Worked on EEPROM, MTP, and NVM IPs across multiple TI technologies.
   - Developed testbenches for IDDQ, program/read currents, margin testing.
   - External IREF margin characterization across PVT and Monte-Carlo (up to 1000 samples per corner)
   - Post-burn and post-bake current analysis and data extraction
3. **High-Voltage Generator & VCO IP Testing**
   - HVGENMINILV / HVGENMINIMVAL IP characterization.
   - Designed testbenches to measure IDDQ, frequency vs control voltage.
   - Verified VCO performance across temperature and process corners.
   - Supported performance improvement through circuit-level modifications.

Analog & Mixed-Signal Design Projects (Training / Internal)

1. **PMOS Capless LDO (lbc10)**
   - Designed and verified a PMOS cap-less LDO with focus on stability, quiescent current, and load regulation.
   - Conducted PVT and Monte-Carlo simulations to verify all the performance parameters and compared with the theoretical values.
2. **Bandgap Reference with trimming (lbc10)**
   - Designed and verified current mode sub 1V bandgap voltage reference using vertical PNP based PTAT, CTAT currents and high gain folded cascode operational amplifier.

- Implemented a 5 bit resistor trimming circuit to tune the BGR across Process corners and mismatch.

3. **Design and Implementation of Synchronous voltage mode CCM Buck Converter (lbc10)**
   - Designed a synchronous CCM buck converter comprising Type II compensated folded cascode amplifier, Comparator, Level shifter, Non-overlapping single phase clock generator, Power switch driver, Power switches.
   - Verified each block and simulated Buck converter across PVT corners and measured performance parameters.
4. **Design and Implementation of 4 bit SAR ADC (lbc10)**
   - Designed a SAR ADC comprising Sample and Hold, Comparator, Successive Approximation Logic, Output buffer, Digital to Analog converter, Internal clock and control signal generator.
   - Verified its functional correctness across the PVT corners and measured essential performance parameters.
5. **Design and Implementation of Delta Sigma Modulator (lbc10)**
   - Designed a Delta Sigma Modulator comprising Fully differential folded cascode op-amp with common mode feedback, First order differential switched capacitor active integrator, Dynamic clocked comparator, One bit Digital to Analog converter, Non-overlapping two phase clock generator.
   - Verified each block and simulated the modulator across PVT corners and measured vital parameters.
6. **Design and verification of Digital Phase Locked Loop (lbc10)**
   - Designed a Digital PLL comprising Phase frequency Detector, Charge pump, Loop filter, Current starved 3 stage VCO, Divide by 2.
   - Verified across all PVT corners and ran Monte-Carlo simulation.

Education

B.E - Electronics and Communication

M.Tech - Digital Electronics and Communication

Ph.D - Analog Circuits

Previous Work Experience

- Design Engineer – KarMic Design Pvt. Ltd. Manipal. (Nov 2024 – Present)
- Faculty – ECE (2008 – 2024)

Additional Highlights

- Author of multiple IEEE journal and conference publications in analog circuits.
- NPTEL Topper – Power Management IC (IIT Chennai)