

33-ma b								X30 I/O LIST				I	n
版本	更新时间							女内容					修改人
	2018.09.04		1		Defacili		止	式版					XHF
PX30 Pin No.	PX30 Pin Name	Pin Type	I/O Def	I/O Pull	Default Drive (mA)	Func 1	Func 2	Func 3	Func 4	Func5	Defualt function	RK618+CVBS_IN	Description
PART I					()								
W19	NPOR	I	I	up	4	NPOR					RESET		System reset input
W20	TVSS	I	I	down	4	TEST					VSS		connect to VSS default
U20	OSC_24M_IN	I	I	N/A	4	OSC_24M_I N					24MXIN_OSC		Oscillator 24MHz clock input
U21	OSC_24M_OUT	0	0	N/A	4	OSC_24M_O UT					24MXOUT_OSC		Oscillator 24MHz clock output
Y21	GPIO0_A0/REF_CLKO	I/O	I	down	4	GPIO0A0	clk_out_wifi				REF_CLKO	RK618_RST	Reference clock output
Y20	GPIO0_A1	I/O	ı	down	4	GPIO0A1					BT_REG_ON	BT_REG_ON	BT_REG_ON
V21	GPIO0 A2	I/O	1	down	4	GPIO0A2					WIFI_REG_ON	WIFI_REG_ON	WIFI module wake up AP
	_												
AA20	GPIO0_A3/SDMMC0_DETN GPIO0_A4/PMIC_SLEEP/TSADC_SHUT_	I/O	l	up		GPIO0A3	sdmmc0_detn	tsadc shut			SDMMC0_DET	SDMMC0_DET	SDMMC0 power control output
V20	M1	I/O	I	down		GPIO0A4	pmic_sleep	m1			PMIC_SLEEP	PMIC_SLEEP	PMIC sleep control output
T21	GPIO0_A5	I/O		up	4	GPIO0A5		, ,			TP_INT	TP_INT	Touch pannel interrupt
W21	GPIO0_A6/TSADC_SHUT_M0/TSADC_S HUTORG	I/O	I	Z		GPIO0A6	tsadc_shutm0	tsadc_shut org			TSADC_SHUT	TSADC_SHUT	Over-temperature protection reset power
Y19	GPIO0_A7	I/O	I	up	4	GPIO0A7					PMIC_INT	PMIC_INT	PMIC interrupt
N18	PLL_AVDD_1V0	Р	N/A	N/A							VDD_1V0	VDD_1V0	PLL analog power supply
	PLL_AVDD_1V8	Р	N/A	N/A							VCC_1V8	VCC_1V8	PLL analog power supply
P17	PMU_VDD_1V0	Р	N/A	N/A							VDD_1V0	VDD_1V0	PMU Post-Driver power supply
T13	OTP_VCC_1V8	Р	N/A	N/A							VCC_1V8	VCC_1V8	PMU digital I/O power supply
U19	PMUIO1	Р	N/A	N/A							VCC3V0_PMU	VCC3V0_PMU	PMUIO1 Post-Driver and digital I/O power supply
N17	AVSS	Р	N/A	N/A							VSS	VSS	pll analog power ground
PART J													
R21	GPIO0_B0/I2C0_SCL	I/O	I	up	4	GPIO0B0	i2c0_scl				I2C0_SCL_PMIC	I2C0_SCL_PMIC	I2C serial port 0,for PMIC,need external pull-up
P21	GPIO0_B1/I2C0_SDA	I/O	I	up	4	GPIO0B1	i2c0_sda				I2C0_SDA_PMIC	I2C0_SDA_PMIC	I2C serial port 0,for PMIC,need external pull-up
N20	GPIO0_B2/UART0_TX	I/O	I	down	4	GPIO0B2	uart0_tx				WIFI_WAKE_HOST	WIFI_WAKE_HOST	WIFI module wake up AP
P18	GPIO0_B3/UART0_RX	I/O	I	down	4	GPIO0B3	uart0_rx				BT_WAKE_HOST	BT_WAKE_HOST	BT module wake up AP
R18	GPIO0_B4/UART0_CTS	I/O	I	up	4	GPIO0B4	uart0_cts				TP_RST	TP_RST	Touch pannel reset
N19	GPIO0_B5/UART0_RTS/TEST_CLK1	I/O	I	up		GPIO0B5	uart0_rts	test_clk1			CHG_DET	CHG_DET	LCD panel power enable
M19	GPIO0_B7/PWM0/OTG_DRV	I/O	I	down	4	GPIO0B7	pwm_0	otg_drv			SENSOR_INT	SENSOR_INT	G-sensor interrupt
N21	GPIO0_C0/UART3_TX_M0/PWM1/PMU_D EBUG3	I/O	ı	down	4	GPIO0C0	pwm_1	uart3_txm0			LCDC_BL_PWM	LCDC_BL_PWM	LCD panel backlight brightness control
P19	GPIO0_C1/UART3_RX_M0/PWM3/PMU_ DEBUG4	I/O	I	up	4	GPIO0C1	pwm_3	uart3_rxm0			IR_IN	IR_IN	IR_IN
T20	GPIO0 C2/I2C1 SCL/UART3 CTS M0	I/O	1	down	4	GPIO0C2	i2c1_scl	uart3 ctsm			I2C1_SCL	I2C1 SCL	I2C serial port 1,for TP/Sensor,need
R20	GPIO0_C3/I2C1_SDA/UART3_RTS_M0/P MU_DEBUG5	I/O	I	down		GPIO0C3	i2c1_sda	uart3_rtsm 0			I2C1_SDA	I2C1_SDA	I2C serial port 1,for TP/Sensor,need external pull-up
P20	GPIO0_C4/CLKIO_32K	I/O	I	Z	4	GPIO0C4	clk_inout_32k				CLKOUT_32K	CLKOUT_32K	32KHz real time clock input or output
R19	FLASH_VOLSEL	I/O	Į.	up	4	GPIO0B6	flash_vol_sel				FLASH_VOLSEL	FLASH_VOLSEL	Nand Flash default power supply voltage select for boot
T19	PMUIO2	Р	N/A	N/A							VCC3V0_PMU	VCC3V0_PMU	PMUIO2 digital I/O power supply
PART B											_	_	
AA5	GPIO2_A0/CIF_D2_M0/RMII_TXEN	I/O	1	down	4	GPIO2A0	cif_d2m0	rmii_txen			RMII_TXEN	CIF_D2	Camera data port
AA8	GPIO2_A1/CIF_D3_M0/RMII_TXD1	I/O	I	down	4	GPIO2A1	cif_d3m0	rmii_txd1			RMII_TXD1	CIF_D3	Camera data port
AA7	GPIO2_A2/CIF_D4_M0/RMII_TXD0	I/O	I	down	4	GPIO2A2	cif_d4m0	rmii_txd0			RMII_TXD0	CIF_D4	Camera data port
Y6	GPIO2_A3/CIF_D5_M0/RMII_RXD0	I/O	I	down		GPIO2A3	cif_d5m0	rmii_rxd0			RMII_RXD0	CIF_D5	Camera data port
Y8	GPIO2_A4/CIF_D6_M0/RMII_RXD1	I/O	I	down	4	GPIO2A4	cif_d6m0	rmii_rxd1			RMII_RXD1	CIF_D6	Camera data port
Y7	GPIO2_A5/CIF_D7_M0/RMII_RXER	I/O	I	down	4	GPIO2A5	cif_d7m0	rmii_rxer			RMII_RXER	CIF_D7	Camera data port



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V1.1	2018.09.04							式版					XHF
PX30 Pin No.		Pin Type	I/O Def	I/O Pull	Default Drive (mA)	Func 1	Func 2	Func 3	Func 4	Func5	Defualt function	RK618+CVBS_IN	Description
W5	GPIO2 A6/CIF D8 M0/RMII RXDV	I/O	I	down	4	GPIO2A6	cif d8m0	rmii rxdv			RMII RXDV	CIF D8	Camera data port
W7	GPIO2_A7/CIF_D9_M0/RMII_MDIO	I/O	ı	down	4	GPIO2A7	cif d9m0	rmii mdio			RMII_MDIO	CIF_D9	Camera data port
U7	GPIO2_B7/CIF_D10_M0/I2C2_SCL	I/O	I	up	4	GPIO2B7	cif_d10m0	i2c2_scl			I2C2_SCL	I2C2_SCL	Camera data port, I2C serial port 1,for camera,need external pull-up
V6	GPIO2_C0/CIF_D11_M0/I2C2_SDA	I/O	I	up	4	GPIO2C0	cif_d11m0	i2c2_sda			I2C2_SDA	I2C2_SDA	Camera data port, I2C serial port 1,for camera,need external pull-up
Y4	GPIO2_B0/CIF_VSYNC_M0	I/O	I	down	4	GPIO2B0	cif_vsyncm0				HOST_WAKE_BT	CIF_VSYNC	Camera vsync input
AA4	GPIO2_B1/CIF_HREF_M0/RMII_MDC	I/O	I	down	4	GPIO2B1	cif_hrefm0	rmii_mdc			RMII_MDC	CIF_HREF	Camera href input
AA6	GPIO2_B2/CIF_CLKI_M0/RMII_CLK	I/O	I	down	4	GPIO2B2	cif_clkim0	rmii_clk			RMII_CLK	CIF_CLKI	Camera clock input
Y5	GPIO2_B3/CIF_CLKO_M0/CLK_OUT_ET HERNET	I/O	I	down	4	GPIO2B3	cif_clkom0	clk_out_eth ernet			MIPI_CLKO	CVBS_RST	Camera clock output
V12	GPIO2_B4/CIF_D0_M0/UART2_TX_M1	I/O	I	down	4	GPIO2B4	cif_d0m0	uart2_txm1			GPIO2_B4	HDMI_INT	Camera data port
V7	GPIO2_B5/PWM2	I/O	I	down	4	GPIO2B5	pwm_2				RMII_RST	CVBS_MODULE_EN	Camera power down control output for front
W6	GPIO2_B6/CIF_D1_M0/UART2_RX_M1	I/O	I	up	4	GPIO2B6	cif_d1m0	uart2_rxm1			CIF_PDN0	CVBS_INT	Camera data port
U6	VCCIO3	Р	N/A	N/A							VCC_RMII		
PART K													
J20	GPIO1_C0/UART1_RX	I/O	I	up	8	GPIO1C0	uart1_rx				UART1_RXD	UART1_RXD	UART0 serial port, for BT module
K20	GPIO1_C1/UART1_TX	I/O	I	up	8	GPIO1C1	uart1_tx				UART1_TXD	UART1_TXD	UART0 serial port, for BT module
K21	GPIO1_C2/UART1_CTS	I/O	I	up	8	GPIO1C2	uart1_cts				UART1_CTS	UART1_CTS	UART0 serial port, for BT module
L21	GPIO1_C3/UART1_RTS	I/O	I	up	8	GPIO1C3	uart1_rts				UART1_RTS	UART1_RTS	UART0 serial port, for BT module
H19	GPIO1_C4/SDMMC1_CMD	I/O	I	up	8	GPIO1C4	sdmmc1_cmd				SDIO_CMD	SDIO_CMD	SDIO0 command output,for WIFI module
M20	GPIO1_C5/SDMMC1_CLK	I/O	I	up	8	GPIO1C5	sdmmc1_clk				SDIO_CLK	SDIO_CLK	SDIO0 clock output,for WIFI module
L20	GPIO1_C6/SDMMC1_D0	I/O	I	up	8	GPIO1C6	sdmmc1_d0				SDIO_D0	SDIO_D0	SDIO0 data port ,for WIFI module
L19	GPIO1_C7/SDMMC1_D1	I/O	I	up	8	GPIO1C7	sdmmc1_d1				SDIO_D1	SDIO_D1	SDIO0 data port ,for WIFI module
M21	GPIO1 D0/SDMMC1 D2	I/O	I	up	8	GPIO1D0	sdmmc1 d2				SDIO D2	SDIO D2	SDIO0 data port ,for WIFI module
J19	GPIO1 D1/SDMMC1 D3	I/O	ı	up	8	GPIO1D1	sdmmc1_d3				SDIO D3	SDIO D3	SDIO0 data port ,for WIFI module
	VCCIO1	Р	N/A	N/A			_				VCC3V3_WL		APIO3 Post-Driver power supply
PART M												_	
B16	LVDS_TX0N/MIPI_TX_D0N/LCDC_D11_M	А	N/A	N/A							LVDS_TX0N/MIPI_TX D0N	LVDS_TX0N/MIPI_TX D0N	MIPI-DSI0 differential lane 0 positive
B17	LVDS_TX0P/MIPI_TX_D0P/LCDC_D8_M1	Α	N/A	N/A							LVDS_TX0N/MIPI_TX	LVDS_TX0N/MIPI_TX	MIPI-DSI0 differential lane 0 negative
A16	LVDS_TX1P/MIPI_TX_D1P/LCDC_D10_M 1	Α	N/A	N/A							LVDS_TX1P/MIPI_TX D1P	LVDS_TX1P/MIPI_TX D1P	MIPI-DSI0 differential lane 1 positive
B15	LVDS_TX1N/MIPI_TX_D1N/LCDC_D1_M1	Α	N/A	N/A							LVDS_TX1N/MIPI_TX _D1N	LVDS_TX1N/MIPI_TX _D1N	MIPI-DSI0 differential lane 1 negative
A14	LVDS_CLKP/MIPI_TX_CLKP/LCDC_D3_ M1	Α	N/A	N/A								LVDS_CLKP/MIPI_T X CLKP	MIPI-DSI0 differential clock lane positive
B14	LVDS_CLKN/MIPI_TX_CLKN/LCDC_D4_ M1	Α	N/A	N/A							LVDS_CLKN/MIPI_T X_CLKN	LVDS_CLKN/MIPI_T X CLKN	MIPI-DSI0 differential clock lane negative
B13	LVDS_TX2P/MIPI_TX_D2P/LCDC_D5_M1	Α	N/A	N/A							LVDS_TX2P/MIPI_TX _D2P	LVDS_TX2P/MIPI_TX	MIPI-DSI0 differential lane 2 positive
C13	LVDS_TX2N/MIPI_TX_D2N/LCDC_VSYN C_M1	Α	N/A	N/A							LVDS_TX2N/MIPI_TX _D2N	LVDS_TX2N/MIPI_TX _D2N	MIPI-DSI0 differential lane 2 negative
A12	LVDS_TX3P/MIPI_TX_D3P/LCDC_DEN_ M1	Α	N/A	N/A									MIPI-DSI0 differential lane 3 positive
B12	LVDS_TX3N/MIPI_TX_D3N/LCDC_HSYN C_M1	Α	N/A	N/A							LVDS_TX3N/MIPI_TX _D3N	LVDS_TX3N/MIPI_TX _D3N	MIPI-DSI0 differential lane 3 negative
D19	GPIO3_A0/LCDC_CLK	I/O	I	down	4	GPIO3A0	lcdc clk					lcdc_clk	LCDC pixel clk output



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版本 V1.1	更新时间 2018.09.04												修改人 XHF
PX30 Pin No.	PX30 Pin Name	Pin Type	I/O Def	I/O Pull	Default Drive (mA)	Func 1	Func 2	Func 3	Func 4	Func5	Defualt function	RK618+CVBS_IN	Description
E13	GPIO3_A1/LCDC_HSYNC_M0/CIF_D0_M 1/I2S2 2CH MCLK/UART5 RX	I/O	I	down	4	GPIO3A1	lcdc_hsyncm0	i2s2_2ch_ mclk	cif_d0m1	uart5_rx		lcdc_hsyncm0	
F13	GPIO3_A2/LCDC_VSYNC_M0/CIF_D1_M 1/I2S2_2CH_SCLK/UART5_TX	I/O	I	down	4	GPIO3A2	lcdc_vsyncm0		Joii_u IIIIII	uart5_tx		lcdc_vsyncm0	I2S2 port,for BT module
	GPIO3_A3/LCDC_DEN_M0/CIF_D2_M1/I2 S2_2CH_LRCK/UART5_CTS	1/0	I	down	4	GPIO3A3	lcdc_denm0	i2s2_2ch_lr ck	cif_d2m1	uart5_cts		lcdc_denm0	I2S2 port,for BT module
	GPIO3_A4/LCDC_D0	I/O	I	down	4	GPIO3A4	lcdc_d0				PHONE_DET1	lcdc_d0	LCDC data port
E15	GPIO3_A5/LCDC_D1_M0/CIF_D3_M1/I2S 2_2CH_SDI/UART5_RTX	I/O	I	down	4	GPIO3A5		i2s2_2ch_s di	cif_d3m1	uart5_rts		lcdc_d1m0	I2S2 port,for BT module
C14	GPIO3_A6/LCDC_D2	I/O	I	down	4	GPIO3A6	lcdc_d2					lcdc_d2	LCDC data port
	GPIO3_A7/LCDC_D3_M0/CIF_D4_M1/I2S 2_2CH_SDO	I/O	I	down	4	GPIO3A7		i2s2_2ch_s do				lcdc_d3m0	I2S2 port,for BT module
E17	GPIO3_B0/LCDC_D4_M0/CIF_D5_M1/I2S 0_8CH_SDI3	I/O	I	down	4	GPIO3B0	lcdc_d4m0	uio	on_donn			lcdc_d4m0	Power enable for RK618
F17	GPIO3_B1/LCDC_D5_M0/CIF_D6_M1/I2S 0_8CH_SDI2/SPI1_CSN	I/O	l ·	down	4	GPIO3B1	lcdc_d5m0	alZ	cif_d6m1	spi1_csn		lcdc_d5m0	Reset for RK618
B18	GPIO3_B2/LCDC_D6	I/O	I	down	4	GPIO3B2	lcdc_d6	spi1_csn1				lcdc_d6	LCDC data port
C17	GPIO3_B3/LCDC_D7/I2S0_8CH_SDI1	I/O	I	down	4	GPIO3B3	lcdc_d7	i2s0_8ch_s di1				lcdc_d7	LCDC data port
F18	GPIO3_B4/LCDC_D8_M0/CIF_D7_M1/I2S 0_8CH_SCLKRX/SPI1_MOSI	I/O	I	down	4	GPIO3B4	lcdc_d8m0	i2s0_8ch_s clkrx	cif_d7m1	spi1_mosi		lcdc_d8m0	Compass interrupt
C16	GPIO3_B5/LCDC_D9_M0/I2S0_8CH_LRC KRX	I/O	I	down	4	GPIO3B5	lcdc_d9m0	i2s0_8ch_lr ckrx				lcdc_d9m0	LCDC data port
Gio	GPIO3_B6/LCDC_D10_M0/CIF_D8_M1/I2 S0_8CH_SD03/SPI1_RXD	I/O	I	down	4	GPIO3B6	lcdc_d10m0	003	Cii_doiiii	spi1_miso		lcdc_d10m0	WIFI module power enable
G17	GPIO3_B7/LCDC_D11_M0/CIF_D9_M1/I2 S0_8CH_SDO2/SPI1_CLK	I/O	I	down	4	GPIO3B7	lcdc_d11m0	002	CII_USIIII	spi1_clk		lcdc_d11m0	LCD panel reset
A20	GPIO3_C0/LCDC_D12/I2S0_8CH_SDO1	I/O	I	down	4	GPIO3C0	lcdc_d12	i2s0_8ch_s do1				lcdc_d12	LCDC data port
B20	GPIO3_C1/LCDC_D13/I2S0_8CH_MCLK	I/O	I	down	4	GPIO3C1	lcdc_d13	i2s0_8ch_ mclk				lcdc_d13	LCDC data port
C19	GPIO3_C2/LCDC_D14/PWM4/I2S0_8CH_ LRCKTX	I/O	I	down	4	GPIO3C2	lcdc_d14	i2s0_8ch_lr	pwm_4	tdm_fsync		lcdc_d14	LCDC data port
Біз	GPIO3_C3/LCDC_D15/PWM5/I2S0_8CH_ LRCKTX	I/O	I	down	4	GPIO3C3	lcdc_d15	i2s0_8ch_s clktx	pwm_5	tdm_sclk		lcdc_d15	LCDC data port
C 16	GPIO3_C4/LCDC_D16/PWM6/I2S0_8CH_ SDO0	I/O	I	down	4	GPIO3C4	lcdc_d16	i2s0_8ch_s do0	pwm_6	tdm_sdo		lcdc_d16	LCDC data port
	GPIO3_C5/LCDC_D17/PWM7/I2S0_8CH_ SDI0	I/O	I	down	4	GPIO3C5	lcdc_d17	i2s0_8ch_s di0	pwm_7	tdm_sdi		lcdc_d17	LCDC data port
D13	GPIO3_C6/LCDC_D18/CIF_D10_M1/PDM _CLK0_M0	I/O	I	down	4	GPIO3C6	lcdc_d18	pdm_clk0m 0	cif_d10m1			lcdc_d18	LCDC data port
D14	GPIO3_C7/LCDC_D19/CIF_D11_M1/PDM _CLK1	I/O	I	down	4	GPIO3C7	lcdc_d19	pdm_clk1	cif_d11m1			lcdc_d19	LCDC data port
D15	GPIO3_D0/LCDC_D20/CIF_CLKOUT_M1/ PDM_SDI1	I/O	I	down	4	GPIO3D0	lcdc_d20	pdm_sdi1	cif_clkout m1			lcdc_d20	LCDC data port
D16	GPIO3_D1/LCDC_D21/CIF_VSYNC_M1/P DM_SDI2/ISP_PRELIGHT_TRIG	I/O	ı	down	4	GPIO3D1	lcdc_d21	pdm_sdi2	cif_vsync m1	isp_prelight_trig		lcdc_d21	LCDC data port
ווט	GPIO3_D2/LCDC_D22/CIF_HREF_M1/PD M_SDI3/ISP_FLASH_TRIGOUT	I/O	I	down	4	GPIO3D2	lcdc_d22			isp_flash_trigout		lcdc_d22	LCDC data port
D18	GPIO3_D3/LCDC_D23/CIF_CLKIN_M1/PD M_SDI0_M0/ISP_FLASH_TRIGIN	I/O	I	down	4	GPIO3D3	lcdc_d23	pdm_sdi0 m0	cif_clkinm 1	isp_flash_trigin		lcdc_d23	LCDC data port
G12	LVDS_RBIAS	Α	N/A	N/A							LVDS_RBIAS	LVDS_RBIAS	LVDS reference current generate,connect a 2K%1 resistor to VSS
F11	MIPI_DSI_VCCA_1V0	Р	N/A	N/A							VDD_1V0	VDD_1V0	LVDS/MIPI phy analog power supply
F12	MIPI_DSI_VCCA_1V8	Р	N/A	N/A							VCC_1V8	VCC_1V8	LVDS/MIPI phy analog power supply
E12	MIPI_DSI_VCCA_3V3	Р	N/A	N/A							VCC_3V0	VCC_3V0	LVDS/MIPI phy analog power supply



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	PX30 Pin Name	Pin Type	I/O Def	I/O Pull	Default Drive (mA)	Func 1	Func 2	Func 3	Func 4	Func5	Defualt function	RK618+CVBS_IN	Description
D12	VCCIO4	Р	N/A	N/A									VCCIO4 domain digital I/O power supply
PART G											VCC 3V3 mode		
	GPIO2_C1/I2S1_2CH_LRCK_TXRX	I/O	1	down	4	GPIO2C1	i2s1 2ch Irck				I2S1 LRCK TXRX	I2S1 LRCK TXRX	I2S 1 port, for RK817 audio codec
0.014	GPIO2 C2/I2S1_2CH_ SCLK	I/O	ı	down	4	GPIO2C2	i2s1_2ch_sclk				I2S1_SCLK	I2S1_SCLK	I2S 1 port, for RK817 audio codec
Y14	GPIO2 C3/I2S1 2CH MCLK	I/O	I	down	4	GPIO2C3	i2s1_2ch_mcl				I2S1_MCLK	I2S1_MCLK	I2S 1 port, for RK817 audio codec
Y15	GPIO2_C4/I2S1_2CH_SDO	I/O	I	down	4	GPIO2C4	i2s1_2ch_sdo				I2S1_SDO	12S1_SDO	I2S 1 port, for RK817 audio codec
AA13	GPIO2 C5/I2S1 SDI/PDM SDIO M1	I/O	I	down	4	GPIO2C5	i2s1_2ch_sdi	pdm_sdi0 m1			I2S1_SDI	I2S1_SDI	I2S 1 port, for RK817 audio codec
W15	GPIO2_C6/PDM_CLK0_M1	I/O	I	down	4	GPIO2C6	pdm_clk0m1				PDM_CLKO	PDM_CLKO	PDM CLK OUT
W16	VCCIO5	Р	N/A	N/A							VCC_3V0	VCC_3V0	VCCIO5 digital I/O power supply
PART H											VCCIO_SD=AUTO		
AA17	GPIO1_D2/SDMMC0_D0/UART2_TX_M0	I/O	I	up	8	GPIO1D2	sdmmc0_d0	uart2_txm0			SDMMC0_D0/UART2 _TX_M0	SDMMC0_D0/UART2 _TX_M0	SDMMC0 data port
AA18	GPIO1_D3/SDMMC0_D1/UART2_RX_M0	I/O	I	up	8	GPIO1D3	sdmmc0_d1	uart2_rxm0			_1\/_1VIU	SDMMC0_D1/UART2 _RX_M0	
AA19	GPIO1_D4/SDMMC0_D2/UART4_RX/JTA G_TCK	I/O	I	up	8	GPIO1D4	sdmmc0_d2	uart4_rx	jtag_tck		TCK	SDMMC0_D2/JTAG_ TCK	JTAG TCK for AP
AA16	GPIO1_D5/SDMMC0_D3/UART4_TX/JTA G_TMS	I/O	I	up	8	GPIO1D5	sdmmc0_d3	uart4_tx	jtag_tms		SDMMC0_D3/JTAG_ TMS	SDMMC0_D3/JTAG_ TMS	JTAG TMS for AP
Y17	GPIO1_D6/SDMMC0_CLKO/UART4_CTS/ TEST_CLK0	I/O	I	down	8	GPIO1D6	sdmmc0_clko	uart4_cts	test_clko		SDMMC0_CLK	SDMMC0_CLK	SDMMC0 clock output
Y16	GPIO1_D7/SDMMC0_CMD/UART4_RTS	I/O	I	up	8	GPIO1D7	sdmmc0_cmd	uart4_rts			SDMMC0_CMD	SDMMC0_CMD	SDMMC0 command output
Y18	VCCIO2	P	N/A	N/A							VCCIO_SD	VCCIO_SD	SDMMC0 digital I/O power supply
	SAR ADC	_											
V14	ADC_IN0	A	N/A	N/A							ADC0_HW_ID	ADC0_HW_ID	Hardware version recognition
W14	ADC_IN1	A	N/A	N/A							ADC1_HP_HOOK	ADC1_HP_HOOK	Headphone key detect
V15	ADC_IN2	A AP	N/A	N/A							ADC2_KEY_IN	ADC2_KEY_IN	AD keyboard input
	ADC_AVDD_1V8	AP	N/A	N/A							VCC_1V8	VCC_1V8	SAR-ADC analog power supply
	MIPI RX PHY MIPI CSI D0P	Α	N/A	N/A							MIPI CSI DP0	MIPI CSI DP0	MIPI-CSI0 differential lane 0 positive
	MIPI_CSI_DON	P	N/A	N/A N/A							MIPI_CSI_DN0		MIPI-CSI0 differential lane 0 positive
	MIPI_CSI_D1P	A	N/A	N/A							MIPI_CSI_DP1		MIPI-CSI0 differential lane 1 positive
	MIPI_CSI_D1N	A	N/A	N/A							MIPI_CSI_DN1		MIPI-CSI0 differential lane 1 negative
V10	MIPI_CSI_CLKP	Α	N/A	N/A							MIPI_CSI_CLKP	MIPI_CSI_CLKP	MIPI-CSI0 differential clock lane positive
U10	MIPI_CSI_CLKN	Α	N/A	N/A							MIPI_CSI_CLKN	MIPI_CSI_CLKN	MIPI-CSI0 differential clock lane negative
U9	MIPI CSI D2P	Α	N/A	N/A							MIPI CSI DP2	MIPI_CSI_DP2	MIPI-CSI0 differential lane 2 positive
	MIPI_CSI_D2N	Α	N/A	N/A							MIPI_CSI_DN2		MIPI-CSI0 differential lane 2 negative
	MIPI_CSI_D3P	Α	N/A	N/A							MIPI_CSI_DP3		MIPI-CSI0 differential lane 3 positive
	MIPI_CSI_D3N	Α	N/A	N/A							MIPI_CSI_DN3	MIPI_CSI_DN3	MIPI-CSI0 differential lane 3 negative
U11	MIPI_CSI_RBIAS	Α	N/A	N/A							MIPI_CSI_RBIAS	MIPI_CSI_RBIAS	MIPI-CSI0 reference current generate,connect a 2K%1 resistor to VSS
	MIPI_CSI_VCCA_1V0	Р	N/A	N/A							VDD_1V0	VDD_1V0	MIPI-CSI0 analog power supply
	USB 2.0 PHY											_	, , , , , , , , , , , , , , , , , , ,
Y10	USB_OTG_DP	Α	N/A	N/A							OTG_DP	OTG_DP	USB OTG Data Plus port
	USB_OTG_DM	Α	N/A	N/A							OTG_DM	OTG_DM	USB OTG Data Minus port
Y13	USB_VBUS	Α	N/A	N/A							USB_DET	USB_DET	TYPEC0 connected/vbus power detect for USB2.0



								PX30 I/O LIST				1	
版本 V1.1	更新时间 2018.09.04							改内容 三式版					修改人 XHF
DY30 Din		Pin Type	I/O Def	I/O Pull	Default Drive (mA)	Func 1	Func 2	Func 3	Func 4	Func5	Defualt function	RK618+CVBS_IN	Description
Y11	USB_ID	А	N/A	up							USB_ID	USB_ID	USB ID detect input,200kohm internal pull-up to USB_AVDD_1V8
AA12	USB_HOST_DP	Α	N/A	N/A							USB_HOST_DP	USB_HOST_DP	USB HOST Data Plus port
Y12	USB_HOST_DM	Α	N/A	N/A							USB_HOST_DM	USB_HOST_DM	USB HOST Data Minus port
AA11	USB_RBIAS	Α	N/A	N/A							USB_RBIAS	USB_RBIAS	USB PHY0(include HOST0&TYPEC0) reference current generate,connect a 133ohm resistor to VSS.
U12	USB_AVDD_1V0	Р	N/A	N/A							USB_AVDD_1V0		USB analog power supply
V13	USB_AVDD_1V8	P	N/A	N/A			<u> </u>				USB_AVDD_1V8		USB analog power supply
W13	USB_AVDD_3V3 EMMC PHY	Р	N/A	N/A							USB_AVDD_3V3	USB_AVDD_3V3	USB analog power supply
E20	GPIO1_A0/FLASH_D0/EMMC_D0/SFC_SI O0	ı	N/A	up	8	GPIO1A0	flash_d0	emmc_d0	sfc_sio0		FLASH_D0	FLASH_D0	EMMC data port
D21	GPIO1_A1/FLASH_D1/EMMC_D1/SFC_SI O1	I	N/A	up	8	GPIO1A1	flash_d1	emmc_d1	sfc_sio1		FLASH_D1	FLASH_D1	eMMC data port
C21	GPIO1_A2/FLASH_D2/EMMC_D2/SFC_SI O2	I	N/A	up	8	GPIO1A2	flash_d2	emmc_d2	sfc_sio2		FLASH_D2	FLASH_D2	eMMC data port
E19	GPIO1_A3/FLASH_D3/EMMC_D3/SFC_SI O3	I	N/A	up	8	GPIO1A3	flash_d3	emmc_d3	sfc_sio3		FLASH_D3	FLASH_D3	eMMC data port
E21	GPIO1_A4/FLASH_D4/EMMC_D4/SFC_C SN0	I	N/A	up	8	GPIO1A4	flash_d4	emmc_d4	sfc_csn0		FLASH_D4	FLASH_D4	eMMC data port
D20	GPIO1_A5/FLASH_D5/EMMC_D5	1	N/A	up	8	GPIO1A5	flash_d5	emmc_d5			FLASH_D5	FLASH_D5	eMMC data port
C20	GPIO1_A6/FLASH_D6/EMMC_D6	ı	N/A	up	8	GPIO1A6	flash_d6	emmc_d6			FLASH_D6	FLASH_D6	eMMC data port
B21	GPIO1_A7/FLASH_D7/EMMC_D7	1	N/A	up	8	GPIO1A7	flash_d7	emmc_d7			FLASH_D7	FLASH_D7	eMMC data port
F19	GPIO1_B0/FLASH_CS0	I		up	8	GPIO1B0	flash_cs0	emmc_pwr en			FLASH_CS0	_	Nand flash select0 port
H18	GPIO1_B1/FLASH_RDY/EMMC_CLKOUT/ SFC_CLK	I		up	8	GPIO1B1	flash_rdy	emmc_clko ut	sfc_clk			FLASH_RDY/EMMC_ CLK/SFC_CLK	EIVIIVIC CIOCK OUT
G19	GPIO1_B2/FLASH_DQS/EMMC_CMD	1	N/A	up	8	GPIO1B2	flash_dqs	emmc_cm d			0.0.5	FLASH_DQS/EMMC_ CMD	eMMC command port
	GPIO1_B3/FLASH_ALE/EMMC_RSTN	1	N/A	down	8	GPIO1B3	flash_ale	emmc_rstn			FLASH_ALE/EMMC_ RST	FLASH_ALE/EMMC_ RST	eMMC strobe port
GZT	GPIO1_B4/FLASH_CLE/UART3_CTS_M1/ SPI0_MOSI/I2C3_SDA	I		down	8	GPIO1B4	flash_cle	1	spi0_mosi	i2c3_sda	FLASH_CLE	FLASH_CLE	Nand flash command latch enable
П20	GPIO1_B5/FLASH_WRN/UART3_RTS_M 1/SPI0_MISO/I2C3_SCL	I		up	8	GPIO1B5	flash_wrn	uart3_rtsm 1	spi0_miso	i2c3_scl	FLASH_WRN	FLASH_WRN	Nand flash write enable
	GPIO1_B6/FLASH_CS1/UART3_TX_M1/S PI0_CSN GPIO1_B7/FLASH_RDN/UART3_RX_M1/	I	0	up	8	GPIO1B6	flash_cs1	uart3_txm1	spi0_csn		FLASH_CS1	FLASH_CS1	Nand flash select1 port
H21	SPI0 CLK	l P	NI/A	up	8	GPIO1B7	flash_rdn	uart3_rxm1	spi0_clk		FLASH_RDN	_	Nand flash read enable
J18 PART A	VCCIO6	Р	N/A	N/A							VCCIO_FLASH	VCCIO_FLASH	eMMC I/O power supply
D4		A	N/A	N/A									
R1 U3	IDDR DQ1 IDDR DQ2	A	N/A N/A	N/A N/A			1						
<u>Y2</u>	DDR DQ3	Ă	N/A	N/A									
N2 R3	DDR DQ0 DDR DQ1 DDR DQ2 DDR DQ3 DDR DQ4 DDR DQ5 DDR DQ6 DDR DQ7 DDR DQ8 DDR DQ8 DDR DQ8 DDR DQ9	A	N/A N/A	N/A N/A									
R2	DDR DQ6	Ä	N/A	N/A									
Y1 AA2	DDR DQ8	A	N/A N/A	N/A N/A									
P3	DDR DQ9	Ä	N/A	N/A									
Y3 M2	DDR DQ10	A	N/A N/A	N/A N/A									
V4	DDR DQ10 DDR DQ11 DDR DQ12 DDR DQ13 DDR DQ14 DDR DQ15	Ä	N/A	N/A									
M3 V3	DDR DQ14	A	N/A N/A	N/A N/A									
N4	DDR DQ15	A	N/A	N/A									



版本	更新时间						修改	内容					修改人
	2018.09.04			<u> </u>	Default		止	式版 I			<u> </u>		XHF
	PX30 Pin Name	Pin Type	I/O Def	I/O Pull	Drive (mA)	Func 1	Func 2	Func 3	Func 4	Func5	Defualt function	RK618+CVBS_IN	Description
F4 G3	DDR DQ16	A	N/A N/A	N/A N/A									
F3	DDR DQ18	Ä	N/A	l N/A									
K2 L2	DDR DQ19	A	N/A N/A	N/A N/A									
<u>M1</u>	DDR DQ21	A	N/A	N/A									
<u>E2</u> L1	IDDR DQ22 IDDR DQ23	A	N/A N/A	N/A N/A									
K3	DDR DQ24	À	N/A	N/A									
J4 C2	IDDR DQ25	A	N/A N/A	N/A N/A									
D2	DDR DQ27	Ä	N/A	N/A									
<u>K4</u> J3	IDDR DQ28	A	N/A N/A	N/A N/A									
<u>D1</u>	DDR DQ30	A	N/A	N/A									
<u>E1</u> W2	IDDR DQ31	A	N/A N/A	N/A N/A									
<u>W1</u>	DDR DQS0 N	A	N/A	N/A									
U2 U1	DDR DQS1 P	A	N/A N/A	N/A N/A									
<u>J2</u> J1	DDR DQ16 DDR DQ17 DDR DQ18 DDR DQ19 DDR DQ20 DDR DQ21 DDR DQ22 DDR DQ22 DDR DQ23 DDR DQ24 DDR DQ25 DDR DQ26 DDR DQ26 DDR DQ26 DDR DQ27 DDR DQ28 DDR DQ29 DDR DQ30 DDR DQ30 DDR DQ31 DDR DQS0 P DDR DQS1 P DDR DQS1 P DDR DQS2 P DDR DQS2 P DDR DQS2 P DDR DQS3 N DDR DQS3 P DDR DQS3 N DDR DQS3 P DDR DQS3 P DDR DQS3 N DDR DQS3 N DDR DQS3 N DDR DQS3 N DDR DQS4 N DDR DQS4 N DDR DQS5 N DDR DQS5 N DDR DQS4 N DDR DQS5 N DDR DQS4 N DDR DQS5 N DDR DQS5 N DDR DQS5 N DDR DQS5 N DDR DQS6 N DDR DQS6 N DDR DQS6 N DDR DQS7 P DDR DQS8 N DDR DQS8 N DDR DQS8 N DDR DQS9 N DQS N DQ	A	N/A N/A	N/A N/A									
G2	DDR DQS3 P	Ä	N/A	N/A									
<u>G1</u> T2	DDR DQS3 N	A	N/A N/A	N/A N/A									
U4	DDR DM1	Ä	N/A	N/A									
G4 M4	DDR DM2	A	N/A N/A	N/A N/A									
C7	DDR3 A0/DDR4 A10	Ä	N/A	N/A									
D10 D8	DDR3 A1/DDR4 A10	A	N/A N/A	N/A N/A									
B5	DDR3 A3/DDR4 A6	Ä	N/A	N/A									
A8 A4	DDR3 A4/DDR4 A5	A	N/A N/A	N/A N/A									
B8	DDR3 A6/DDR4 A7	A	N/A	N/A									
B4 C10	DDR3 A7/DDR4 A11 DDR3 A8/DDR4 A13	Α	N/A N/A	N/A N/A									
<u>C6</u>	DDR3 A9/DDR4 A0	A	N/A	N/A									
A10 B7	DDR3 A10/DDR4 CS0N DDR3 A11/DDR4 A3	A	N/A N/A	N/A N/A									
Ā9	DDR3 A12/DDR4 BA1	À	N/A	N/A									
D6 A7	DDR3 A13/DDR4 A2	A	N/A N/A	N/A N/A									
C9 A3	DDR3 A15/DDR4 ODT0 DDR3 BA0/DDR4 BG0	A	N/A N/A	N/A									
B10	DDR3 BA1/DDR4 CASN/DDR4 A15	A	N/A	N/A									
<u>A5</u> B3	DDR3 BA2/DDR4 BA0 DDR3 CSN0/DDR4 ACTN	A	N/A N/A	N/A N/A									
D11	DDR3 CSN1/DDR4 CS1N	Â	N/A	N/A									
B2 B1	DDR3 CLKP/DDR4 CLKP DDR3 CLKN/DDR4 CLKN	A	N/A N/A	N/A N/A									
D5	DDR3 ODT0/DDR4 WEN/DDR4 A14	Ā	N/A	N/A									
C11 A2	DDR3 ODT1/DDR4 ODT1 DDR3 RESETN/DDR4 RESETN	A	N/A N/A	N/A N/A									
D9	DDR3 CASN/DDR4 A12	Â	N/A	N/A									
C4 B11	DDR3 RASN/DDR4 CKE DDR3 CKE/DDR4 RASN/DDR4 A16	A	N/A N/A	N/A N/A									
C8	IDDR3 WEN/DDR4 BG1	Ä	N/A	N/A									
F9	DDRIO VDD 1 DDRIO VDD 2	P	N/A N/A	N/A N/A									
F10	IDDRIO VDD 3	P	N/A	N/A									
G10	DDRIO VDD 4 DDRIO VDD 5	P	N/A N/A	N/A N/A									
J6	DDRIO VDD 6 DDRIO VDD 7	P	N/A N/A	N/A N/A									
K6	DDRIO VDD 8	P	N/A	N/A									
K7	DDRIO VDD 9 DDRIO VDD 10	P	N/A N/A	N/A N/A									
L7	DDRIO VDD 11	P	N/A	N/A									
M6 M7	DDRIÓ VDD 12 DDRIÓ VDD 13	P	N/A N/A	N/A N/A									
PART N	POWER	_											
K9	LOGIC VDD 1	P	N/A N/A	N/A									
L9 K10	LOGIC VDD 2 LOGIC VDD 3	P	N/A N/A	N/A N/A									
L10	LOGIC_VDD_4	P	N/A	N/A									



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版本	更新时间						修改	女内容					修改人
V1.1	2018.09.04						Ē	式版					XHF
					Default								7
PX30 Pin	PX30 Pin Name	Pin	I/O	I/O		F 4	F 0		F 4	F	D . f f	DICOLO : OVER IN	December
No.	PX30 Pin Name	Туре	Def	Pull	Drive	Func 1	Func 2	Func 3	Func 4	Func5	Defualt function	RK618+CVBS_IN	Description
		1 ypc	501	' "	(mA)								
N11	LOGIC VDD 5 LOGIC VDD 6 LOGIC VDD 7 LOGIC VDD 8 LOGIC VDD 9	Р	N/A	N/A	` ′								
N11 N13	LOGIC VDD 6	P	N/A	N/A									
N12	LOCIC VDD 7	P	N/A	N/A									
N 12	LOGIC_VDD_1	<u> </u>	IN/A	IN/A									
M11	LOGIC VDD 8	Р	N/A	N/A									
L11	LOGIC_VDD_9	Р	N/A	N/A									
H14	ICPU VDD 1	P	N/A	N/A									
H15	CPU_VDD_2	Р	N/A	N/A									
H16	CPLL VDD 3	Р	N/A	N/A									
J14	CPU VDD 3 CPU VDD 4	P	N/A	N/A									
J15	CDL VDD 5	P	NI/A	N/A							+	+	
J15	CPU VDD 5		N/A	IN/A									
J16	CPU_VDD_6	Р	N/A	N/A									
K14	CPU VDD 7	Р	N/A	N/A									
K15	CPU_VDD_8	l P	N/A	N/A									
K16	CPU VDD 9	Р	N/A	N/A									
PART C	GROUND		T										
A1	IVSS 1	G	N/A	N/A									
Á21	VSS 2	Ğ	N/A	N/A								1	
AA21	VSS 3	Ğ	N/A	N/A									
ĀĀ1	CPU VDD 7 CPU VDD 9 GROUND VSS 1 VSS 2 VSS 3 VSS 4 VSS 5 VSS 6 VSS 7 VSS 8 VSS 9 VSS 10 VSS 11 VSS 12 VSS 13 VSS 14 VSS 15 VSS 15 VSS 16 VSS 15 VSS 16 VSS 17 VSS 18 VSS 20 VSS 21 VSS 22 VSS 23 VSS 21 VSS 22 VSS 23 VSS 25 VSS 25 VSS 25 VSS 26 VSS 27 VSS 28 VSS 29 VSS 31 VSS 27 VSS 28 VSS 29 VSS 31 VSS 31 VSS 31 VSS 31 VSS 32 VSS 33 VSS 34 VSS 34 VSS 35 VSS 35 VSS 35	Ğ	N/A	N/A N/A N/A									
A11	VSS 5	G	N/A	N/A			<u> </u>						
B6	VSS 6	Ğ	N/A	N/A N/A N/A N/A N/A N/A N/A									
B9	VSS 7	G	l N/A	N/A									
C3	VSS 8	G	N/A	N/A									
C5	VSS 9	G	N/A	N/A									
C12	VSS 10	G	N/A	N/A									
<u>D3</u>	VSS 11	G	N/A	N/A									
<u>D4</u>	VSS 12	G	N/A	N/A									
<u>D7</u>	VSS 13	<u>G</u>	N/A	N/A N/A N/A N/A N/A N/A									
<u>E3</u>	VSS 14	G	N/A	N/A									
<u> </u>	VSS 15	G	N/A	N/A									
<u> </u>	VSS 16	<u>G</u>	N/A	N/A									
<u> </u>	V66 40	<u> </u>	N/A	N/A									
<u> </u>	V	<u> </u>	N/A N/A	N/A N/A									
<u> </u>	V	6	N/A N/A	IN/A							+	+	
E9	V 3 3 2 U	6	N/A	N/A N/A N/A									
E10	VSS 21	2	N/A	N/Δ									
F5	VSS 23	6	N/A	N/A									
F11	VSS 24	Ğ	N/A	N/A									
F14	VSS 25	Ğ	N/A	N/A									
F15	VSS 26	Ğ	N/A	N/A									
F16	VSS 27	Ğ	N/A	N/A N/A									
G5	VSS 28	Ğ	N/A	N/A									
G 7	VSS 29	G	N/A	N/A									
G8	VSS 30	G	N/A	N/A									
G11	VSS 31	G	N/A	N/A									
W3	VSS 32	G	N/A	N/A									
<u>G13</u>	VSS 33	∣ <u>G</u>	N/A	N/A							1	1	
G14	VSS 34	<u>G</u>	N/A	N/A				1			1	1	
W11	VŠŠ 35 VSS 36	<u> </u>	N/A	N/A				-	-		1	1	
T12	VSS 35	<u> </u>	N/A	N/A				1	 		 	 	
H2	VSS 37	Ä	N/A	N/A				-	_		 	 	
H3	VŠŠ 38 VSS 39	K	N/A	N/A				-	-		1	1	
H4	V	<u> </u>	N/A	N/A				-	 		+	+	
H5 H7	VŠŠ 40 VSS 41	6	N/A N/A	N/A N/A				-	 		+	+	
H8	VOO 41 VOO 42	G	N/A N/A	N/A N/A				1	 		+	+	
<u>по</u> Н9	VŠŠ 42 VŠS 43	<u> </u>	N/A	N/A				+	 		1	1	
H10	IVSS 44	Ğ	N/A	N/A				1			 	 	
H11	VSS 45	Ä	N/A	N/A									
H12	IVŠŠ 46	Ğ	N/A	N/A				1	<u> </u>				
G16	VSS 45 VSS 46 VSS 47 VSS 48	Ğ	N/A	N/A					1				
G16 G15	IVŠŠ 48	Ğ	N/A	N/A					1				
l J5	IVSS 49	Ğ	N/A	N/A								1	
.18	IVSS 50	Ğ	N/A	N/A									
J9	VSS 51 VSS 52 VSS 53	Ğ	N/A	N/A									
J10	VSS 52	Ğ	N/A	N/A									
J11	VSS 53	Ğ	N/A	N/A									
J12	VSS 54 VSS 55	Ğ	N/A	N/A			<u> </u>						
H13	VSS 55	Ğ	N/A	N/A			<u> </u>						
J17	VSS 56 VSS 57 VSS 58 VSS 59	G	N/A	N/A									
H17	VSS 57	G	N/A	N/A									
K5	VSS 58	G	N/A	N/A									
K8	VSS 59	G	N/A	N/A				ļ	<u> </u>				



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<u>版本</u> V1.1	更新时间 2018.09.04	1					修成	<u> </u>					修改人 XHF
					Default		ــــــــــــــــــــــــــــــــــــــ	1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	T		T		ANF
PX30 Pin	PX30 Pin Name	Pin	I/O	I/O	Default	Func 1	Eupo 2	Eupo 2	Funo 4	Func5	Defuelt function	DI/610+C\/DC IN	Description
No.	PX30 Pin Name	Туре	Def	Pull	Drive	Func i	Func 2	Func 3	Func 4	Funco	Defualt function	RK618+CVBS_IN	Description
	VSS 60	G			(mA)								
M13 K11 M12 K12 J13 K13 L14 K17 K18 L13 L3	VSS 61	G	N/A N/A N/A	N/A N/A									
M12	VSS 62	Ğ	N/A	N/A									
K12	VSS 63	Ğ	N/A N/A	N/A									
<u>J13</u>	VSS 64	G	N/A	N/A									
K13	VSS 65	G	N/A	N/A									
L14 K17	VSS 67	G	N/A N/Δ	IN/A N/Δ									
K18	VSS 68	Ğ	N/A N/A N/A	N/A									
L13	VSS 69	Ğ	N/A	N/A									
<u>L3</u>	VSS 70	G	N/A	N/A									
<u> </u>	VSS /1	G	N/A N/A	N/A									
L3	VSS 73	G	N/A N/A	N/A N/Δ									
N14	VSS 74	Ğ	N/A	N/A									
L5 L8 N14 M14 W18 L12	VSS 75	G	N/A	N/A									
W18	VSS 76	G	N/A N/A N/A	N/A									
L12 L17	VSS 11	G	N/A	N/A N/A									
L18	VSS 79	G	N/A	N/A									
L18 M5 M8	VSS 80	Ğ	N/A	N/A									
<u>M8</u>	VSS 81	G	N/A	N/A									
M15	VSS 82 VSS 82	G	N/A	N/A					 		1		
M16 M9	VSS 60 VSS 61 VSS 62 VSS 63 VSS 64 VSS 65 VSS 66 VSS 67 VSS 68 VSS 70 VSS 70 VSS 71 VSS 72 VSS 73 VSS 74 VSS 75 VSS 75 VSS 76 VSS 78 VSS 78 VSS 78 VSS 78 VSS 78 VSS 81 VSS 82 VSS 83 VSS 84 VSS 85 VSS 88 VSS 88 VSS 88 VSS 89 VSS 90 VSS 91 VSS 93 VSS 94 VSS 95 VSS 98 VSS 98 VSS 99	G	N/A N/A	N/A					 				
M10 M17	VŠŠ 85	Ğ	N/A N/A N/A	N/A					1		1		
M17	VSS 86	Ğ	N/A	N/A									
L15	VSS 87	G	N/A	N/A									
L16	VSS 88	G	N/A N/A	N/A									
L16 N3 N5 N6	VSS 90	Ğ	N/A	N/A									
N6	VSS 91	Ğ	N/A	N/A									
N7 N8 N15	VSS 92	G	N/A	N/A									
<u>N8</u>	VSS 93	G	N/A N/A	N/A									
N15	VSS 94	G	N/A N/A	N/A N/A									
N16 N9	VSS 95	G	N/A	N/A									
N10	VSS 97	Ğ	N/A	N/A									
N10 AA3 W17	VSS 98	G	N/A	N/A									
W17	VSS 99	G	N/A N/A	N/A									
P5	VSS 100	G	N/A	N/A									
P4 P5 P6	VSS 101 VSS 102 VSS 103 VSS 104 VSS 105	Ğ	N/A	N/A N/A N/A N/A									
P7	VSS 103	G	N/A	N/A									
P8	VSS 104	G	N/A	N/A									
P9 P10	VSS 105 VSS 106		N/A N/A	N/A N/A									
P11	VSS 107	Ğ	N/A	N/A									
P12	IVSS 108	G	N/A	N/A									
P13	VŠŠ 109 VSS 110		N/A	N/A									
P14 P16	VSS 110 VSS 111	6	N/A N/A	N/A N/A					-				
P15	VSS 112	Ğ	N/A	N/A N/A									
R5	VSS 113	Ğ	N/A	N/A								<u> </u>	
R6	VSS 114	G	N/A	N/A									
R7 R8	VSS 115 VSS 116	G	N/A N/A	N/A N/A					 		1		<u> </u>
<u>R8</u> R9	VSS 116 VSS 117	G	N/A N/A	N/A N/A				+	+				
R10	IVSS 118	G	N/A	N/A									
R11	VSS 119		N/A	N/A									
R12	VSS 120	G	N/A	N/A									
R13 R14	VSS 121 VSS 122	G	N/A N/A	N/A N/A				+			1	+	
R15	IVSS 123	G	N/A	N/A					1		1		
R16	VSS 124	Ğ	N/A	N/A									
R17	VSS 125	G	N/A	N/A									
<u>T3</u> T4	VSS 126 VSS 127	G	N/A	N/A N/A				<u> </u>	-		1		
T5	VSS 127 VSS 128	G	N/A N/A	N/A N/A				+	+				
T6	VŠŠ 129	Ğ	N/A	N/A					1		1		
<u> </u>	VŠS 129 VSS 130	G	N/A	N/A									
T8	IVSS 131	G		N/A	ļ								
T9 T10	VSS 132 VSS 133	I G	N/A N/A	N/A N/A				<u> </u>	-		1		
T11	VSS 134	G	N/A N/A	N/A N/A			1		 		+		
W4	VSS 135	Ğ	N/A	N/A									



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版本	更新时间						160	<u> </u>					修改人
V1.1	2018.09.04						XHF						
_	PX30 Pin Name	Pin Type	I/O Def	I/O Pull	Default Drive (mA)	Func 1	Func 2	Func 3	Func 4	Func5	Defualt function	RK618+CVBS_IN	Description
T14	VSS 136	G	N/A	N/A									
T15 T16	VSS 130 VSS 137 VSS 138 VSS 139 VSS 140 VSS 141 VSS 142 VSS 143 VSS 144	G	N/A	N/A									
T16	VSS 138	G	N/A	N/A									
T17 T18 U5	VSS 139	G	N/A	N/A									
T18	VSS 140	G	N/A	N/A									
U5	VSS 141	G	N/A	N/A									
U14	VSS 142	G	N/A	N/A									
U14 U15 U16 U17 U18	VSS 143	G	N/A	N/A									
U16	VSS 144	G	N/A	N/A									
U17	VSS 145 VSS 146	G	N/A	N/A									
U18	VSS 146	G	N/A	N/A									
V2 V5	VSS 147 VSS 148	G	N/A	N/A									
V5	VSS 148	G	N/A	N/A									
V16	IVSS 149	G	N/A	N/A									
V17	VSS 150	G	N/A	N/A									
V18	VSS 151 VSS 152	G	N/A	N/A									
V19	VSS 152	G	N/A	N/A									