RV1126 RV1109 IO IO Domain Configuration Developer Guide

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Preface

Overview

This document mainly introduce the ways to configure IO power domain of RV1126, RV1109 SDK platform, aiming to help developers to configure IO power domain correctly.

The IO level of the controller's power domain must be matched with the IO level of the connected peripheral chip, and the voltage configuration of the software must be consistent with the voltage of the hardware.

There are 9 independent IO power domains in RV1126/RV1109, they are PMUIO[0:1] and VCCIO[1:7]. The software voltage configuration of PMUIO[0:1] and VCCIO[2:7] must be consistent with the voltage of the hardware:

- When the hardware IO level is connected to 1.8V, the software voltage configuration should also be configured to 1.8V accordingly;
- When the hardware IO level is connected to 3.3V, the software voltage configuration should also be configured to 3.3V accordingly

The hardware power supply of VCCIO1 power domain must be consistent with the up and down status of FLASH_VOL_SEL pin:

- When FLASH_VOL_SEL is low, VCCIO1 voltage must be connected to 3.3V;
- When FLASH_VOL_SEL is high, VCCIO1 voltage must be connected to 1.8V;

Otherwise:

- If the software configuration is 1.8V, but the hardware power supply is 3.3V, it will cause the low withstand voltage circuit working in overvoltage state, and the chipset will be damaged after long time working.
- If the software configuration is 3.3V, but the hardware power supply is 1.8V, the circuit will work abnormally;

Product Version

Chipset	Kernel Version
RV1126/RV1109	Kernel 4.19

Intended Audience

- Technical support engineers
- Software development engineers
- Hardware development engineers

Revision History

Version	Author	Date	Change Description
V1.0.0	CWW	2021-04-21	Initial version
V1.0.1	CWW	2021-05-12	Update the title of the fourth and fifth steps
V1.1.0	CWW	2021-05-19	Rename the name of the document
V1.2.0	CWW	2021-06-02	Update overview, third and fifth steps
V1.2.1	CWW	2021-06-19	Update reference configuration and overview
V1.2.2	Ruby	2021-08-19	Update intended audience

Contents

1. Step 1: Obtain the Hardware Schematic Diagram and Check the Design of the Hardware Power Supply

It will take RV1126_RV1109_EVB_DDR3P216SD6_V13_20200630 EVB board as an example to introduce in this document.

Hardware schematic diagram is: RV1126_RV1109_EVB_DDR3P216SD6_V13_20200630.pdf

Power solution: checking from the hardware schematic,
RV1126_RV1109_EVB_DDR3P216SD6_V13_20200630 EVB board is with a PMU (RK809-2).

2. Step 2: Find the Corresponding Kernel dts Configuration File

From the first step, it can be seen that the hardware power supply design of the EVB board is with a PMU, and the corresponding kernel dts configuration file is located in:

kernel/arch/arm/boot/dts/rv1126-evb-ddr3-v13.dts (The solution discussed in this document).

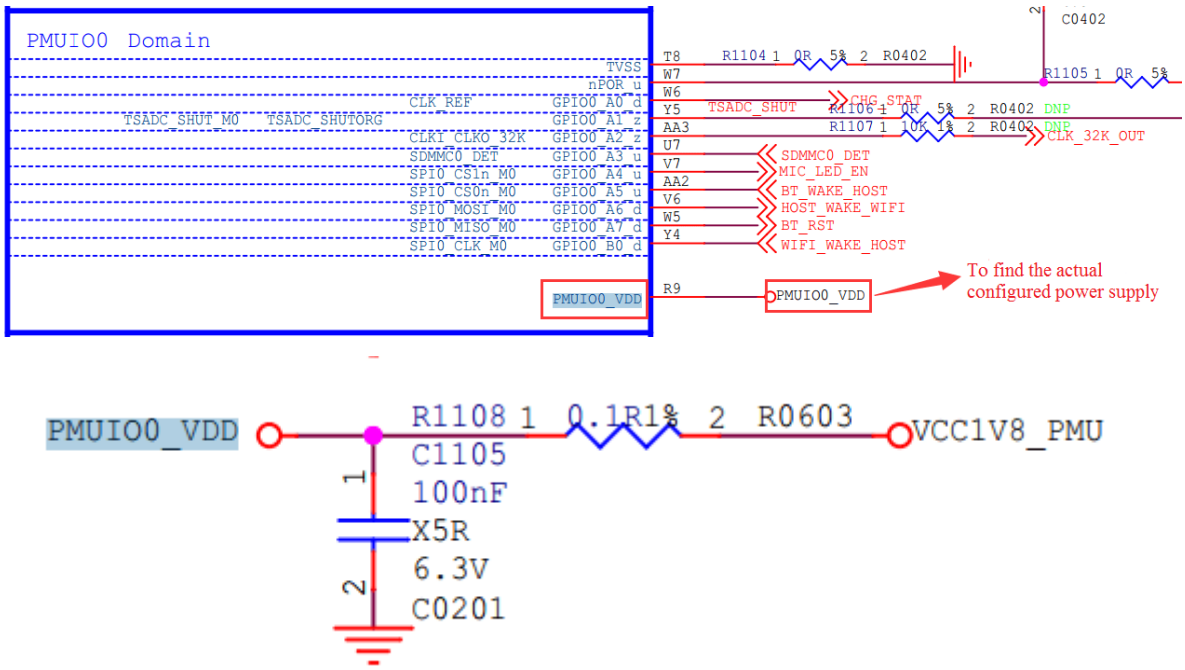
If the hardware power supply design without a PMU (that is a discrete power supply solution), the corresponding kernel dts configuration file is stored in:

kernel/arch/arm/boot/dts/rv1126-38x38-v10-emmc.dts

3. Step 3: Modify the Power Domain Configuration Node pmu_io_domains of the Kernel dts

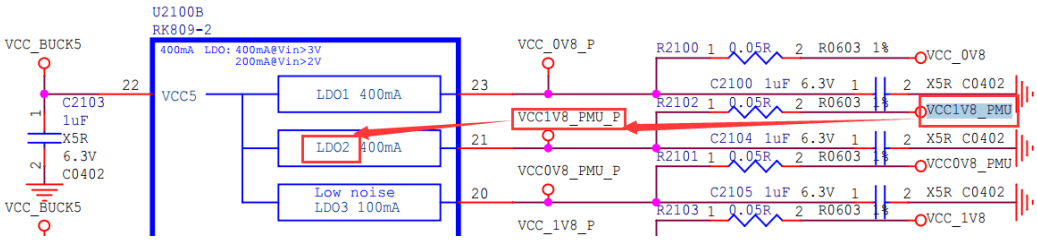
```
&pmu_io_domains {
    status = "okay";

    pmuio0-supply = <&vcc1v8_pmu>;
    pmuio1-supply = <&vcc3v3_sys>;
    vccio2-supply = <&vccio_sd>;
    vccio3-supply = <&vcc_1v8>;
    vccio4-supply = <&vcc_1v8>;
    vccio5-supply = <&vcc_3v3>;
    vccio6-supply = <&vcc_1v8>;
    vccio7-supply = <&vcc_1v8>;
};
```

Take **pmuio0-supply** as an example, firstly, check the hardware schematic diagram to confirm the configuration of the pmuio0 power domain (pmuio0_vdd) as shown in the figure.



From the schematic diagram, **PMUIO0_VDDd** is connected to **VCC1V8_PMU**, and then go to find **VCC1V8_PMU**.

PMIC RK809 LDO



Find **VCC1V8_PMU** is connected to PMIC RK809 LDO2, continue to find the voltage configuration corresponding to LDO2, as shown in the figure below:

RV1126_RV1109 Power-on Sequence

Power Name	PMIC Channel	Time Slot (step 2ms)	Default voltage	Supply Limit	Default ON/OFF	Sleep ON/OFF	Peak Current	Sleep Current
VCC_BUCK5	RK809-2 BUCK5	Slot: 1	2.2V	2.5A	ON	ON		
VCC0V8_PMU	RK809-2 LDO3	Slot: 2	0.8V	0.1A	ON	ON		
VCC_0V8	RK809-2 LDO1	Slot: 2	0.8V	0.4A	ON	OFF		
VDD_LOGIC	Ext(SY8089AAC)	Slot: 2	0.8V	2.5A	ON	OFF		
VDD_ARM	RK809-2 BUCK2	Slot: 2	0.8V	2.5A	ON	OFF		
VCC1V8_PMU	RK809-2 LDO2	Slot: 3	1.8V	0.4A	ON	ON		
VCC_1V8	RK809-2 LDO4	Slot: 3	1.8V	0.4A	ON	OFF		
VDD_NPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF		
VDD_VEPU	RK809-2 BUCK1	Slot: 2	0.8V	2.0A	ON	OFF		
VCC_DDR	RK809-2 BUCK3	Slot: 3	1.5V	1.5A	ON	ON		
VCC3V3_SYS	RK809-2 BUCK4	Slot: 4	3.3V	1.5A	ON	ON		
VCC_3V3	RK809-2 SWOUT2	Slot: 4	3.3V	1.5A	ON	OFF		
VCCIO_SD	RK809-2 LDO8	Slot: 4	3.3V	0.4A	ON	OFF		
VCC3V3_SD	RK809-2 LDO9	Slot: 4	3.3V	0.4A	ON	OFF		
VCC1V8_DOVDD	RK809-2 LDO5		1.8V	0.4A	OFF	OFF		
VCC_DVDD	RK809-2 LDO6		1.2V	0.4A	OFF	OFF		
VCC_AVDD	RK809-2 LDO7		2.8V	0.4A	OFF	OFF		
VCC5V0_HOST	RK809-2 SWOUT1		5V	2.1A	OFF	OFF		
RESET	RK809-2 sent out Reset signal for CPU(timing:10)							

NOTE:VCC_DVDD and VCC_AVDD according to camera sensor voltage

So, we can see that the configured power domain of **pmuio0-supply** is vcc1v8_pmu (that is VCC1V8_PMU in the schematic diagram, that is, 1.8V).

[Note]

- The software does not configure vccio1_vdd, and the hardware is configured according to the actual storage interface IO power domain level.
- For other power domains (pmuio1 and vccio[2:7]), please refer to the configuration steps of pmuio1 above.

4. Step 4: Check the Power Domain Configuration of the Current Firmware from the SDK

Command: `./build.sh info`

```
PLEASE CHECK BOARD GPIO POWER DOMAIN CONFIGURATION !!!!!
<<< ESPECIALLY Wi-Fi/Flash/Ethernet IO power domain >>> !!!!!
Check Node [pmu_io_domains] in the file: /home/cww/tmp/1109/kernel/arch/arm/boot/dts/rv1126-evb-ddr3-v13.dts

请再次确认板级的电源域配置！！！！！！
<<< 特别是 Wi-Fi, FLASH, 以太网这几路IO电源的配置 >>> ！！！！！
检查内核文件 /home/cww/tmp/1109/kernel/arch/arm/boot/dts/rv1126-evb-ddr3-v13.dts 的节点 [pmu_io_domains]


pmuio0-supply
regulator-min-microvolt =  1800mV
regulator-max-microvolt =  1800mV


pmuio1-supply
regulator-min-microvolt =  3300mV
regulator-max-microvolt =  3300mV


vccio2-supply
regulator-min-microvolt =  1800mV
regulator-max-microvolt =  3300mV


vccio3-supply
regulator-min-microvolt =  1800mV
regulator-max-microvolt =  1800mV


vccio4-supply
regulator-min-microvolt =  1800mV
regulator-max-microvolt =  1800mV


vccio6-supply
regulator-min-microvolt =  1800mV
regulator-max-microvolt =  1800mV


vccio7-supply
regulator-min-microvolt =  1800mV
regulator-max-microvolt =  1800mV
```

5. Step 5: Confirm whether the Register Value Is Correct after Flashing the Firmware

There are 2 ways: **check from the register directly** and **check from the boot log**

5.1 Check from registers directly

Take **RV1126/RV1109** chipset as an example, and obtain the PUMGRF_IO_VSEL register (base address: 0xFE020140) according to the manual. The description is as follows:

PMUGRF_IO_VSEL

Address: Operational Base + offset (0x0140)

Bit	Attr	Reset Value	Description
31:16	WO	0x0000	write_enable Write enable for lower 16bits, each bit is individual. 1'b0: Write access disable 1'b1: Write access enable
15:10	RO	0x00	reserved
9	RW	0x0	pmuio1_vsel PMUIO1 voltage selection. 1'b0: 3.3V 1'b1: 1.8V
8	RW	0x0	pmuio0_vsel PMUIO0 voltage selection. 1'b0: 3.3V 1'b1: 1.8V
7	RW	0x0	vccio7_vsel VCCIO7 voltage selection. 1'b0: 3.3V 1'b1: 1.8V
6	RW	0x0	vccio6_vsel VCCIO6 voltage selection. 1'b0: 3.3V 1'b1: 1.8V
5	RW	0x0	vccio5_vsel VCCIO5 voltage selection. 1'b0: 3.3V 1'b1: 1.8V
4	RW	0x0	vccio4_vsel VCCIO4 voltage selection. 1'b0: 3.3V 1'b1: 1.8V
3	RW	0x0	vccio3_vsel VCCIO3 voltage selection. 1'b0: 3.3V 1'b1: 1.8V
2	RW	0x0	vccio2_vsel VCCIO2 voltage selection. 1'b0: 3.3V 1'b1: 1.8V
1	RW	0x0	vccio1_vsel VCCIO1 voltage selection. 1'b0: 3.3V 1'b1: 1.8V

```
# io -4 -r 0xFE020140
fe020140:  000001d8
```

5.2 Check from boot log

```
dmesg |grep io-domains|grep supplied

rockchip-iodomain fe020000.syscon:io-domains: vccio2(3300000 uV) supplied by
vccio_sd
rockchip-iodomain fe020000.syscon:io-domains: vccio3(1800000 uV) supplied by
vcc_1v8
rockchip-iodomain fe020000.syscon:io-domains: vccio4(1800000 uV) supplied by
vcc_1v8
rockchip-iodomain fe020000.syscon:io-domains: vccio5(3300000 uV) supplied by
vcc_3v3
rockchip-iodomain fe020000.syscon:io-domains: vccio6(1800000 uV) supplied by
vcc_1v8
rockchip-iodomain fe020000.syscon:io-domains: vccio7(1800000 uV) supplied by
vcc_1v8
rockchip-iodomain fe020000.syscon:io-domains: pmuio0(1800000 uV) supplied by
vcc1v8_pmu
rockchip-iodomain fe020000.syscon:io-domains: pmuio1(3300000 uV) supplied by
vcc3v3_sys
```

If you have opened debugfs, you can also check from the corresponding node as follows:

```
ls /sys/kernel/debug/iodomain
pmuio0  pmuio1  vccio2  vccio3  vccio4  vccio5  vccio6  vccio7

cat /sys/kernel/debug/iodomain/pmuio1/voltage
3300000
```