GURURAJA GONAL

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OBJECTIVE

Electronics and Communication Engineering undergraduate with a strong foundation in Digital Design and Verification, specializing in RTL development and functional verification using SystemVerilog and UVM. Experienced in building constrained-random testbenches and debugging at both RTL and gate levels. Eager to contribute to the world of semiconductors, bringing a passion for silicon validation and collaborative problem-solving in high-performance chip development environments.

EXPERIENCE

K-VLSI: Digital VLSI Design (IIIT-B) (Currently Pursuing)

- Recognized as one of the top candidates from Karnataka for a distinguished 6-month VLSI Design internship and training program, collaboratively hosted by IIIT-Bangalore, IESA, SAFL, and KDEM.
- Developed and executed constrained-random, coverage-driven verification environments using SystemVerilog and UVM.
- Underwent structured training based on an industry-relevant syllabus covering RTL design, static timing analysis, and CMOS circuit fundamentals using Verilog and SystemVerilog.
- Actively participating in advanced training led by IIIT-Bangalore faculty and industry experts, with focused mentorship and guest lectures; approaching program completion.

TECHNICAL SKILLS

EDA Tools	Cadence Virtuoso, ModelSim, Quartus Prime, Vivado, Silvaco TCAD
HDLs	Verilog, SystemVerilog, UVM
Verification Concepts	Constrained-Random, Coverage-Driven, Assertion-Based Verification
Programming Languages	Python, C++
Scripting Languages	Python and basic Perl
Fundamentals	Digital, Analog and Basic Electronics, ASIC Design Flow, FSM, STA
Soft Skills	Problem Solving, Written and Communication Skills, Time Management

EDUCATION

International Institute of Information Technology, Bengaluru (IIIT-B) Currently Pursuing

PG Diploma in VLSI

Dayananda Sagar College of Engineering, Bengaluru 2021-2025

Bachelor of Engineering CGPA-8.29

Siddaganga P.U College, Davanagere 2019-2021

Pre-University Percentage-99.5

Deepayan English Medium School, Hosapete 2019

High School Percentage-91.36

PROJECTS

Design And Implementation Of 5-Stage Pipelined RISC-V Processor

- Designed and implemented a 5-stage pipelined RISC-V processor focusing on Fetch, Decode, Execute, Memory, and Write back stages.
- Developed the processor architecture and control logic using Verilog HDL. Verified functionality through simulation and ensured proper instruction flow across pipeline stages.

SystemVerilog-Based Testbench for SPI Slave Verification

- Designed and implemented a complete SystemVerilog testbench environment to verify an SPI Slave module.
- The architecture included modules and classes such as the DUT, generator, driver, monitor, scoreboard, mailbox, interface, and transaction-level classes.
- Verified protocol correctness, edge case handling, and data consistency through simulation and functional checks.

RTL Design for a simple ATM and Washing Machine using FSM methodology

- Designed RTL models for a simple ATM and Washing Machine system using Finite State Machine (FSM) methodology.
- Implemented control logic for user interactions, mode selection, and operation sequencing using Verilog.
- Simulated and verified the functionality using testbenches to ensure correct state transitions and outputs.

I2C and UART Protocol Implementation through Verilog

- Designed and implemented I2C and UART modules using Verilog, focusing on efficient data communication between master and slave devices.
- The modules support various communication modes, ensuring reliable data transfer and synchronization. Optimized the design for low latency and high-speed operation in embedded systems.

RTL Design For Memory BIST

- Designed an RTL-based Memory Built-In Self-Test (MBIST) architecture to automate memory testing and fault detection
- Implemented at-speed testing techniques to ensure reliability and identify manufacturing defects efficiently. Enabled structured access to embedded memory blocks for comprehensive verification and validation.

ACHIEVEMENTS

Best Socially Relevant project for Design of Double Gate Double Material TFET for Biosensing Application

Designed and simulated a DG DM T-FET using TCAD for liver cancer biosensing applications. The project aimed to detect liver cancer by testing the presence of cancerous cells via the variation of the drain current of the T-FET for non-cancerous and cancerous cells. This project was awarded the Best Socially Relevant Project at the College Open Day.

CERTIFICATIONS

VLSI Physical Design With Static Timing Analysis (IIT-Roorkee)

This NPTEL course covers the complete VLSI physical design flow, including partitioning, chip planning, placement, routing, clock routing, and static timing analysis. It provides in-depth knowledge of key design steps essential for VLSI chip development.

AI/ML for Geo-Data Analysis by ISRO (ISRO IIRS)

Gained foundational knowledge of AI/ML techniques for geospatial data analysis. Explored applications of machine learning in satellite imagery processing and geographic pattern recognition. Learned essential methods for extracting insights from geospatial datasets.