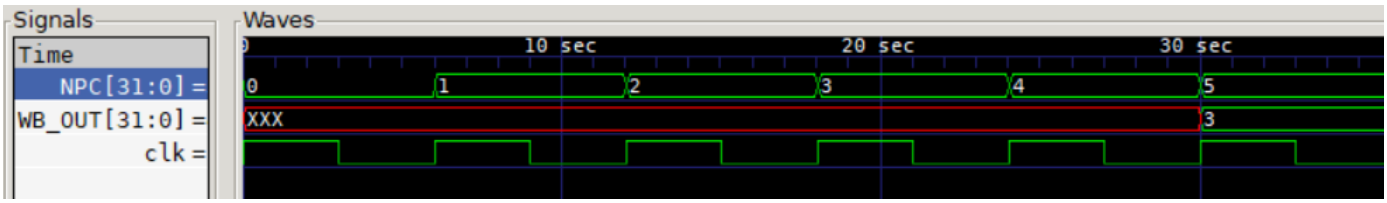
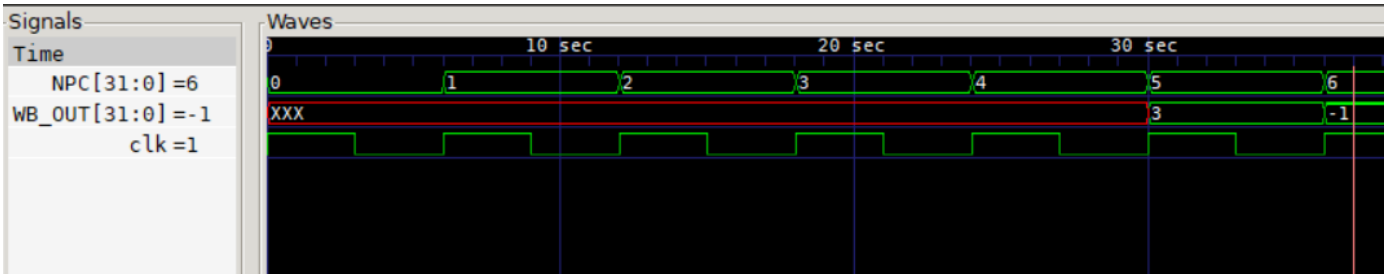
Waveforms of RISC-V Core Verilog Netlist and Testbench for RISC-V Core

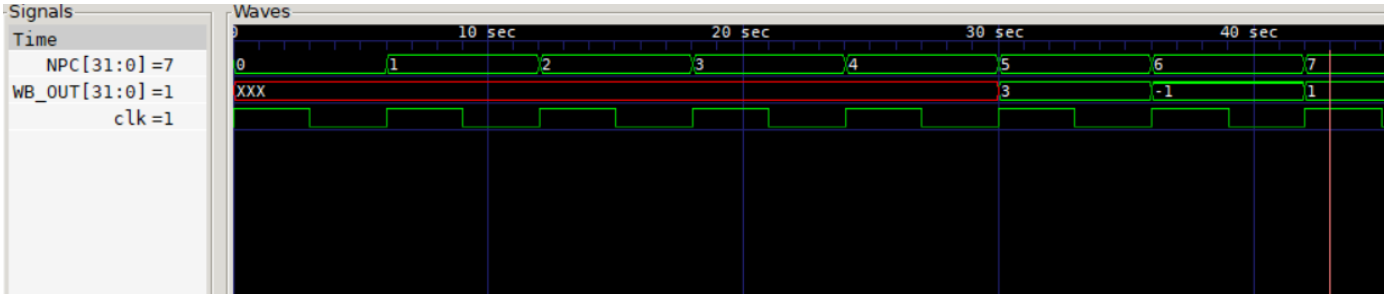
Instruction 1: add r6,r1,r2



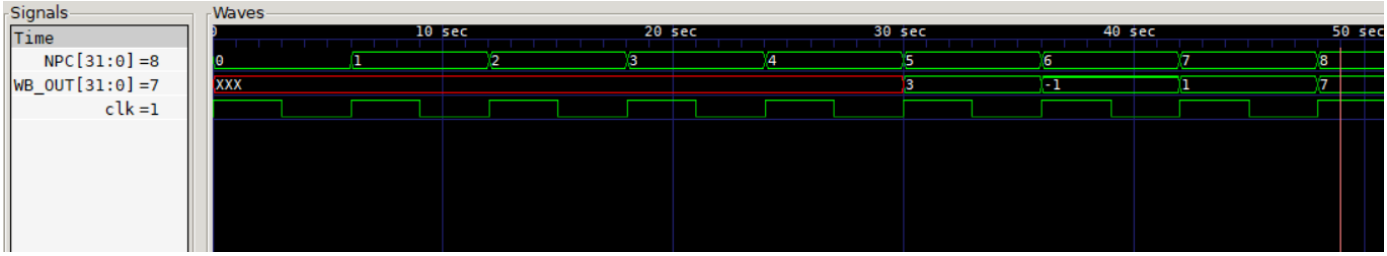
Instruction 2: sub r7,r1,r2



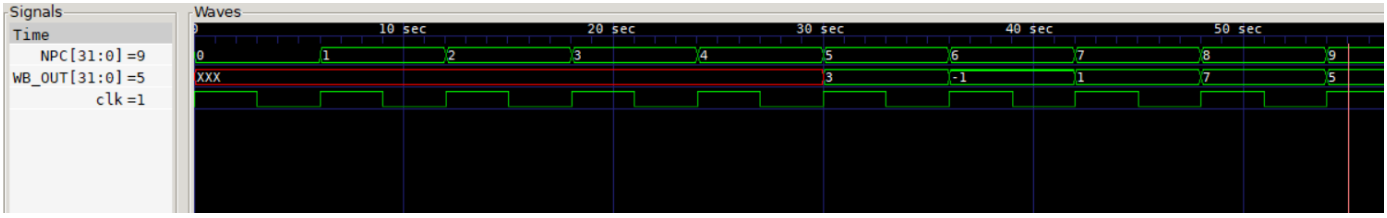
Instruction 3: and r8,r1,r3



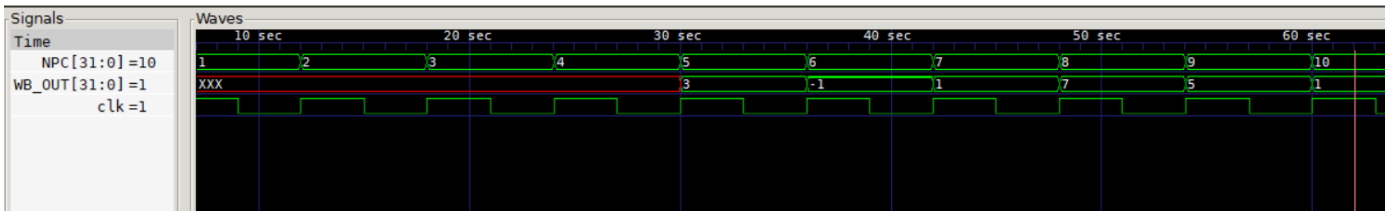
Instruction 4: or r9,r2,r5



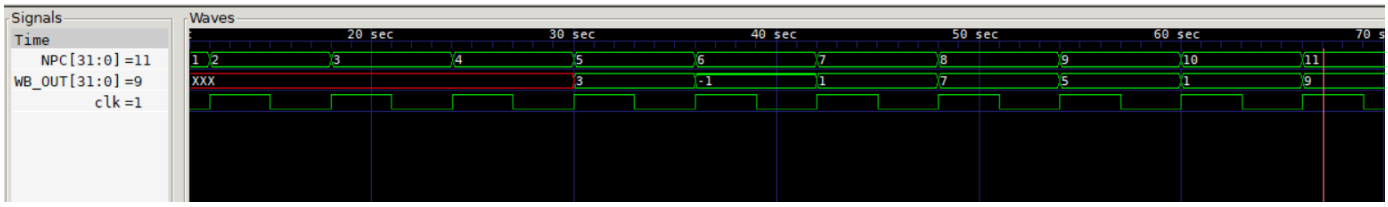
Instruction 5: xor r10,r1,r4



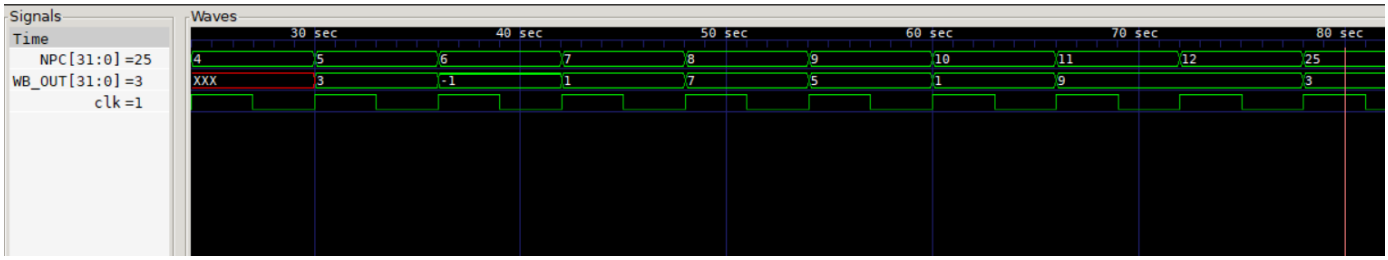
Instruction 6: slt r11,r2,r4



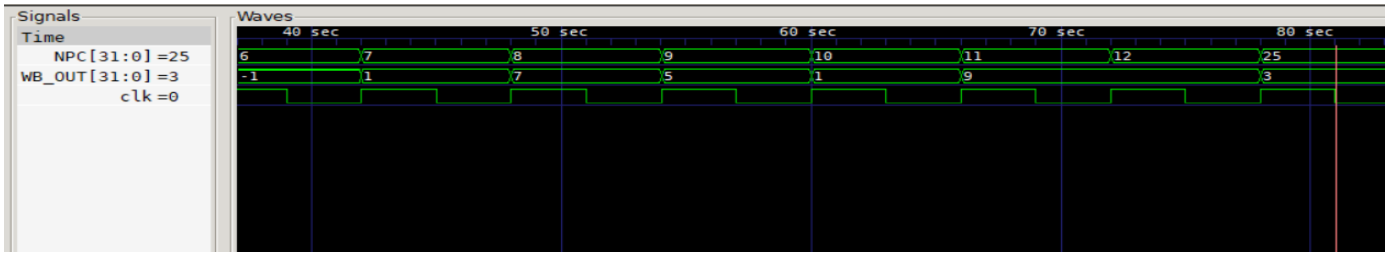
Instruction 7: addi r12,r4,5



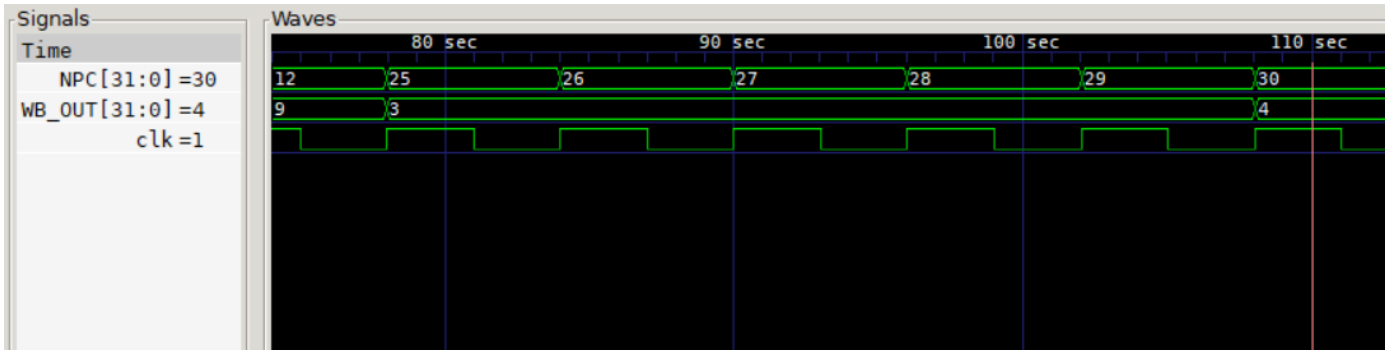
Instruction 8: sw r3,r1,2



Instruction 9: lw r13,r1,2



Instruction 10: beq r0,r0,15



Instruction 11: add r14,r2,r2