1.

a. Assuming a single-cycle processor, the total number of clock cycles for both files, prob1softfloat and prob1hardfloat, would be 19644 and 11578, respectively. This is because we use the raw instruction count and multiply that by 1 since we use a single-cycle processor.
   Furthermore, 19644 - 11578 = 8066 additional instructions are needed to make the software multiplier compared to the hardware multiplier.
   8066/19644 is the fraction of the cycles the software multiplication function requires.

b. The part of the application that will most benefit from a hardware multiplier is the multiply function used in software (prob1softfloat). We know that the hardware multiply is around 8066 times faster (if it loops once)(depending on the looping conditions, this could change), and the multiplication takes about 41% of the cycles.
   Using Amdahl Law, the SpeedUp = 1 / ( (1 - 0.41) + 0.41 / 8066 ) = 1.695
   This is confirmed using the clock cycles, 19644/11578 = 1.696.

c. With a slower clock frequency, the speedup for the multiply function would be 25% less of the speedup before (1.69 – 25% = 1.27).
   Using Amdahl Law, the SpeedUp = 1 / ( (1 - 0.41) + 0.41 / 1.27 ) = 1.10
   Therefore, the hardware is 1.1 times faster than the software multiply function.

2.

a. The cycle time for the worst-case latency for the pipelined processor is DMEM, which is 270ps. DMEM sets the cycle time because it takes the longest to complete, meaning all the other stages must be set to the same cycle time. Regarding instructions, loading/storing words would be the worst-case for the pipelined processor.
b. For the single-cycle processor, the worst case would be a load instruction, the same as part a. However, the single-cycle processor must go through all the components in one cycle. This evaluates to the minimum clock cycle being 775ps. This includes the IMEM (230ps), RegRead (120ps), ALU (130ps), DMEM (270ps), and the Mux at the MemToReg (25ps).
   The calculation for CPI:
   775/270 = 2.87 CPI
   The CPI needs to be 3 for the pipeline design to benefit performance.