Gurumanie Singh Dhiman
CprE 381 Homework 11

[Note: This is your final homework of the semester. These problems will help you gain some familiarity with virtual memory and its implications for hardware.]

1. Virtual Memory
    a. ZyBooks (Textbook) 5.19.16.a-e
    Assume 4 KiB pages, a 4-entry fully associative TLB, and true LRU replacement. If pages must be brought in from disk, increment the next largest page number.

a) 2^2 * 2^10 = 2^12, 12 offset bits
(In this case, the very first page fault is replaced in the last index since the valid bit = 0, after using up the row with 0 as a valid bit, the first row is assumed to be replaced.)

	VPN	PO	TLB	PT	PageFault
1) 4669	0001	0010 0011 1101	Miss	Miss	yes
2) 2227	0000	1000 1011 0011	Miss	Hit	No
3) 13916	0011	0110 0101 1100	Hit	Hit	No
4) 34587	1000	0111 0001 1011	Miss	Miss	yes
5) 48870	1011	1110 1110 0110	Miss	Hit	No
6) 12608	0011	0001 0100 0000	Hit	Hit	No
7) 49225	1100	0000 0100 1001	Miss	Miss	yes

TLB State:

0.

Valid	Tag	PPN
1	11	12
1	7	4
1	3	6
0	4	9

1.

Valid	Tag	PPN
1	11	12
1	7	4
1	3	6
1	1	13

2.

Valid	Tag	PPN
1	0	5
1	7	4
1	3	6
1	1	13

3.

Valid	Tag	PPN
1	0	5
1	7	4
1	3	6
1	1	13

4.

Valid	Tag	PPN
1	0	5
1	8	14
1	3	6
1	1	13

5.

Valid	Tag	PPN
1	0	5
1	8	14
1	3	6
1	11	12

6.

Valid	Tag	PPN
1	0	5
1	8	14
1	3	6
1	11	12

7.

Valid	Tag	PPN
1	12	15
1	8	14
1	3	6
1	11	12

b) 2^4 * 2^10 = 2^14, 14 offset bits

(In this case, the very first page fault is replaced in the last index since the valid bit = 0, after using up the row with 0 as a valid bit, the first row is assumed to be replaced.)

		VPN	PO	TLB	PT	PageFault
1)	4669	00	01 0010 0011 1101	Miss	Hit	No
2)	2227	00	00 1000 1011 0011	Hit	Hit	No
3)	13916	00	11 0110 0101 1100	Hit	Hit	No
4)	34587	10	00 0111 0001 1011	Miss	Miss	yes
5)	48870	10	11 1110 1110 0110	Hit	Hit	No
6)	12608	00	11 0001 0100 0000	Hit	Hit	No
7)	49225	11	00 0000 0100 1001	Hit	Hit	No

TLB State:

0.

Valid	Tag	PPN
1	11	12
1	7	4
1	3	6
0	4	9

1.

Valid	Tag	PPN
1	11	12
1	7	4
1	3	6
1	0	5

2.

Valid	Tag	PPN
1	11	12
1	7	4
1	3	6
1	0	5

3.

Valid	Tag	PPN
1	11	12
1	7	4
1	3	6
1	0	5

4.

Valid	Tag	PPN
1	2	13
1	7	4
1	3	6
1	0	5

5.

Valid	Tag	PPN
1	2	13
1	7	4
1	3	6
1	0	5

6.

Valid	Tag	PPN
1	2	13
1	7	4
1	3	6
1	0	5

7.

Valid	Tag	PPN
1	2	13
1	7	4
1	3	6
1	0	5

There are more hits in this case when compared to part a. This also means smaller page tables are needed for the same virtual memory range. A disadvantage of this is that there is a reduction in the TLB granularity as discussed in lecture, since 4KiB pages allow for more bits in memory mapping (4 Tag bits in 4KiB compared to 2 in 16KiB).

c) 2^2 * 2^10 = 2^12, 12 offset bits

(In this case, the very first page fault is replaced in the last index since the valid bit = 0, after using up the row with 0 as a valid bit, the first row is assumed to be replaced.)

		VPN	PO	TLB	PT	PageFault
1)	4669	0001	0010 0011 1101	Miss	Hit	No
2)	2227	0000	1000 1011 0011	Miss	Hit	No
3)	13916	0011	0110 0101 1100	Miss	Miss	yes
4)	34587	1000	0111 0001 1011	Miss	Hit	No
5)	48870	1011	1110 1110 0110	Miss	Hit	No
6)	12608	0011	0001 0100 0000	Hit	Hit	No
7)	49225	1100	0000 0100 1001	Miss	Miss	yes

set

TLB State:

0.

	Valid	Tag	PPN
0	1	11	12
1	1	7	4

	Valid	Tag	PPN
0	1	3	6
1	0	4	9

1.

	Valid	Tag	PPN
0	1	11	12
1	1	7	4

	Valid	Tag	PPN
0	1	3	6
1	1	6	5

2.

	Valid	Tag	PPN
0	1	0	5
1	1	7	4

	Valid	Tag	PPN
0	1	3	6
1	1	0	5

3.

	Valid	Tag	PPN
0	1	0	5
1	1	1	13

	Valid	Tag	PPN
0	1	3	6
1	1	0	5

4.

	Valid	Tag	PPN
0	1	0	5
1	1	1	13

	Valid	Tag	PPN
0	1	4	9
1	1	0	5

5.

	Valid	Tag	PPN
0	1	0	5
1	1	1	13

	Valid	Tag	PPN
0	1	4	9
1	1	5	11

6.

	Valid	Tag	PPN
0	1	0	5
1	1	1	13

	Valid	Tag	PPN
0	1	4	9
1	1	5	11

7.

	Valid	Tag	PPN
0	1	6	14
1	1	1	13

	Valid	Tag	PPN
0	1	4	9
1	1	5	11

d) 2^2 * 2^10 = 2^12, 12 offset bits

(In this case, the very first page fault is replaced in the first index)

		VPN	PO	TLB	PT	PageFault
1)	4669	0001	0010 0011 1101	Miss	Hit	No
2)	2227	0000	1000 1011 0011	Miss	Hit	No
3)	13916	0011	0110 0101 1100	Miss	Miss	yes
4)	34587	1000	0111 0001 1011	Miss	Hit	No
5)	48870	1011	1110 1110 0110	Miss	Hit	No
6)	12608	0011	0001 0100 0000	Miss	Hit	No
7)	49225	1100	0000 0100 1001	Miss	Hit	No

index bits

TLB State:

0.

Valid	Tag	PPN
1	11	12
1	7	4
1	3	6
0	4	9

1.

Valid	Tag	PPN
1	11	12
1	0	5
1	3	6
0	4	9

2.

Valid	Tag	PPN
1	0	5
1	0	5
1	3	6
0	4	9

3.

Valid	Tag	PPN
1	11	12
1	0	5
1	3	6
1	0	5

4.

Valid	Tag	PPN
1	2	13
1	0	5
1	3	6
0	4	9

5.

Valid	Tag	PPN
1	11	12
1	0	5
1	3	6
1	2	13

6.

Valid	Tag	PPN
1	11	12
1	0	5
1	3	6
1	0	5

7.

Valid	Tag	PPN
1	3	6
1	0	5
1	3	6
0	4	9

e) A CPU must have a TLB for high performance because without the use of a TLB, each memory access would require a full page table lookup which would increase the access latency. Without the use of a TLB, every access to memory would need a full page table walk in order to translate the VPN to PPN.

b. ZyBooks (Textbook) 5.19.17a-c

a) #PTEs = Virtual Address / Page Size = 2^32 / (2^3 * 2^10) = 2^32 / 2^13 = 2^19 PTEs
Page Table Size = #PTEs * sizePTE = 2^19 * 2^2 = 2^21 bytes
Page Table Size (for half memory) = 2^21 / 2^1 = 2^20 bytes (1 MiB)
Page Table Size (for 5 applications) = 2^20 * 5 = 5 MiB

b) #PTEs (First Level) = 256 (2^8) entries (given)
Total #PTEs = 2^19 entries (from part a)
#PTEs (Second Level) = 2^(19 – 8) = 2^11 entries
sizePTE = 2^11 * 4 = 8 KiB (use sizePTE from part a)
Virtual Address = 2^11 * (2^3 * 2^10) = 2^24

Assuming half the memory:
2^31 bytes (since VA bits in part a = 32)
Then,
Second Level (Minimum) = 5 * (2^31/2^24) * 8 KiB = 5 MiB
First Level (Minimum) = 5 * 128 * 6 B = 3840 B
Second Level (Maximum) = 5 * 256 * 8 KiB = 10 MiB
First Level (Maximum) = 5 * 256 * 6 B = 7680 B

c) The page index is 13 bits (address bits 12 down to 0)
16 KiB direct-mapped cache with two 64-bit words per block would have 16-byte blocks.
Which translates to:
16 KiB/16 B = 1024 blocks = 2^10, so 10 index bits
16 KiB = 2^4, so 4 offset bits
Therefore, the index would extend outside of the page index. The designer could increase the cache's associativity. This would reduce the number of index bits so that the cache's index fits completely inside the page index.

2. Exam 3 Question

Develop your own exam question (roughly 10-15 points) from control hazards, memory technologies, caches, and virtual memory. Your question shouldn't simply ask students to recall information, but should ask for an application of a concept or require understanding of a concept or need analysis of a processor/application. You must include a correct and complete solution to your question. This question should be your own work and not copied from a book or an old exam. ***Post your question and solution to the Exam3 channel for others to use.***

Posted on Teams.