CS546 "Parallel and Distributed Processing"
Homework 4

Submission:
Due by 11:59pm of 10/29/2019
Total points 150 - Late penalty: 10% penalty for each day late
Please upload your assignment on Blackboard with the following name:
CS546_SectionNumber_LastName_FirstName_HW4.
Please do NOT email your assignment to the instructor and/or TA!

1. **(10 points)** What is the typical performance pitfall of (distributed memory) parallel processing?
2. **(10 points)** You are given a non-pipelined processor design which has a cycle time of 10ns.
   (1) What is the best speedup you can get by pipelining it into 5 stages?
   (2) If the 5 stages are 1ns, 1.5ns, 4ns, 3ns and 0.5ns, what is the best speedup you can get compared to the original processor?
3. **(10 points)** How does cache associativity affect the cache performance?
4. **(10 points)** Just providing deeper memory hierarchies does NOT bridge the gap between processor and memory performance. Why?
5. **(15 points)** Derive the formula for calculating the current average access time (C-AMAT) for a word in the first level cache of a system. Assume the following values for a theoretical system containing an L1 cache.

Location	Hit Time	Hit Concurrency	Pure Miss Rate	Pure Miss Concurrency	Pure Miss Penalty
L1	5ns	3	35%	5	1000ns

   Determine the current average access time for a memory word in the described system.

6. **(15 points)** Derive the **recursive** formula for calculating the current average access time (C-AMAT) for a word in a system with three levels of cache. Assume the following values for a theoretical system containing an L1, L2, and L3 cache.

Location	Hit Time	Hit Concurrency	Pure Miss Rate	η
L1	5ns	2.75	45%	1.5
L2	10ns	3.25	30%	2.25
L3	35ns	4.5	15%	4
Main Memory	100ns	6	0	0

   Determine the current average access time for a memory word in the described system.
   Hint:

$$C\text{-}AMAT_1 = \frac{H_1}{C_{H_1}} + pMR_1 \times \eta_1 \times C\text{-}AMAT_2$$

Where

$$C\text{-}AMAT_1 = \frac{H_1}{C_{H_1}} + pMR_1 \times \frac{pAMP_1}{C_{M_1}}$$

$$C\text{-}AMAT_2 = \frac{H_2}{C_{H_2}} + pMR_2 \times \frac{pAMP_2}{C_{M_2}}$$

$$\eta_1 = \frac{pAMP_1}{AMP_1} \times \frac{C_{m_1}}{C_{M_1}}$$

7. **(10 points)** How to optimize the following code to reduce the **miss rate** of a memory system? Please give the optimized code and explain why briefly.

```
for (i = 0; i < N; i++) {
    A[i] = B[i] + C[i];
}
for (i = 0; i < N; i++) {
    D[i] = B[i] + A[i];
}
```

8. **(10 points)** What are the hardware technologies which can increase **Hit Concurrency** in the formula of C-AMAT and explain why briefly?

9. **(10 points)** What is the Non-block cache and what are its characteristics?

10. **(10 points)** What is memory stall time? What is the advantage of the Layered Performance Matching method? Why LPM can improve memory performance (in terms of memory stall time) by more than one hundred times?

11. **(10 points)** What is Pace Data Transfer? Can we achieve Pace Data Transfer?

12. **(15 points)** The following Figure 1 shows a cycle-accurate C-AMAT example. In this example, there are 10 data accesses in L1 cache. Among these data accesses, data access 1, 3, 5 are hit data accesses, others are miss data accesses. As Figure 1 shows, the green cycles are hit cycles and the black cycles are miss cycles. (hint: please be careful about what is the difference of miss data access and pure miss data access)

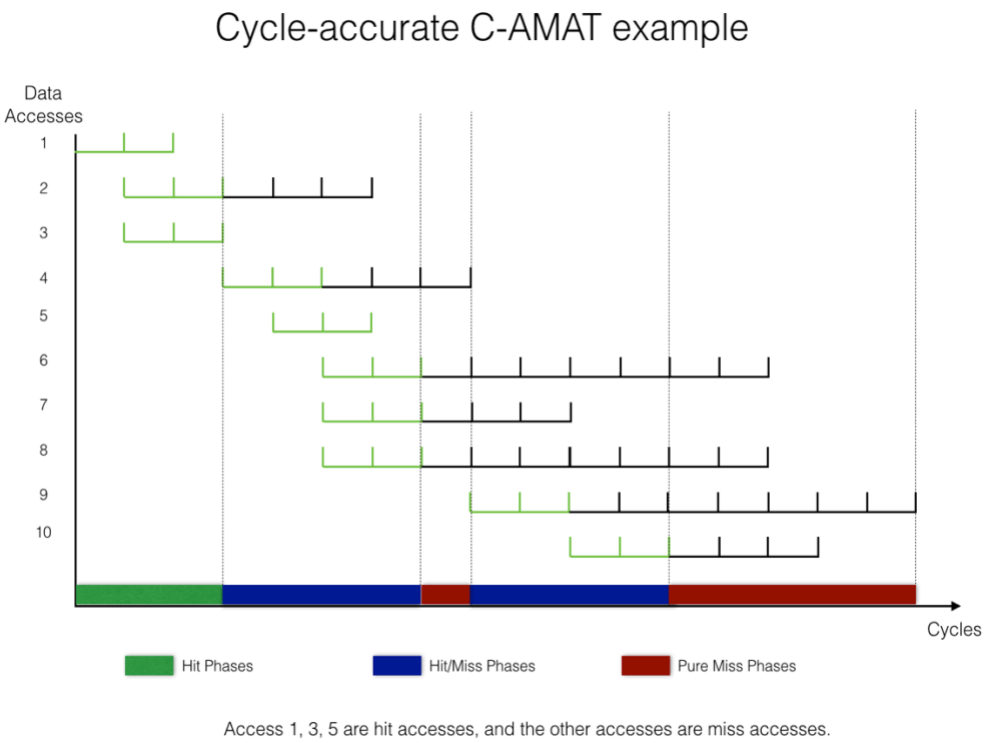

Figure 1. Cycle-accurate C-AMAT Example

Please calculate the AMAT and C-AMAT value of this example in this Figure 1.

13. **(15 points)** In this following table, one set of AMAT and other parameters in L1 cache are given. Is it possible to use the given AMAT and other parameters to calculate C-AMAT in L1 cache? If it is possible, please calculate it and explain why?

Location	Hit Time	Hit Concurrency	Miss Concurrency	K	AMAT
L1	3ns	1.5	2	0.3	50ns

Note: We encourage collaboration between you and your classmates. Discuss various approaches and techniques to better understand the questions. However, we do NOT allow copying solutions or code. This is considered as cheating and falls under IIT code of honor. Penalties will be enforced. Please make sure you write your own solutions.
GOOD LUCK!