

CS570 “Advanced Computer Architecture”

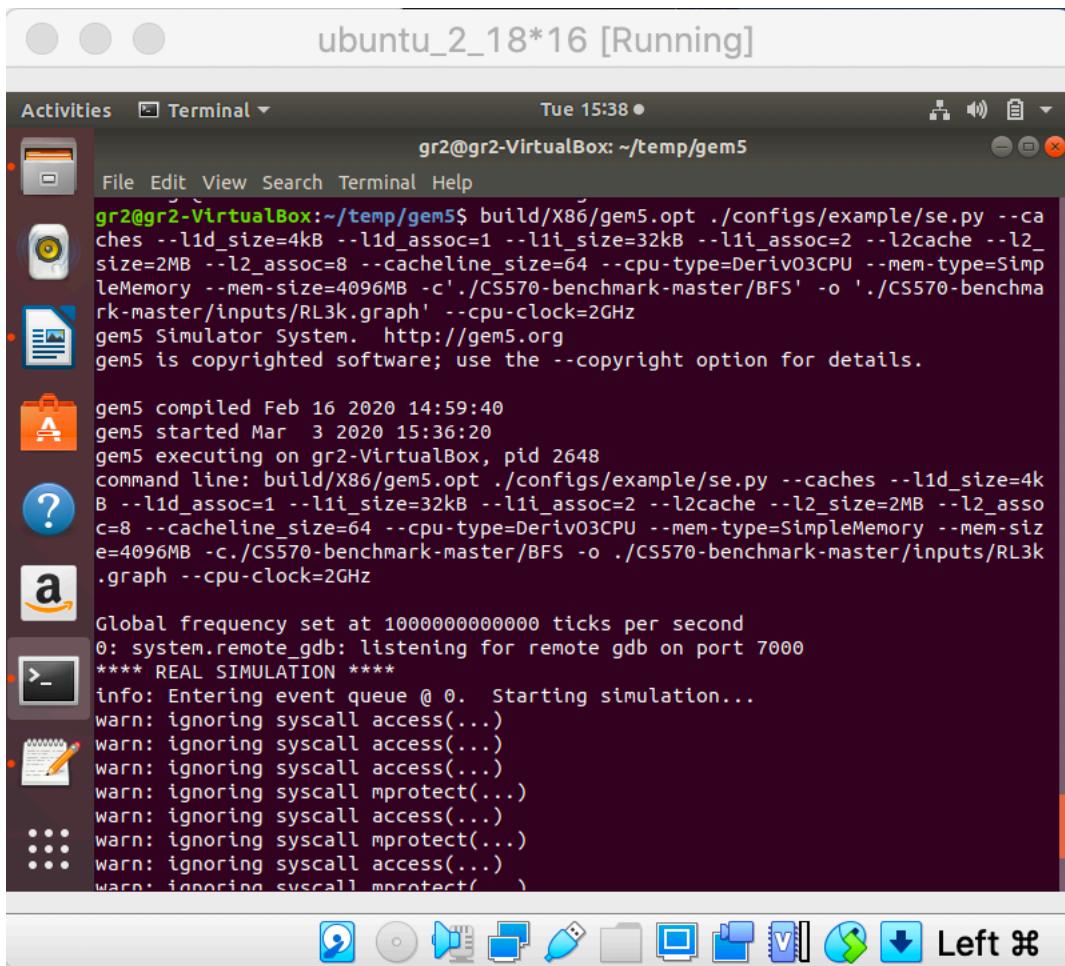
Homework 4

1. BFS

(i) Associativity: 1way, size:4kB

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=4kB --l1d_assoc=1  
--l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --  
cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-  
master/inputs/RL3k.graph --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]". The terminal is running on a system named "gr2@gr2-VirtualBox". The command entered is:

```
gr2@gr2-VirtualBox:~/temp/gem5$ build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=4kB --l1d_assoc=1 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/BFS' -o './CS570-benchmark-master/inputs/RL3k.graph' --cpu-clock=2GHz
```

Output from the terminal:

```
gem5 Simulator System. http://gem5.org  
gem5 is copyrighted software; use the --copyright option for details.  
  
gem5 compiled Feb 16 2020 14:59:40  
gem5 started Mar 3 2020 15:36:20  
gem5 executing on gr2-VirtualBox, pid 2648  
command line: build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=4kB --l1d_assoc=1 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/BFS' -o './CS570-benchmark-master/inputs/RL3k.graph' --cpu-clock=2GHz  
  
Global frequency set at 1000000000000 ticks per second  
0: system.remote_gdb: listening for remote gdb on port 7000  
**** REAL SIMULATION ****  
info: Entering event queue @ 0. Starting simulation...  
warn: ignoring syscall access(...)  
warn: ignoring syscall access(...)  
warn: ignoring syscall access(...)  
warn: ignoring syscall mprotect(...)  
warn: ignoring syscall access(...)  
warn: ignoring syscall mprotect(...)  
warn: ignoring syscall access(...)  
warn: ignoring syscall mprotect(...)
```

stats.txt: contain numerous statistics from the simulation. Interesting statistics include:

1. sim_seconds: simulation time (**0.004919**)
2. system.cpu.ipc: instructions per cycle achieved by the simulated CPU (**1.294793**)
3. system.cpu.dcache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.099607**)
4. system.l2.overall_misses::total: L2 cache miss rate (**25340**)

ubuntu_2_18*16 [Running]

Tue 15:46 ●

Activities Text Editor

Open Save

stats.txt ~ /temp/gem5/m5out

```
system.cpu.dcache.overall_accesses::total      3598126
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.099607                                     # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total     0.099607
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.099607                                     # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total    0.099607
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
20951.072801                                  # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
20951.072801                                  # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
20951.072801                                  # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
20951.072801                                  # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs    19765
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets   95
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs            737
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets          6
# number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
26.818182                                     # average number of cycles each access was
```

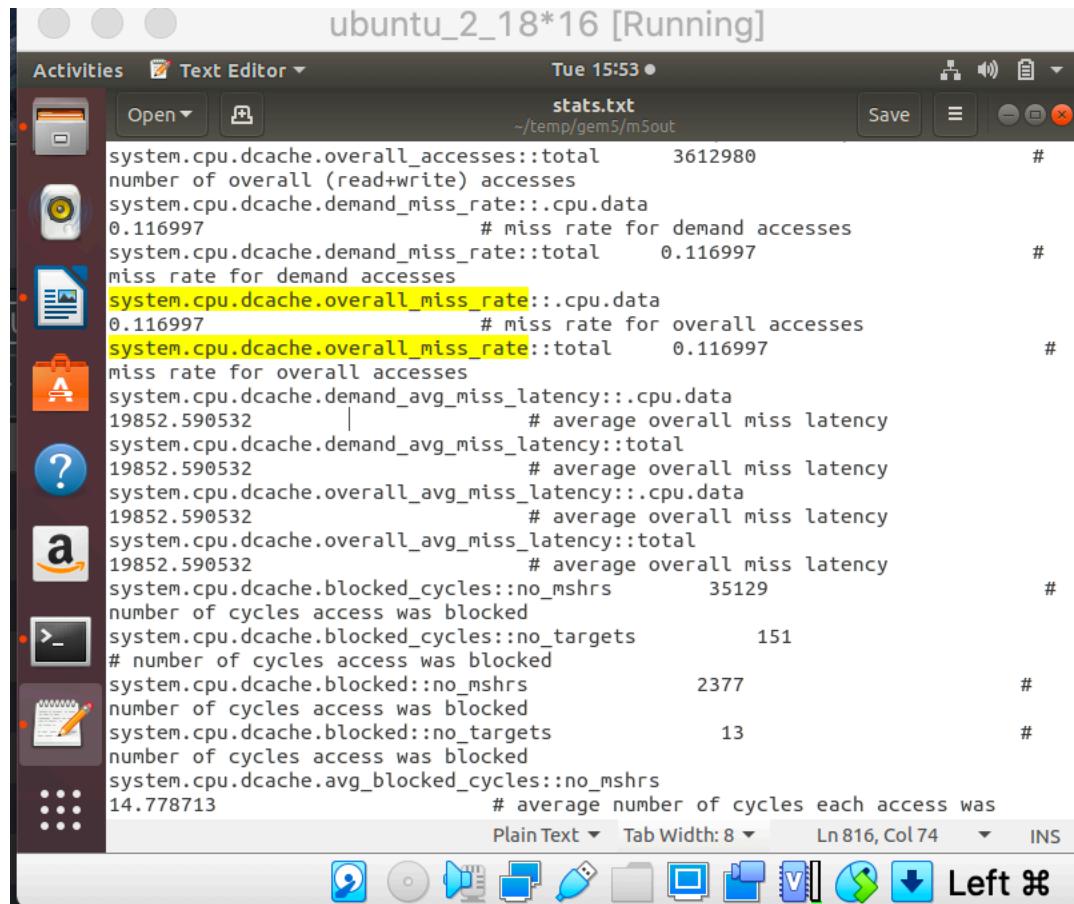
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Left ☰

(ii) **Associativity: 1way, size:16kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=16kB --l1d_assoc=1 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-master/inputs/RL3k.graph --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The terminal displays the contents of a file named "stats.txt". The file contains various performance metrics from a Gem5 simulation. Some lines in the file are highlighted in yellow, specifically: "system.cpu.dcache.overall_miss_rate::cpu.data 0.116997", "system.cpu.dcache.overall_miss_rate::total 0.116997", and "system.cpu.dcache.avg_blocked_cycles::no_mshrs 14.778713". The terminal window also shows standard Linux desktop icons in the dock at the bottom.

```
system.cpu.dcache.overall_accesses::total      3612980
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.116997                                     # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total      0.116997
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.116997                                    # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total    0.116997
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
19852.590532 |                                     # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
19852.590532                                     # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
19852.590532                                     # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
19852.590532                                     # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs      35129
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets     151
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs              2377
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets             13
number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
14.778713                                       # average number of cycles each access was
Plain Text ▾ Tab Width: 8 ▾ Ln 816, Col 74 ▾ INS
Left ☰
```

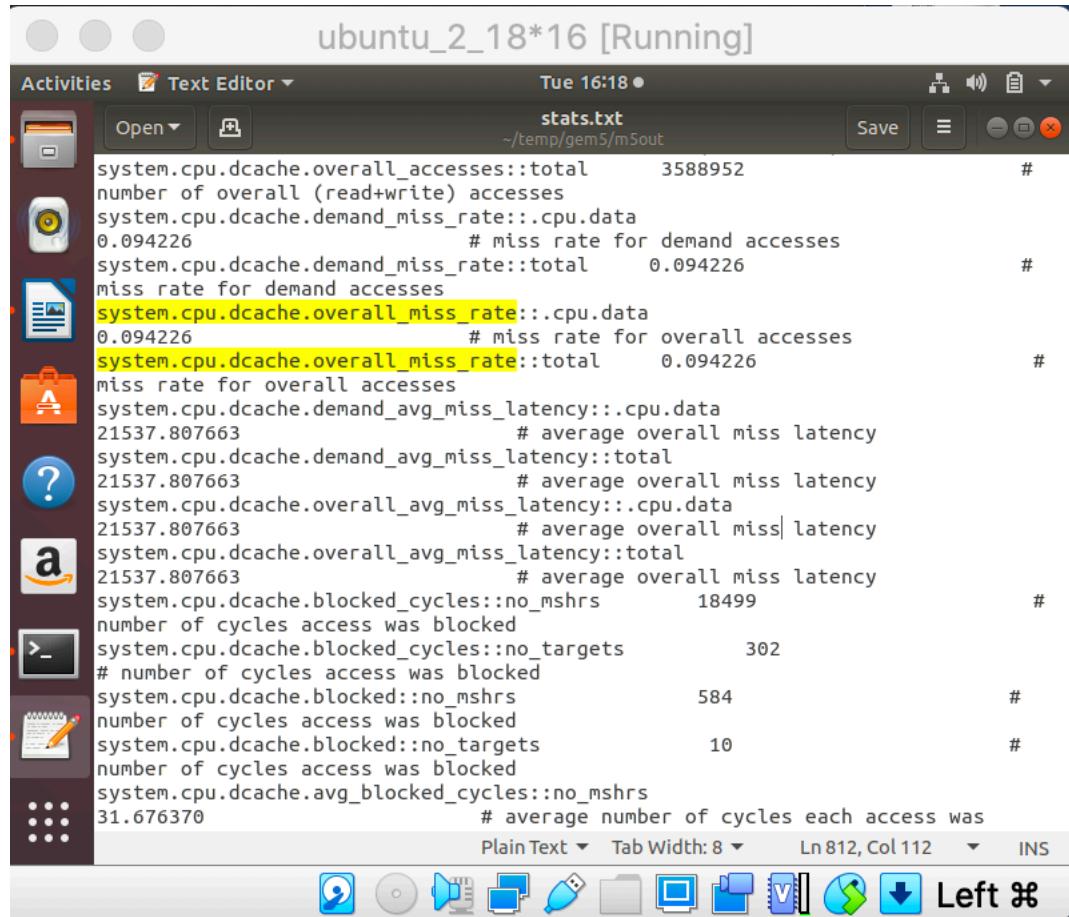
stats.txt: contain numerous statistics from the simulation. Interesting statistics include:

1. sim_seconds: simulation time (**0.005067**)
2. system.cpu.ipc: instructions per cycle achieved by the simulated CPU (**1.256953**)
3. system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.116997**)
4. system.l2.overall_misses::total: L2 cache miss rate (**25340**)

(iii) **Associativity: 1way, size:64kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=64kB --l1d_assoc=1 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-master/inputs/RL3k.graph --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The terminal displays the contents of a file named "stats.txt". The file contains various performance metrics from a Gem5 simulation. Some lines in the file are highlighted in yellow, specifically: "system.cpu.dcache.overall_miss_rate::cpu.data 0.094226", "system.cpu.dcache.overall_miss_rate::total 0.094226", and "system.cpu.dcache.blocked_cycles::no_mshrs 18499". The terminal window has a standard Linux interface with icons for file operations and a status bar at the bottom.

```
ubuntu_2_18*16 [Running]
Activities Text Editor Tue 16:18 •
Open Save
stat.txt ~/temp/gem5/m5out
system.cpu.dcache.overall_accesses::total 3588952
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.094226 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.094226
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.094226 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.094226
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
21537.807663 # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
21537.807663 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
21537.807663 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
21537.807663 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 18499
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 302
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 584
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 10
number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
31.676370 # average number of cycles each access was
Plain Text Tab Width: 8 Ln 812, Col 112 INS
Left
```

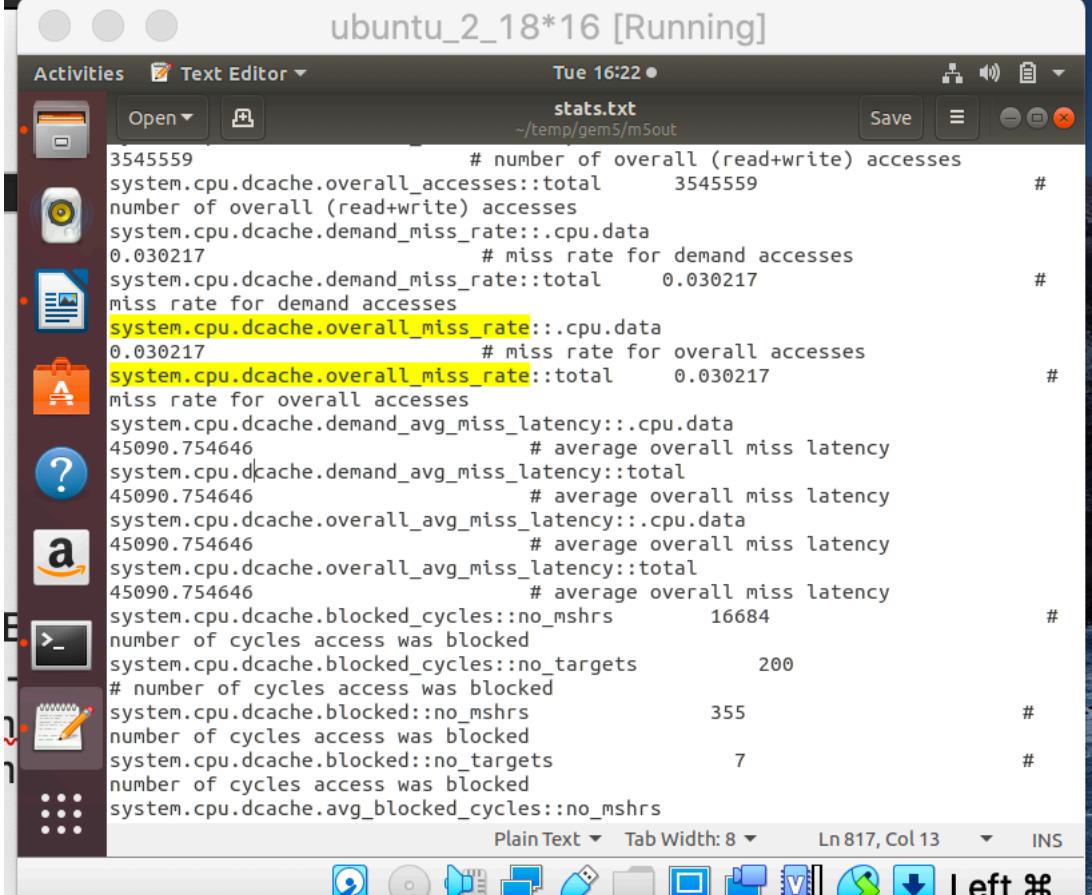
stats.txt: contain numerous statistics from the simulation. Interesting statistics include:

1. sim_seconds: simulation time (**0.004866**)
2. system.cpu.ipc: instructions per cycle achieved by the simulated CPU (**1.308950**)
3. system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.094226**)
4. system.l2.overall_misses::total: L2 cache miss rate (**25323**)

(iv) **Associativity: 1way, size:512kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=64kB --l1d_assoc=1 --  
l1i_size=512kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --  
cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-  
master/inputs/RL3k.graph --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The window displays a file named "stats.txt" containing performance metrics from a Gem5 simulation. The metrics include overall accesses, miss rates, and average miss latencies for L1 and L2 caches. The L1 data cache miss rate is highlighted in yellow.

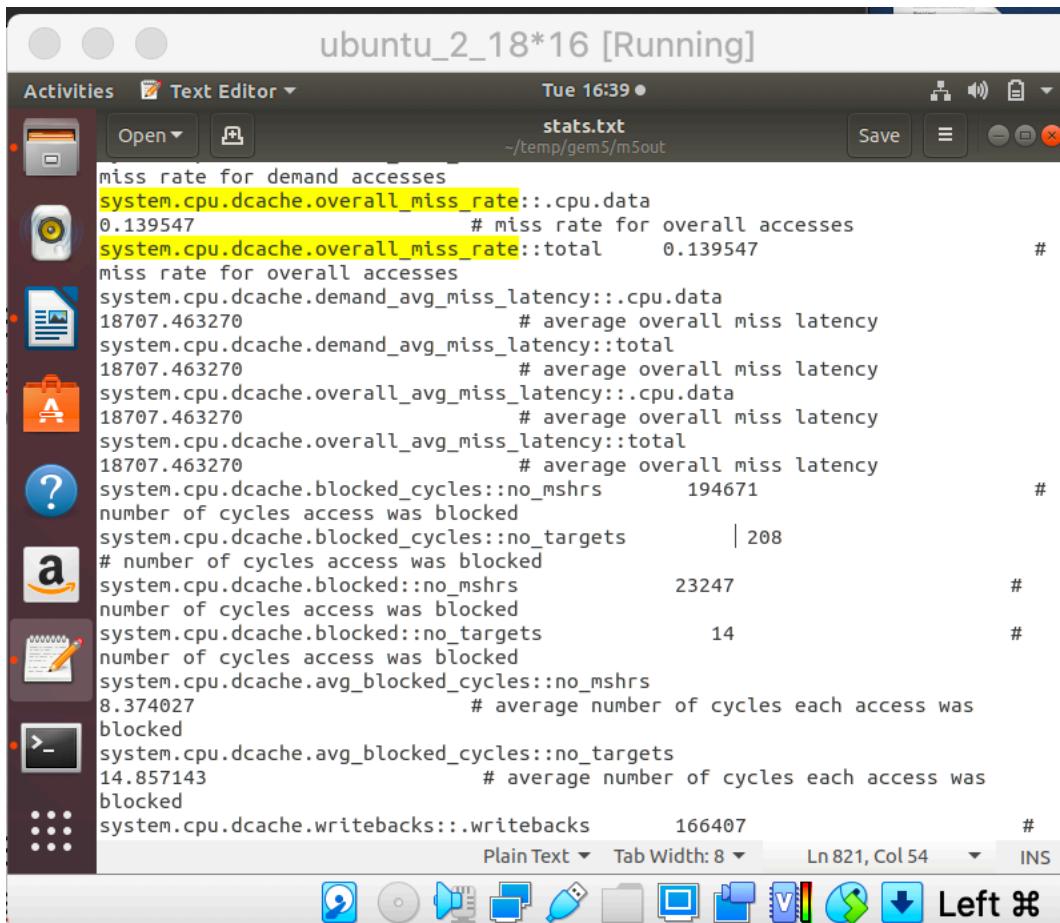
```
3545559 # number of overall (read+write) accesses  
system.cpu.dcache.overall_accesses::total 3545559 #  
number of overall (read+write) accesses  
system.cpu.dcache.demand_miss_rate::cpu.data  
0.030217 # miss rate for demand accesses  
system.cpu.dcache.demand_miss_rate::total 0.030217 #  
miss rate for demand accesses  
system.cpu.dcache.overall_miss_rate::cpu.data  
0.030217 # miss rate for overall accesses  
system.cpu.dcache.overall_miss_rate::total 0.030217 #  
miss rate for overall accesses  
system.cpu.dcache.demand_avg_miss_latency::cpu.data  
45090.754646 # average overall miss latency  
system.cpu.dcache.demand_avg_miss_latency::total  
45090.754646 # average overall miss latency  
system.cpu.dcache.overall_avg_miss_latency::cpu.data  
45090.754646 # average overall miss latency  
system.cpu.dcache.overall_avg_miss_latency::total  
45090.754646 # average overall miss latency  
system.cpu.dcache.blocked_cycles::no_mshrs 16684 #  
number of cycles access was blocked  
system.cpu.dcache.blocked_cycles::no_targets 200 #  
number of cycles access was blocked  
system.cpu.dcache.blocked::no_mshrs 355 #  
number of cycles access was blocked  
system.cpu.dcache.blocked::no_targets 7 #  
number of cycles access was blocked  
system.cpu.dcache.avg_blocked_cycles::no_mshrs
```

system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (0.030217)

(V) **Associativity: 2way, size: 4 kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=32kB --l1d_assoc=2 --l1i_size=4kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-master/inputs/RL3k.graph --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The window displays a text file named "stats.txt" located at "/tmp/gem5/m5out". The terminal output shows various cache performance metrics. A specific line in the output is highlighted in yellow: "system.cpu.dcache.overall_miss_rate::cpu.data 0.139547". This line represents the L1 data cache miss rate, which is explicitly labeled in the text below.

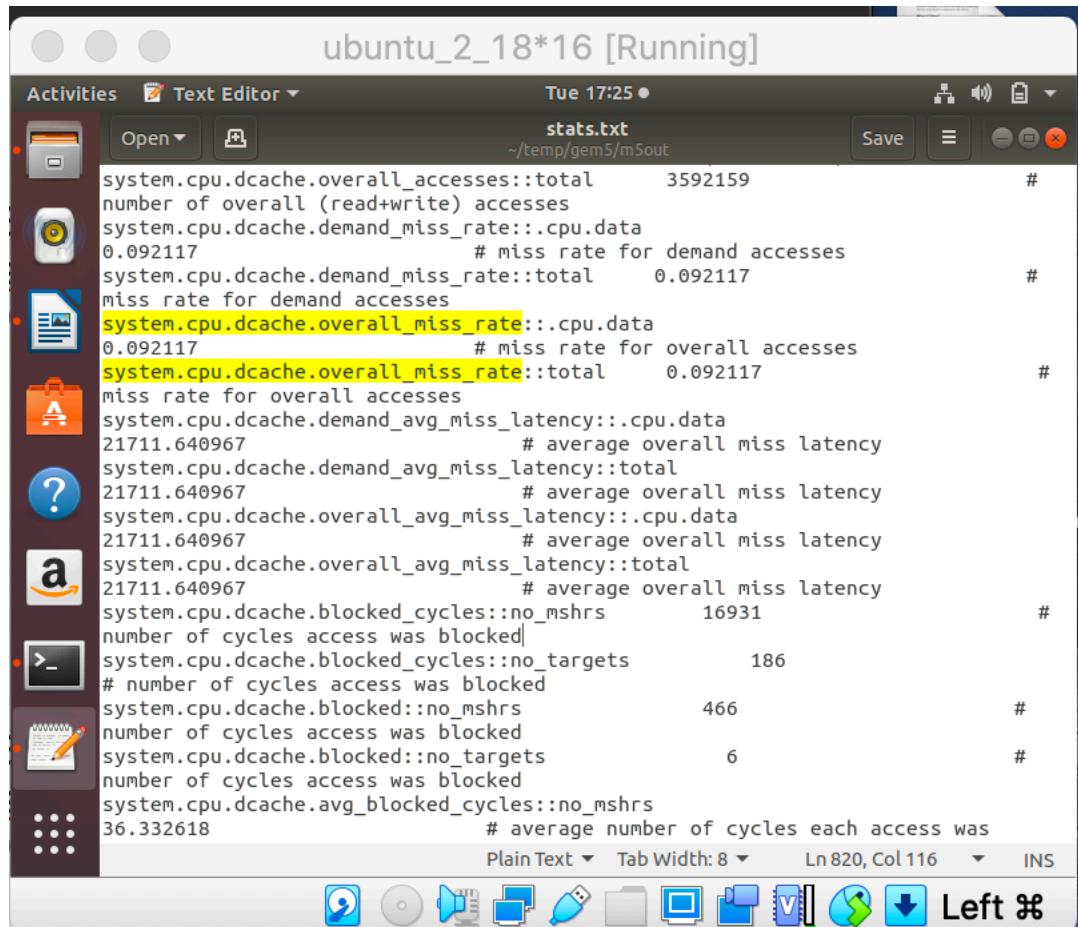
```
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.139547          # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total      0.139547      #
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
18707.463270        # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
18707.463270        # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
18707.463270        # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
18707.463270        # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs      194671      #
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets      | 208
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs                23247      #
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets                14      #
number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
8.374027          # average number of cycles each access was
blocked
system.cpu.dcache.avg_blocked_cycles::no_targets
14.857143          # average number of cycles each access was
blocked
system.cpu.dcache.writebacks::writebacks         166407      #
Plain Text ▾ Tab Width: 8 ▾ Ln 821, Col 54 ▾ INS
```

system.cpu.dache的整体命中率::cpu.data: L1数据缓存命中率 (**0.139547**)

(VI) Associativity: 2way, size: 64 kB

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=32kB --l1d_assoc=2 --l1i_size=4kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-master/inputs/RL3k.graph --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The window displays the contents of a file named "stats.txt" located at "/tmp/gem5/m5out". The terminal output includes various cache statistics, with several lines related to L1 data cache miss rates highlighted in yellow:

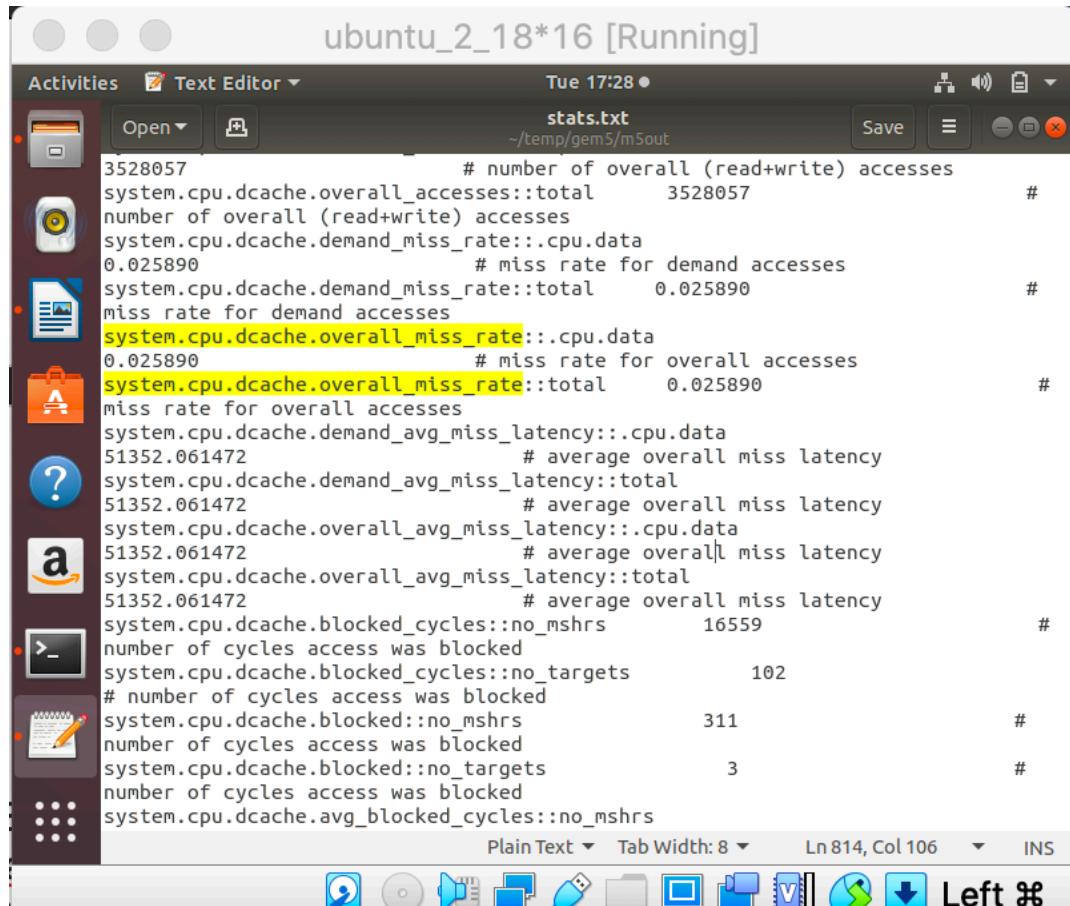
```
system.cpu.dcache.overall_accesses::total      3592159
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.092117                                     # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total      0.092117
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.092117                                     # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total      0.092117
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
21711.640967                                  # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
21711.640967                                  # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
21711.640967                                  # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
21711.640967                                  # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs     16931
number of cycles access was blocked|
system.cpu.dcache.blocked_cycles::no_targets    186
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs             466
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets           6
number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
36.332618                                     # average number of cycles each access was
```

system.cpu.dache的整体miss率 (0.092117)

(VII) Associativity: 2way, size: 512 kB

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=32kB --l1d_assoc=2 --l1i_size=4kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-master/inputs/RL3k.graph --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The window displays a text file named "stats.txt" containing performance metrics from a Gem5 simulation. The metrics include overall accesses, miss rates, and average miss latencies for the L1 data cache. The "system.cpu.dcache.overall_miss_rate::cpu.data" metric is highlighted in yellow.

```
3528057 # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total 3528057 #
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.025890 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.025890 #
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.025890 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.025890 #
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
51352.061472 # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
51352.061472 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
51352.061472 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
51352.061472 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 16559 #
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 102
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 311 #
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 3 #
number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
```

system.cpu.dache的整体命中率 (0.025890)

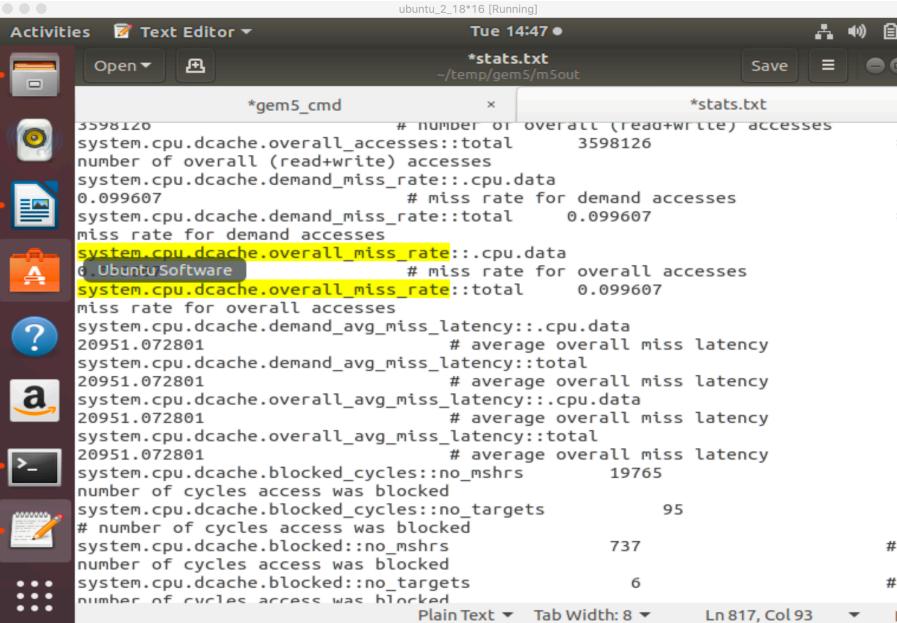
(VIII) Associativity: 2way, size:32kB

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=32kB --l1d_assoc=2 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-master/inputs/RL3k.graph --cpu-clock=2GHz
```

stats.txt: contain numerous statistics from the simulation. Interesting statistics include:

1. sim_seconds: simulation time (**0.004919**)
2. system.cpu.ipc: instructions per cycle achieved by the simulated CPU (**1.294793**)
3. system.cpu.dcache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.099607**)
4. system.l2.overall_misses::total: L2 cache miss rate (**25340**)

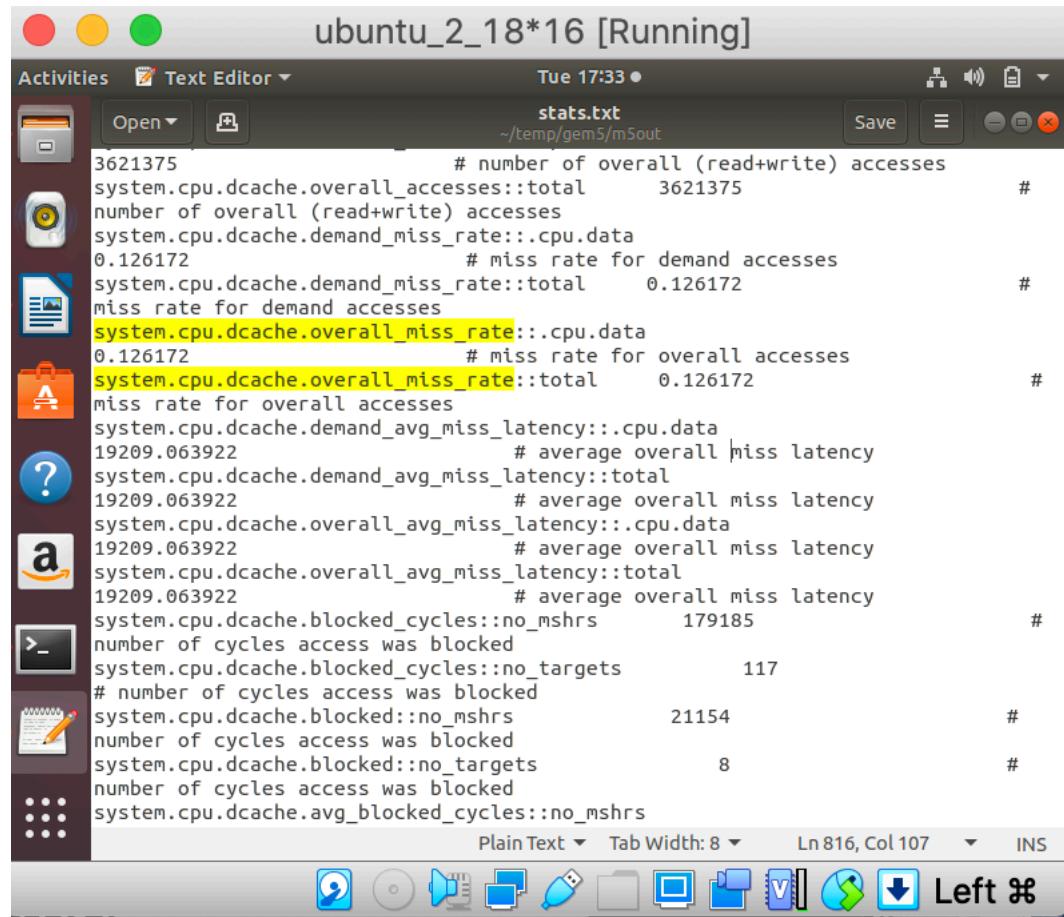


```
ubuntu_2_18*16 [Running]
Activities Text Editor Tue 14:47
*gem5_cmd *stats.txt
*gem5_cmd x *stats.txt
~/.temp/gem5/m5out
Save
*gem5_cmd
3598126 # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total 3598126
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.099607 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.099607
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.099607 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.099607
miss rate for overall accesses
system.cpu.dcache.demand_avg_latency::cpu.data
20951.072801 # average overall miss latency
system.cpu.dcache.demand_avg_latency::total
20951.072801 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
20951.072801 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
20951.072801 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 19765
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 95
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 737 #
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 6 #
number of cycles access was blocked
```

(IX) Associativity: 8way, size: 4 kB

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=4kB --l1d_assoc=8 --l1i_size=32kB --l1i_assoc=8 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-master/inputs/RL3k.graph --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The terminal displays a file named "stats.txt" located at "/tmp/gem5/m5out". The content of the file is as follows:

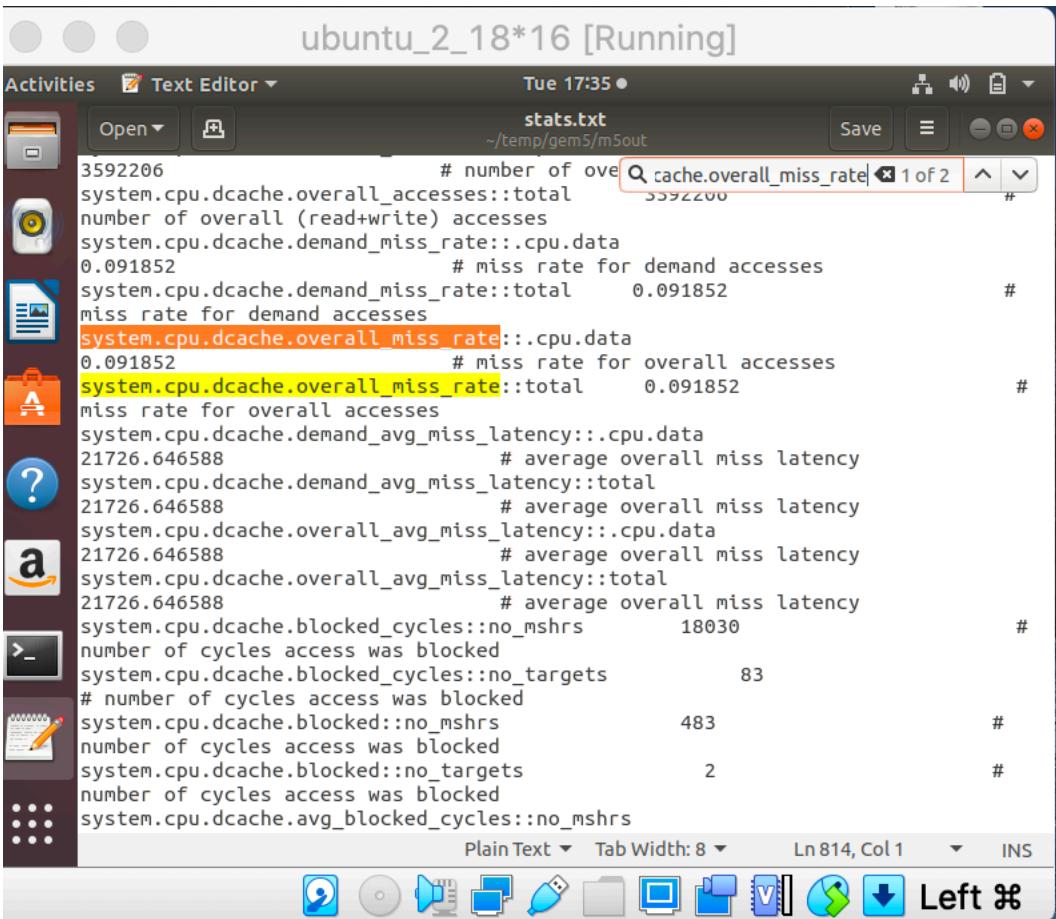
```
3621375 # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total 3621375 #
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.126172 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.126172 #
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.126172 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.126172 #
miss rate for overall accesses
system.cpu.dcache.demand_avg_latency::cpu.data
19209.063922 # average overall miss latency
system.cpu.dcache.demand_avg_latency::total
19209.063922 # average overall miss latency
system.cpu.dcache.overall_avg_latency::cpu.data
19209.063922 # average overall miss latency
system.cpu.dcache.overall_avg_latency::total
19209.063922 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 179185 #
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 117
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 21154 #
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 8 #
number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
```

system.cpu.dache的整体命中率 (0.126172)

(X) **Associativity: 8way, size: 64 kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=64kB --l1d_assoc=8 --l1i_size=32kB --l1i_assoc=8 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-benchmark-master/BFS -o ./CS570-benchmark-master/inputs/RL3k.graph --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The terminal displays simulation statistics from Gem5. A search bar at the top of the terminal window has the text "cache.overall_miss_rate" entered. The terminal output includes the following relevant lines:

```
3592206      # number of overall accesses
system.cpu.dcache.overall_miss_rate::total    0.091852
system.cpu.dcache.demand_miss_rate::cpu.data
0.091852      # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total    0.091852
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.091852      # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total    0.091852
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
21726.646588  # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
21726.646588  # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
21726.646588  # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
21726.646588  # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs     18030
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets    83
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs              483
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets             2
# number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
```

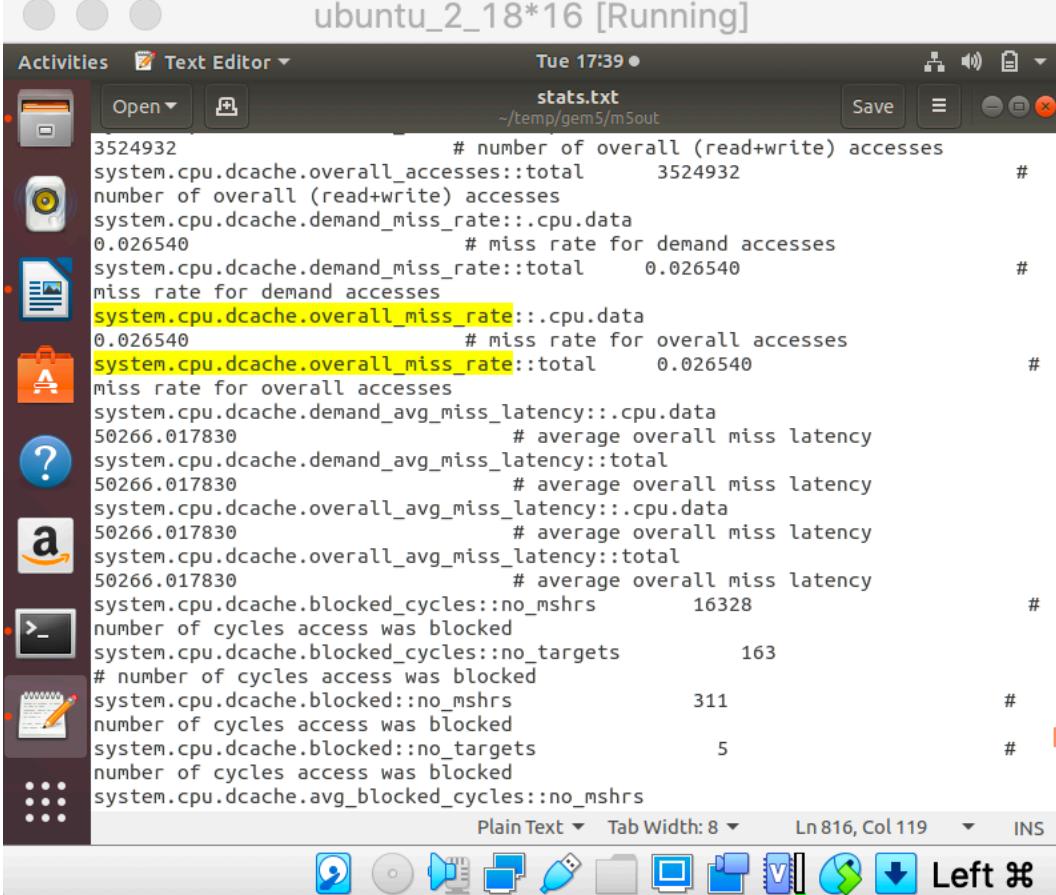
The terminal also shows status information like "Tue 17:35" and file navigation buttons at the bottom.

system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.091852**)

(XI) **Associativity: 8way, size: 512 kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=512kB --l1d_assoc=8 -  
-l1i_size=32kB --l1i_assoc= --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64  
--cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c./CS570-  
benchmark-master/BFS -o ./CS570-benchmark-master/inputs/RL3k.graph --cpu-  
clock=2GHz
```



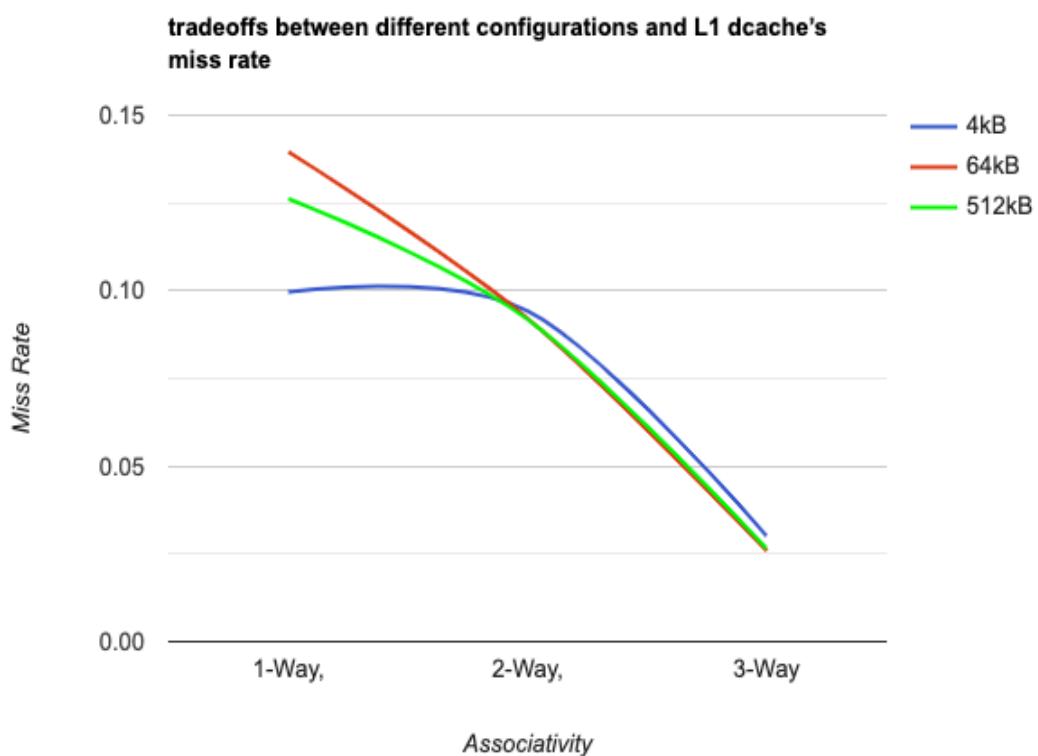
The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The terminal displays simulation statistics from Gem5. The output includes various cache metrics such as overall accesses, miss rates, and average miss latencies. A specific line in the output is highlighted in yellow: "system.cpu.dcache.overall_miss_rate::cpu.data 0.026540". This line represents the L1 data cache miss rate. The terminal window also shows other metrics like overall_avg_latency and blocked_cycles.

```
3524932          # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total      3524932
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.026540          # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total      0.026540
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.026540          # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total      0.026540
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
50266.017830      # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
50266.017830      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
50266.017830      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
50266.017830      # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs      16328
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets     163
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs               311
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets              5
# number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
```

system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.026540**)

	4kB	64kB	512kB
1-way	0.099607	0.094226	0.03021
2-way	0.139547	0.092117	0.025890
3-way	0.126172	0.091852	0.026540

tradeoffs between different configurations and L1 dcache's miss rate



Cache size and miss rates

Cache size also has a significant impact on performance In a larger cache there's less chance there will be of a conflict Again this means the miss rate decreases, so the AMAT and number of memory stall cycles also decrease The complete Figure depicts the miss rate as a function of both the cache size and its associativity

Block size and miss rates

Finally, the figure shows miss rates relative to block size and overall cache size Smaller blocks do not take maximum advantage of spatial locality But if blocks are too large, there are fewer blocks available, and more potential conflicts misses

2. QUEENS

(i) Associativity: 1way, size:4kB

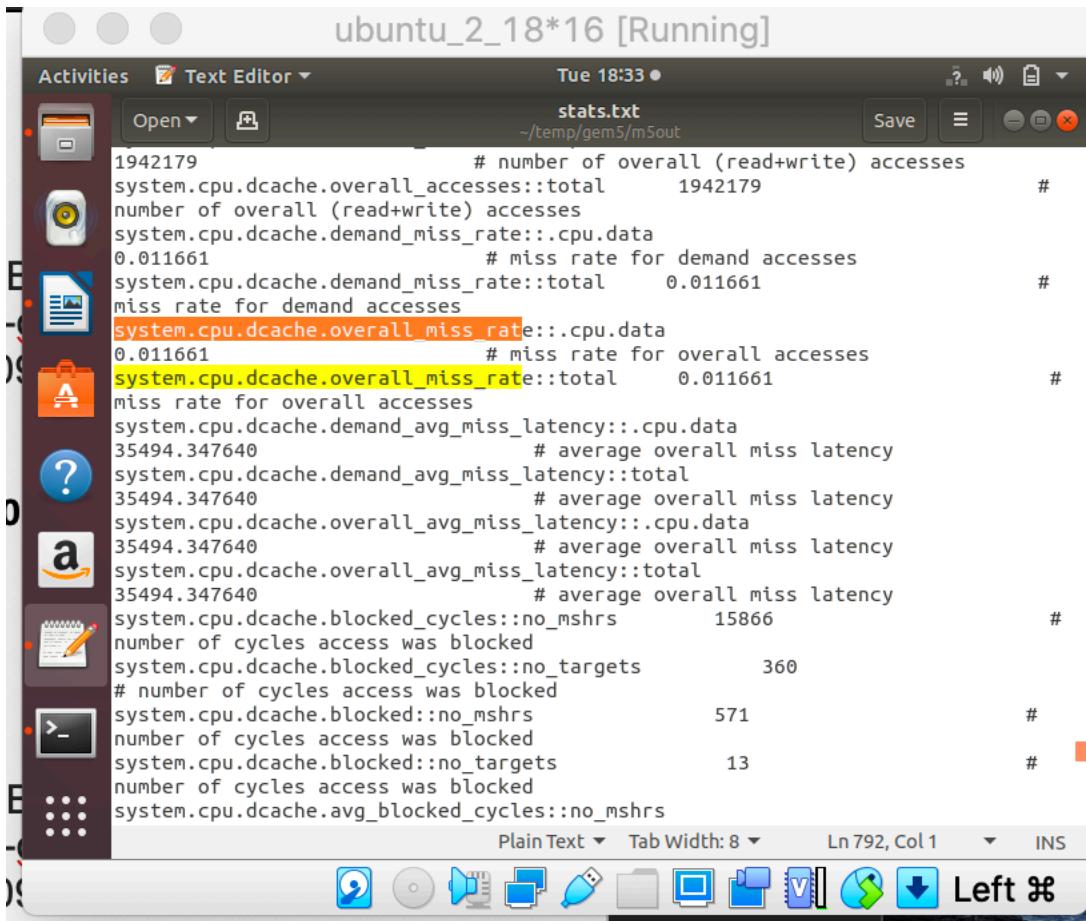
Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=4kB --l1d_assoc=1 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o '-c 10' --cpu-clock=2GHz
```

The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop environment. The terminal window has a dark background and displays the output of the Gem5 simulator. The output shows the command being run, the simulation parameters, and the results of the N-Queens search.

```
File Edit View Search Terminal Help  
-clock=2GHz  
gem5 Simulator System. http://gem5.org  
gem5 is copyrighted software; use the --copyright option for details.  
gem5 compiled Feb 16 2020 14:59:40  
gem5 started Mar 3 2020 18:31:19  
gem5 executing on gr2-VirtualBox, pid 3205  
command line: build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=4kB --l1d_assoc=1 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o '-c 10' --cpu-clock=2GHz  
  
Global frequency set at 1000000000000 ticks per second  
0: system.remote_gdb: listening for remote gdb on port 7000  
**** REAL SIMULATION ****  
info: Entering event queue @ 0. Starting simulation...  
warn: ignoring syscall access(...)  
warn: ignoring syscall access(...)  
warn: ignoring syscall access(...)  
warn: ignoring syscall mprotect(...)  
warn: ignoring syscall mprotect(...)  
warn: ignoring syscall mprotect(...)  
warn: ignoring syscall mprotect(...)  
info: Increasing stack size by one page.  
10 queens on a 10x10 board...  
...there are 724 solutions  
Exiting @ tick 3008190000 because exiting with last active thread context  
gr2@gr2-VirtualBox:~/temp/gem5$
```

system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.011661**)



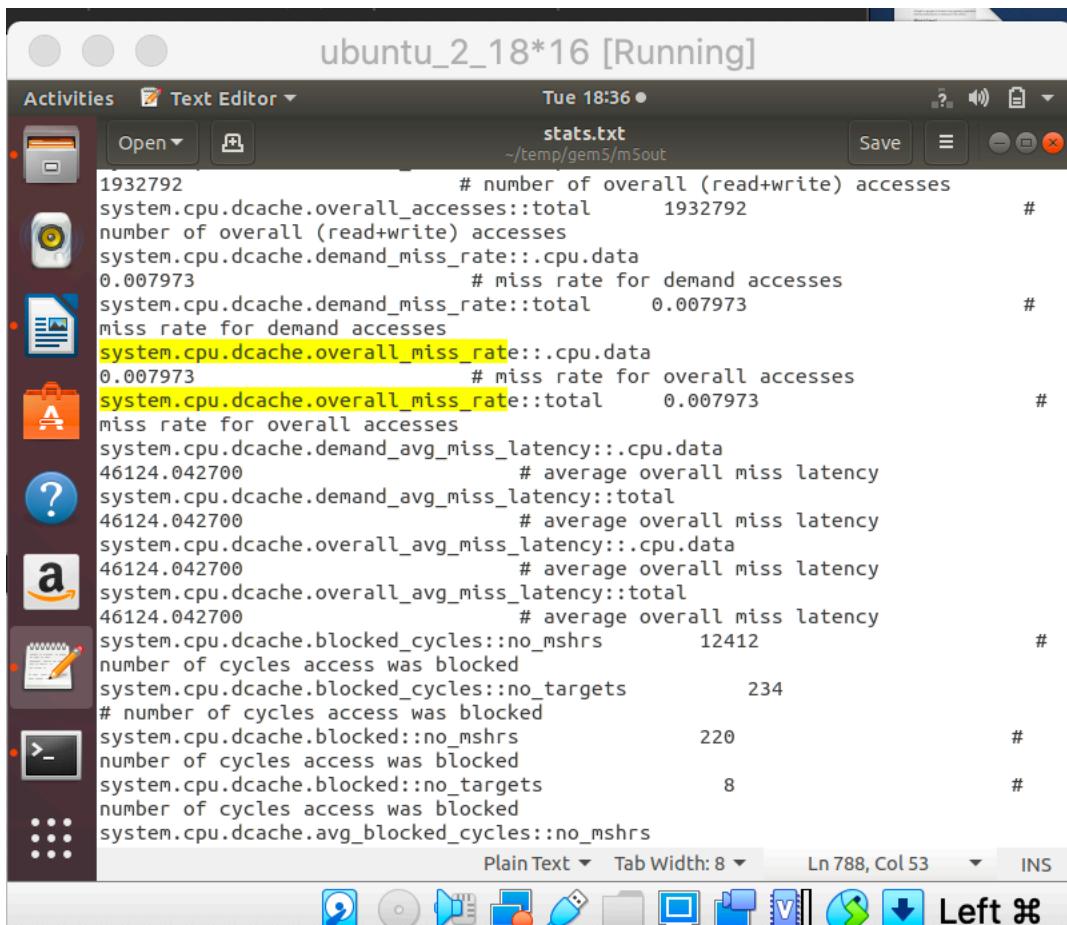
The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The terminal displays a file named "stats.txt" located at "/tmp/gem5/m5out". The content of the file is as follows:

```
1942179          # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total      1942179          #
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.011661          # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total      0.011661          #
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.011661          # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total      0.011661          #
miss rate for overall accesses
system.cpu.dcache.demand_avg_latency::cpu.data
35494.347640      # average overall miss latency
system.cpu.dcache.demand_avg_latency::total
35494.347640      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
35494.347640      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
35494.347640      # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs      15866          #
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets      360
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs                571          #
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets                13          #
number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
```

(ii) **Associativity: 1way, size:64kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=64kB --l1d_assoc=1 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o 'c 10' --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The window displays simulation statistics from the Gem5 tool. The statistics include various cache metrics such as overall accesses, miss rates, and latency. The "system.cpu.dcache.overall_miss_rate::cpu.data" metric is highlighted in yellow, showing a value of 0.007973. Other metrics like "system.cpu.dcache.demand_avg_latency" and "system.cpu.dcache.blocked_cycles" are also listed.

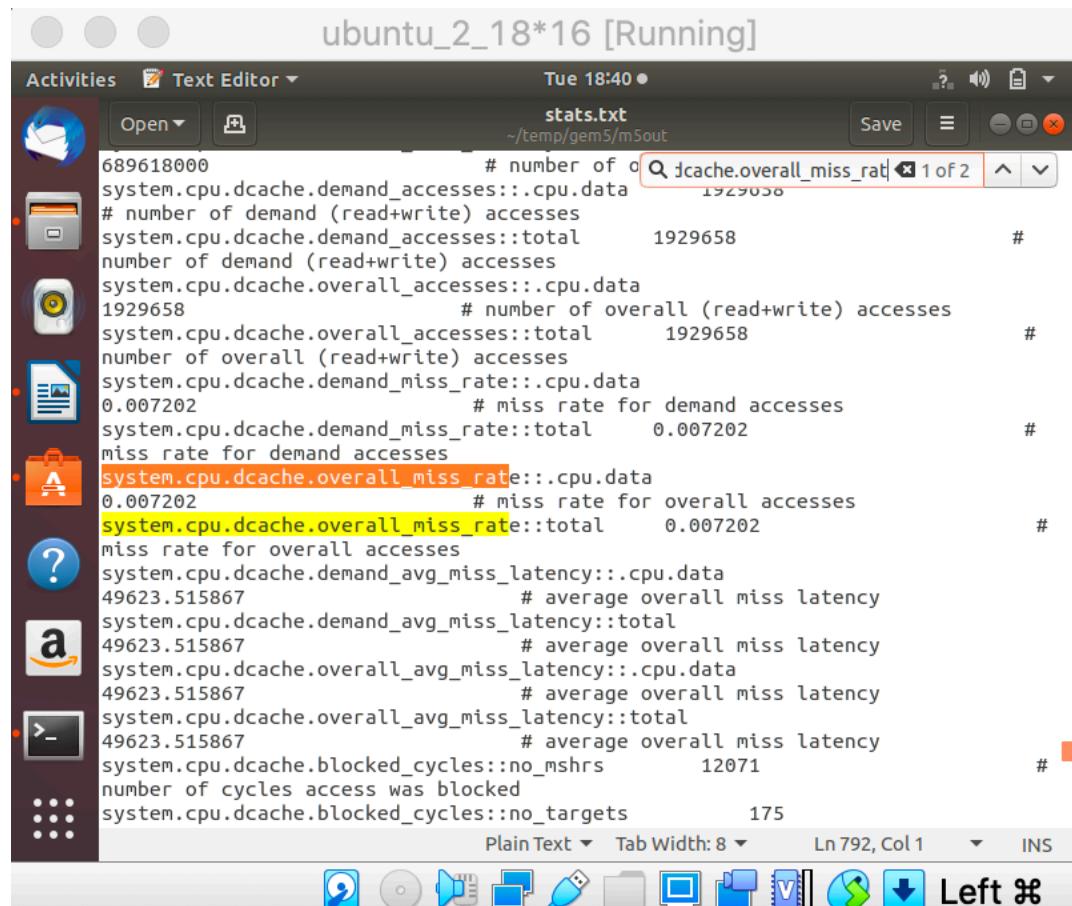
```
1932792          # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total      1932792          #
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.007973          # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total      0.007973          #
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.007973          # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total      0.007973          #
miss rate for overall accesses
system.cpu.dcache.demand_avg_latency::cpu.data
46124.042700      # average overall miss latency
system.cpu.dcache.demand_avg_latency::total
46124.042700      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
46124.042700      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
46124.042700      # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs      12412           #
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets     234             #
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs              220             #
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets            8               #
number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
```

system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (0.007973)

(iii) **Associativity: 1way, size:512kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=512kB --l1d_assoc=1 -  
-l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --  
cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-  
size=4096MB -c'./CS570-benchmark-master/queens' -o ' -c 10' --cpu-clock=2GHz
```



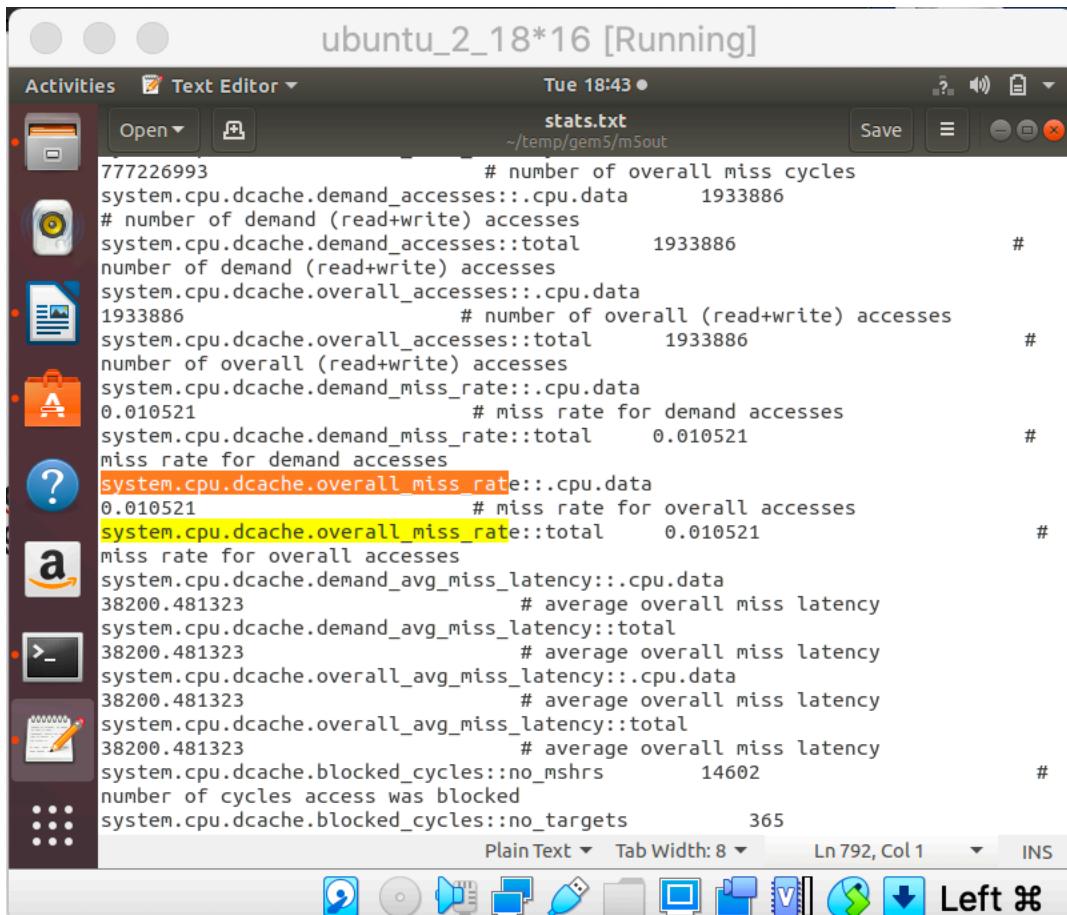
```
ubuntu_2_18*16 [Running]
Activities Text Editor Tue 18:40 •
stat.txt ~ /temp/gem5/m5out Save
689618000 # number of cache.demand_accesses::cpu.data
system.cpu.dcache.demand_accesses::cpu.data 1929658
# number of demand (read+write) accesses
system.cpu.dcache.demand_accesses::total 1929658
# number of demand (read+write) accesses
system.cpu.dcache.overall_accesses::cpu.data
1929658 # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total 1929658
# number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.007202 # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total 0.007202
# miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.007202 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.007202
# miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
49623.515867 # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
49623.515867 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
49623.515867 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
49623.515867 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 12071
# number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 175
Plain Text Tab Width: 8 Ln 792, Col 1 INS
Left
```

system.cpu.dache的整体miss率: L1数据缓存miss率 (0.007202)

(iv) **Associativity: 2way, size:4kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=4kB --l1d_assoc=2 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o 'c 10' --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The window contains the output of a Gem5 simulation, specifically the contents of "stats.txt". The text output includes various performance metrics such as miss cycles, access counts, and miss rates for the L1 cache. A yellow highlight is placed over the line "system.cpu.dcache.overall_miss_rate::cpu.data" and its value "0.010521".

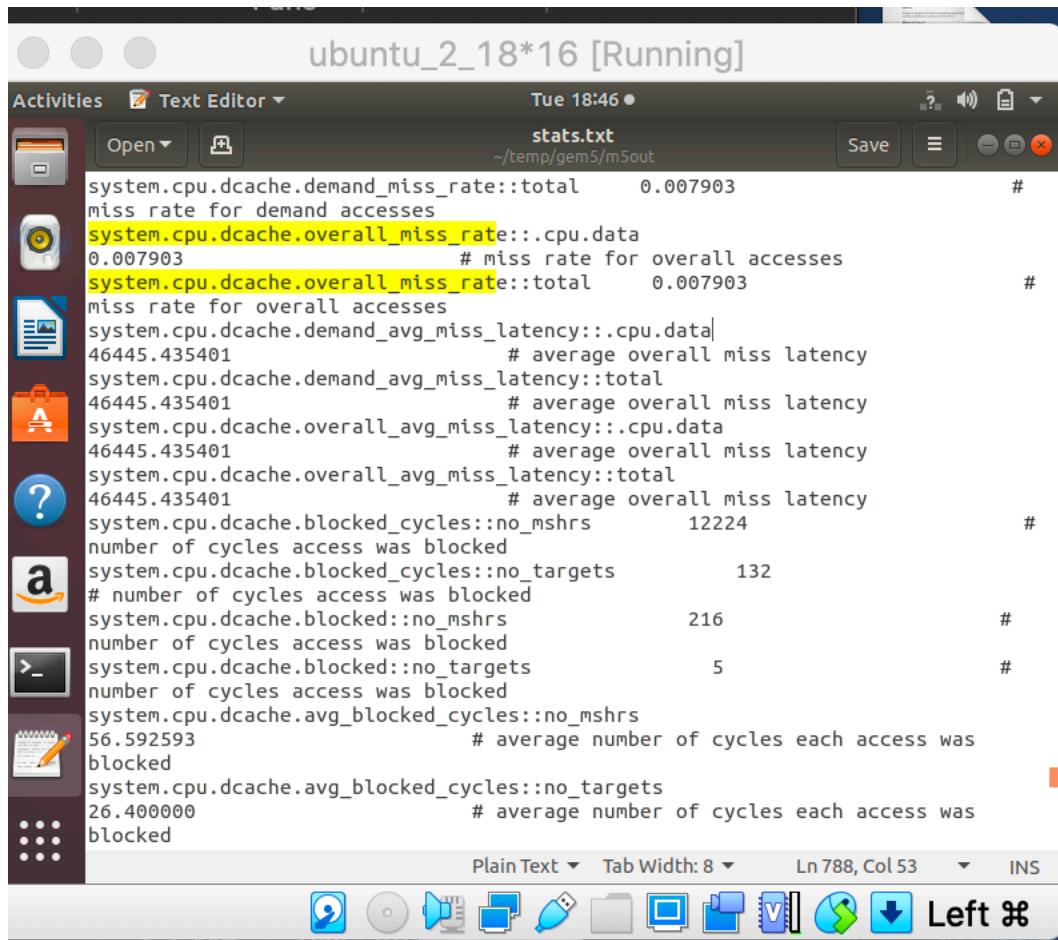
```
777226993          # number of overall miss cycles
system.cpu.dcache.demand_accesses::cpu.data      1933886
# number of demand (read+write) accesses
system.cpu.dcache.demand_accesses::total      1933886          #
number of demand (read+write) accesses
system.cpu.dcache.overall_accesses::cpu.data
1933886          # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total      1933886          #
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.010521          # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total      0.010521          #
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.010521          # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total      0.010521          #
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
38200.481323      # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
38200.481323      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
38200.481323      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
38200.481323      # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs      14602          #
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets      365
```

system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.010521**)

(v) **Associativity: 2way, size:64kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=64kB --l1d_assoc=2 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o 'c 10' --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The window contains the following text output from the Gem5 simulation:

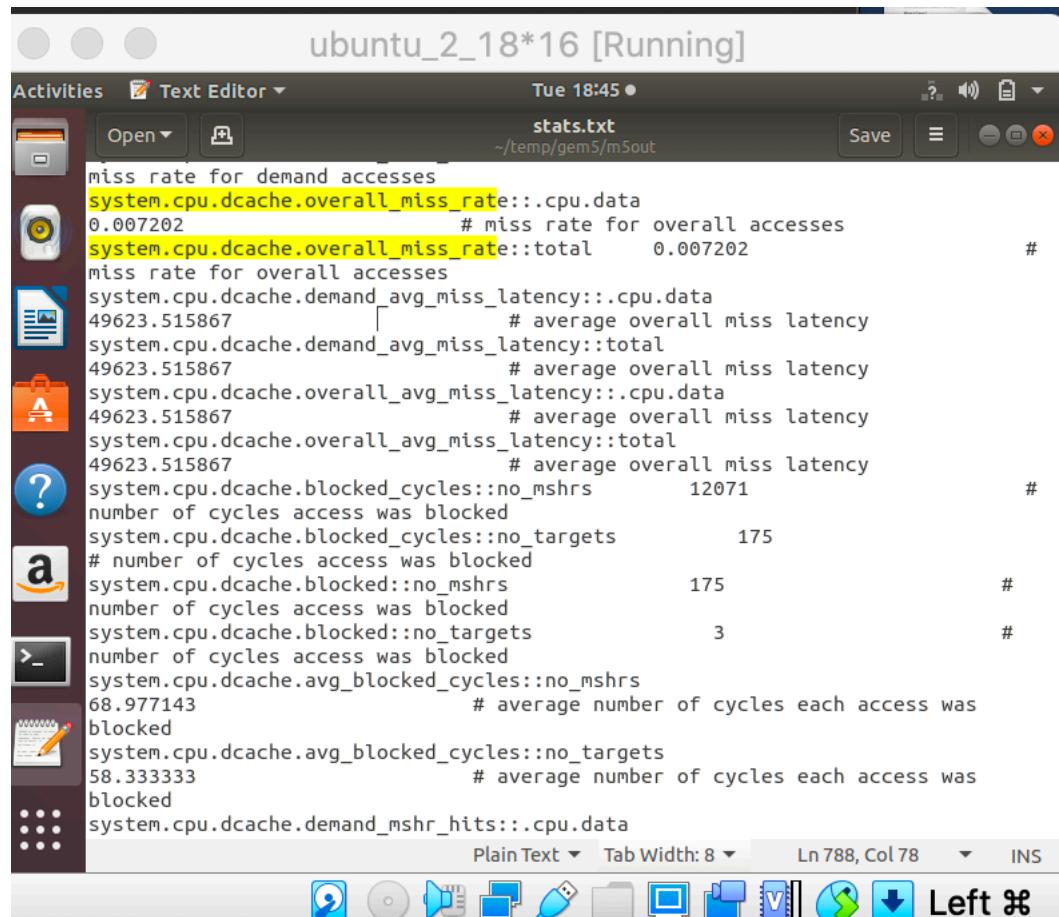
```
system.cpu.dcache.demand_miss_rate::total      0.007903
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.007903                                     # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total      0.007903
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
46445.435401                                  # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
46445.435401                                  # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
46445.435401                                  # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
46445.435401                                  # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs     12224
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets    132
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs             216
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets            5
# number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
56.592593                                     # average number of cycles each access was
blocked
system.cpu.dcache.avg_blocked_cycles::no_targets
26.400000                                     # average number of cycles each access was
blocked
```

system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.007903**)

(vi) **Associativity: 2way,size:512kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=64kB --l1d_assoc=2 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o 'c 10' --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The window contains the following text:

```
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.007202 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.007202 #
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
49623.515867 # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
49623.515867 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
49623.515867 # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
49623.515867 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 12071 #
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 175
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 175 #
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 3 #
number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
68.977143 # average number of cycles each access was
blocked
system.cpu.dcache.avg_blocked_cycles::no_targets
58.333333 # average number of cycles each access was
blocked
system.cpu.dcache.demand_mshr_hits::cpu.data
```

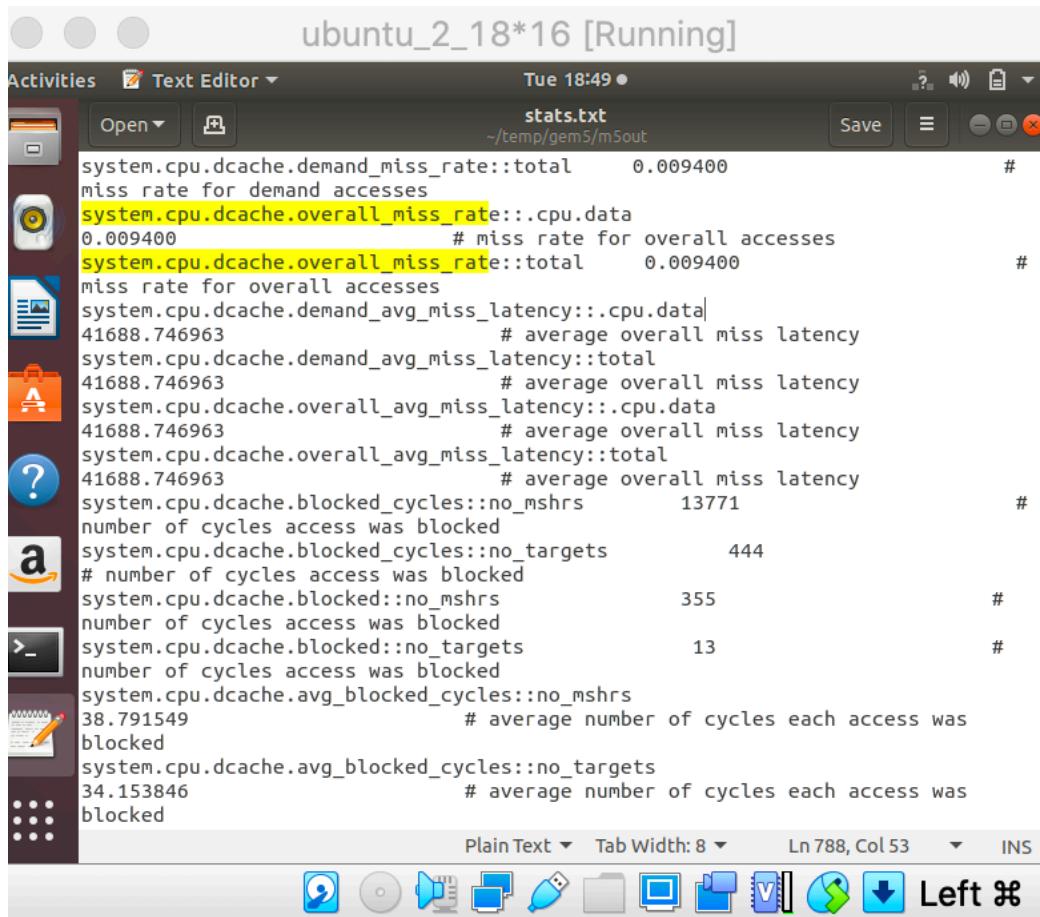
The terminal window has a dark theme and includes standard Linux desktop icons in its sidebar.

system.cpu.dache的整体命中率(cpu.data): L1数据缓存命中率 (**0.007202**)

(vii) **Associativity: 8way, size:4kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=4kB --l1d_assoc=8 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o '-c 10' --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The window contains the output of a Gem5 simulation. The text in the terminal is as follows:

```
Activities Text Editor Tue 18:49 ●
Open stats.txt ~/temp/gem5/m5out Save
# system.cpu.dcache.demand_miss_rate::total 0.009400
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.009400 # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total 0.009400
miss rate for overall accesses
system.cpu.dcache.demand_avg_latency::cpu.data
41688.746963 # average overall miss latency
system.cpu.dcache.demand_avg_latency::total
41688.746963 # average overall miss latency
system.cpu.dcache.overall_avg_latency::cpu.data
41688.746963 # average overall miss latency
system.cpu.dcache.overall_avg_latency::total
41688.746963 # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs 13771
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets 444
# number of cycles access was blocked
system.cpu.dcache.blocked::no_mshrs 355
number of cycles access was blocked
system.cpu.dcache.blocked::no_targets 13
# number of cycles access was blocked
system.cpu.dcache.avg_blocked_cycles::no_mshrs
38.791549 # average number of cycles each access was
blocked
system.cpu.dcache.avg_blocked_cycles::no_targets
34.153846 # average number of cycles each access was
blocked
```

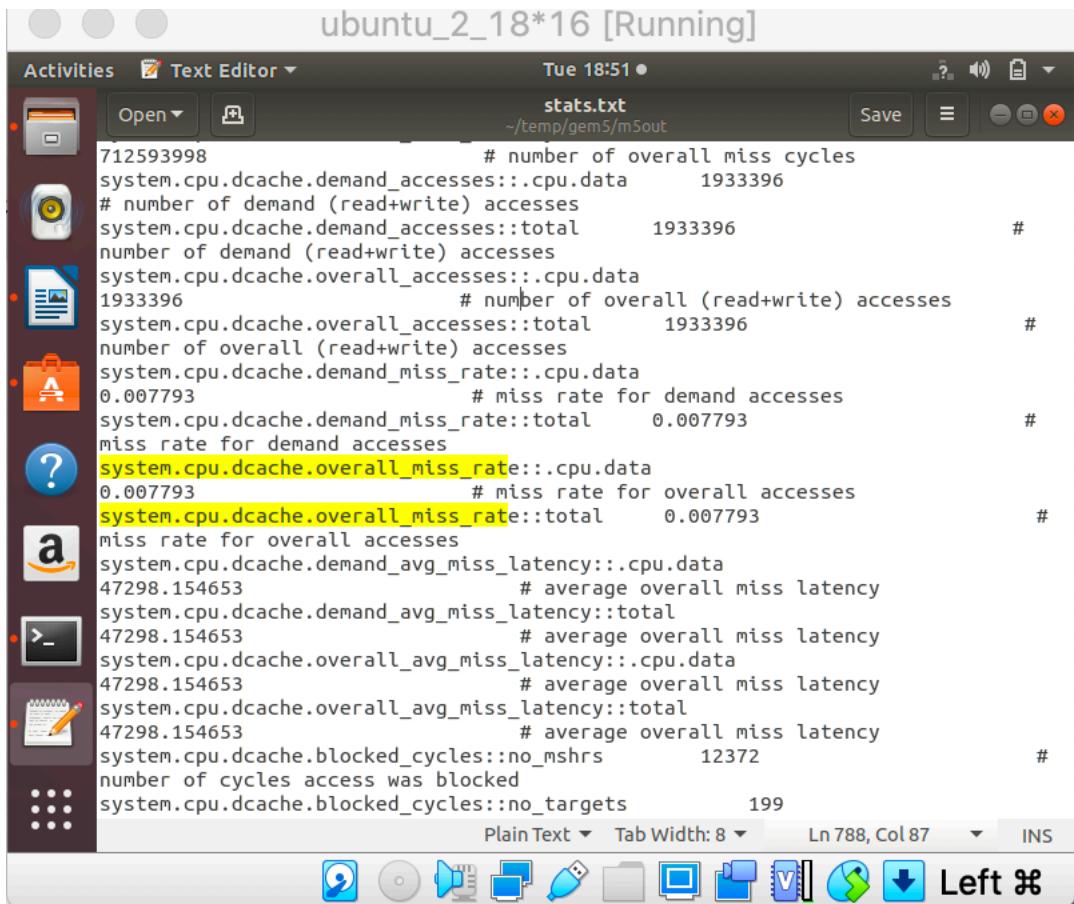
The terminal window has a standard Linux desktop interface with icons for various applications like a file browser, terminal, and system settings.

system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.009400**)

(viii) **Associativity: 8way, size:64kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=64kB --l1d_assoc=8 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o 'c 10' --cpu-clock=2GHz
```



The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The terminal displays simulation statistics from the Gem5 tool. The output includes various cache metrics such as miss counts, miss rates, and average miss latency. The "system.cpu.dcache.overall_miss_rate::cpu.data" metric is highlighted in yellow, showing a value of 0.007793. Other metrics shown include system.cpu.dcache.demand_accesses::cpu.data, system.cpu.dcache.demand_accesses::total, system.cpu.dcache.overall_accesses::cpu.data, system.cpu.dcache.overall_accesses::total, system.cpu.dcache.demand_miss_rate::cpu.data, system.cpu.dcache.demand_miss_rate::total, system.cpu.dcache.overall_miss_rate::cpu.data, system.cpu.dcache.overall_miss_rate::total, system.cpu.dcache.demand_avg_miss_latency::cpu.data, system.cpu.dcache.demand_avg_miss_latency::total, system.cpu.dcache.overall_avg_miss_latency::cpu.data, system.cpu.dcache.overall_avg_miss_latency::total, and system.cpu.dcache.blocked_cycles::no_mshrs.

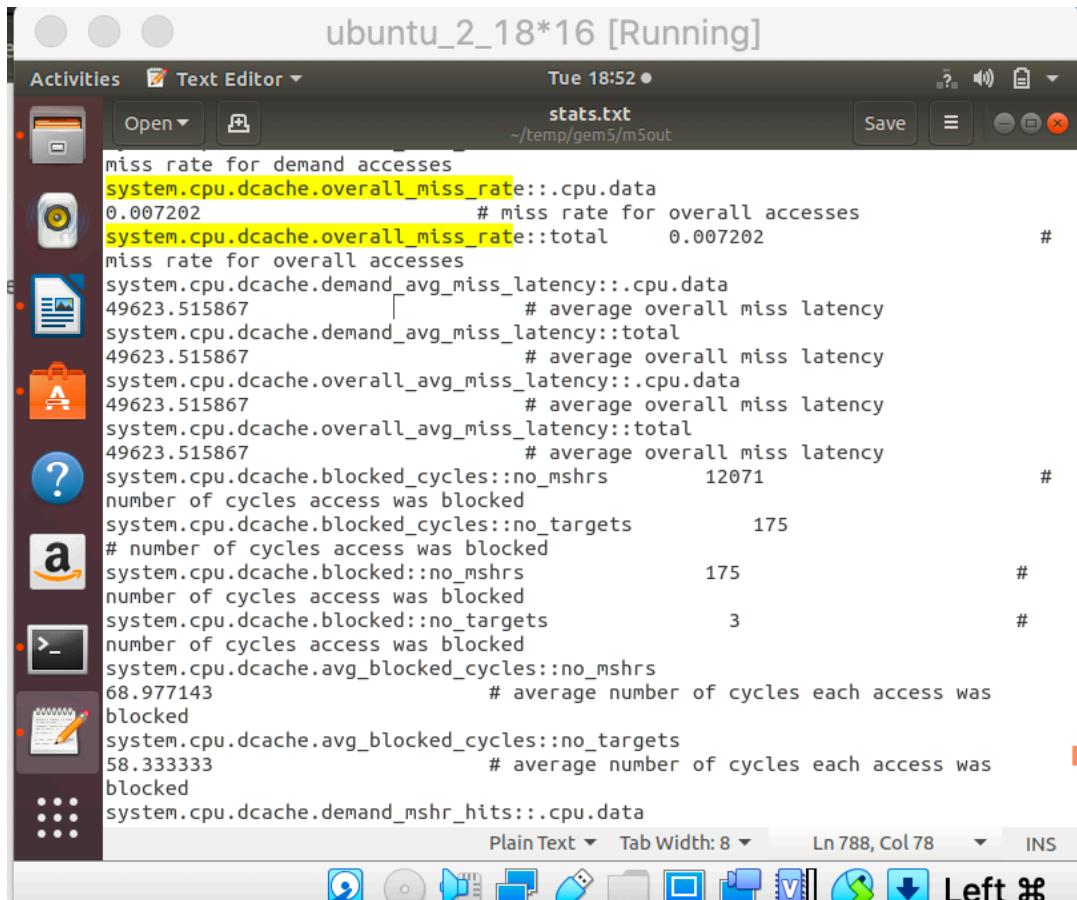
```
712593998          # number of overall miss cycles
system.cpu.dcache.demand_accesses::cpu.data      1933396
# number of demand (read+write) accesses
system.cpu.dcache.demand_accesses::total        1933396          #
number of demand (read+write) accesses
system.cpu.dcache.overall_accesses::cpu.data
1933396          # number of overall (read+write) accesses
system.cpu.dcache.overall_accesses::total        1933396          #
number of overall (read+write) accesses
system.cpu.dcache.demand_miss_rate::cpu.data
0.007793          # miss rate for demand accesses
system.cpu.dcache.demand_miss_rate::total        0.007793          #
miss rate for demand accesses
system.cpu.dcache.overall_miss_rate::cpu.data
0.007793          # miss rate for overall accesses
system.cpu.dcache.overall_miss_rate::total        0.007793          #
miss rate for overall accesses
system.cpu.dcache.demand_avg_miss_latency::cpu.data
47298.154653      # average overall miss latency
system.cpu.dcache.demand_avg_miss_latency::total
47298.154653      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::cpu.data
47298.154653      # average overall miss latency
system.cpu.dcache.overall_avg_miss_latency::total
47298.154653      # average overall miss latency
system.cpu.dcache.blocked_cycles::no_mshrs       12372          #
number of cycles access was blocked
system.cpu.dcache.blocked_cycles::no_targets      199           
```

system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (0.007793)

(ix) **Associativity: 8way, size:512kB**

Gem5 Command:

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=512kB --l1d_assoc=8 -  
-l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --  
cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o '-c 10' --cpu-clock=2GHz
```



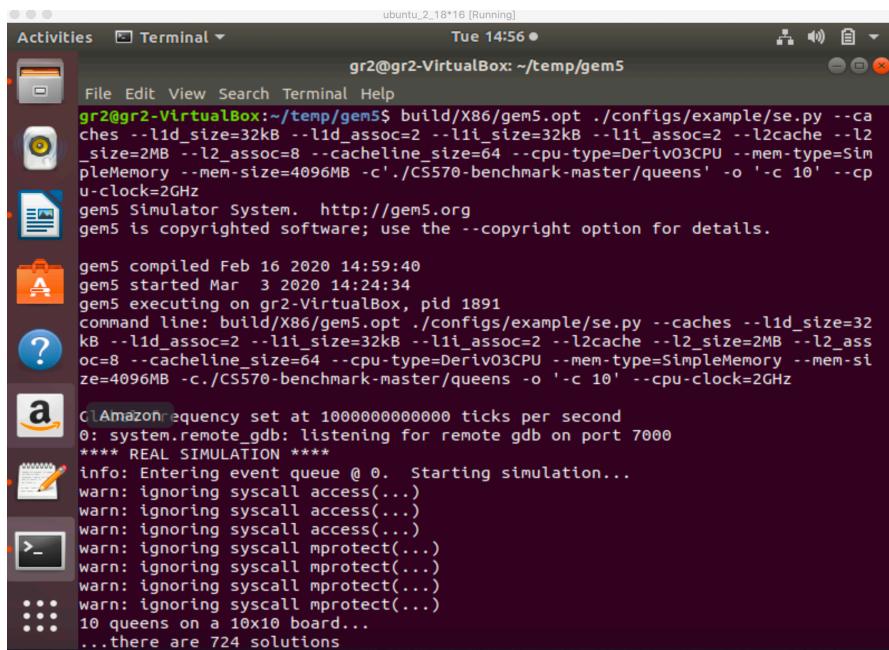
The screenshot shows a terminal window titled "ubuntu_2_18*16 [Running]" running on a Linux desktop. The terminal displays simulation statistics from Gem5. The output includes various cache metrics such as miss rates, average miss latencies, and blocked cycles. A specific line of interest is highlighted in yellow: "system.cpu.dcache.overall_miss_rate::cpu.data 0.007202". This value represents the L1 data cache miss rate.

```
miss rate for demand accesses  
system.cpu.dcache.overall_miss_rate::cpu.data  
0.007202 # miss rate for overall accesses  
system.cpu.dcache.overall_miss_rate::total 0.007202 #  
miss rate for overall accesses  
system.cpu.dcache.demand_avg_miss_latency::cpu.data  
49623.515867 # average overall miss latency  
system.cpu.dcache.demand_avg_miss_latency::total  
49623.515867 # average overall miss latency  
system.cpu.dcache.overall_avg_miss_latency::cpu.data  
49623.515867 # average overall miss latency  
system.cpu.dcache.overall_avg_miss_latency::total  
49623.515867 # average overall miss latency  
system.cpu.dcache.blocked_cycles::no_mshrs 12071 #  
number of cycles access was blocked  
system.cpu.dcache.blocked_cycles::no_targets 175  
# number of cycles access was blocked  
system.cpu.dcache.blocked::no_mshrs 175 #  
number of cycles access was blocked  
system.cpu.dcache.blocked::no_targets 3 #  
number of cycles access was blocked  
system.cpu.dcache.avg_blocked_cycles::no_mshrs  
68.977143 # average number of cycles each access was  
blocked  
system.cpu.dcache.avg_blocked_cycles::no_targets  
58.333333 # average number of cycles each access was  
blocked  
system.cpu.dcache.demand_mshr_hits::cpu.data
```

system.cpu.dache的整体命中率:cpu.data: L1数据缓存命中率 (0.007202)

(x) Associativity: 2way size:32kB

```
build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=32kB --l1d_assoc=8 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o '-c 10' --cpu-clock=2GHz
```



```
ubuntu_2_18*16 [Running]
Activities Terminal Tue 14:56 ●
gr2@gr2-VirtualBox: ~/temp/gem5
File Edit View Search Terminal Help
gr2@gr2-VirtualBox:~/temp/gem5$ build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=32kB --l1d_assoc=2 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o '-c 10' --cpu-clock=2GHz
gem5 Simulator System. http://gem5.org
gem5 is copyrighted software; use the --copyright option for details.

gem5 compiled Feb 16 2020 14:59:40
gem5 started Mar 3 2020 14:24:34
gem5 executing on gr2-VirtualBox, pid 1891
command line: build/X86/gem5.opt ./configs/example/se.py --caches --l1d_size=32kB --l1d_assoc=2 --l1i_size=32kB --l1i_assoc=2 --l2cache --l2_size=2MB --l2_assoc=8 --cacheline_size=64 --cpu-type=DerivO3CPU --mem-type=SimpleMemory --mem-size=4096MB -c'./CS570-benchmark-master/queens' -o '-c 10' --cpu-clock=2GHz

0: Amazon frequency set at 1000000000000 ticks per second
0: system.remote_gdb: listening for remote gdb on port 7000
**** REAL SIMULATION ****
info: Entering event queue @ 0. Starting simulation...
warn: ignoring syscall access(...)
warn: ignoring syscall access(...)
warn: ignoring syscall access(...)
warn: ignoring syscall mprotect(...)
warn: ignoring syscall mprotect(...)
warn: ignoring syscall mprotect(...)
warn: ignoring syscall mprotect(...)

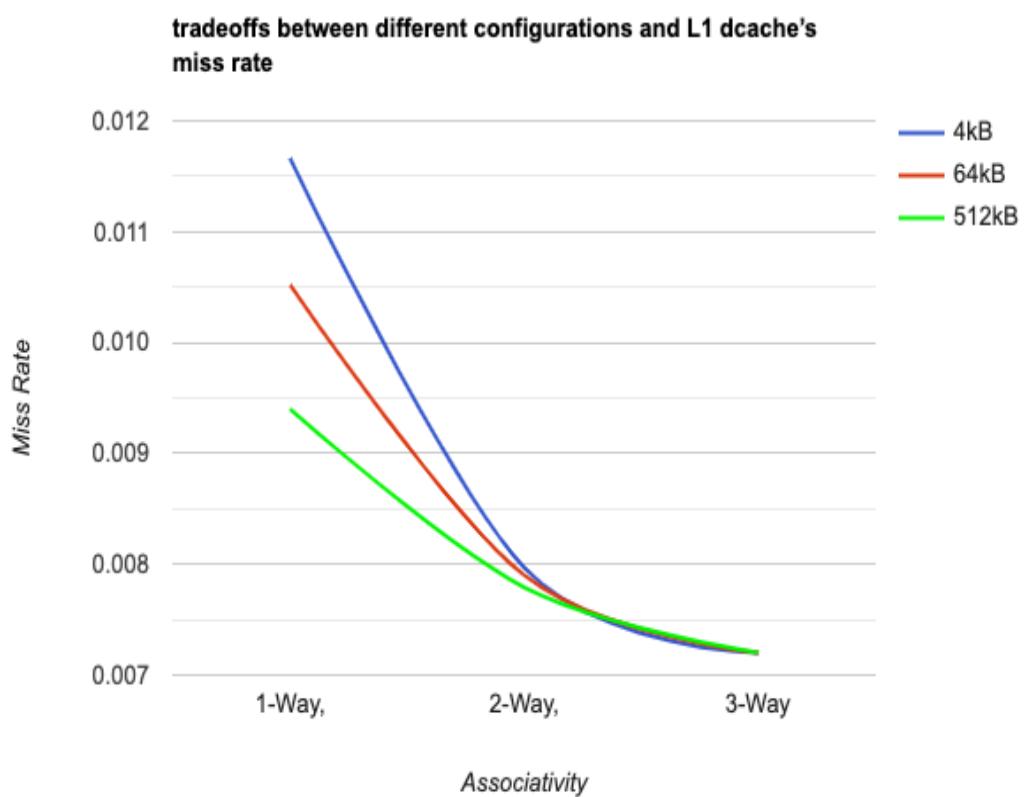
10 queens on a 10x10 board...
...there are 724 solutions
```

stats.txt: contain numerous statistics from the simulation. Interesting statistics include:

1. sim_seconds: simulation time (**0.003004**)
2. system.cpu.ipc: instructions per cycle achieved by the simulated CPU (**0.730768**)
3. system.cpu.dache.overall_miss_rate::cpu.data: L1 data cache miss rate (**0.008261**)
4. system.l2.overall_misses::total: L2 cache miss rate (**3926**)

	4kB	64kB	512kB
1-way	0.011661	0.007973	0.007202
2-way	0.010521	0.007903	0.007202
3-way	0.009400	0.007793	0.007202

tradeoffs between different configurations and L1 dcache's miss rate



Cache size and miss rates

Cache size also has a significant impact on performance In a larger cache there's less chance there will be of a conflict Again this means the miss rate decreases, so the AMAT and number of memory stall cycles also decrease The complete Figure depicts the miss rate as a function of both the cache size and its associativity

Block size and miss rates

Finally, the figure shows miss rates relative to block size and overall cache size Smaller blocks do not take maximum advantage of spatial locality But if blocks are too large, there are fewer blocks available, and more potential conflicts misses