PROJECT STATUS REPORT

Course : B.Tech (Electronics and Communication Engineering)
Project name : Implementation Of Vision For Robots

Completed WORK

DATE	STATUS	DETAILS
11/01/2021	Completed	Implementation of vision for robots on FPGA topic is selected.
18/01/2021	Completed	Literature survey on IJCV paper Distinctive Image Features from Scale-Invariant Keypoints
09/02/2021	Completed	Installation of Xilinx Software
21/02/2021	Completed	Implementation of basic circuits in VHDL using Xilinx
18/04/2021	Completed	Literature survey on different research papers
22/05/2021	Completed	Abstract verification
30/05/2021	Completed	Implemented SIFT in python using Open CV library
14/06/2021	Completed	Implemented SIFT in Matlab and Simulink
28/06/2021	Completed	Implemented SIFT Feature Descriptor Sysgen Model in Xilinx System Generator
03/07/2021	Completed	Conversion of Sysgen Model to HDL code
06/07/2021	Completed	Documentation work

DATE	STATUS	DETAILS
	Yet to be done	Verification of the documentation work

PROJECT STATUS

OVERALL PROJECT STATUS	**90% COMPLETED**	**SUMMARY**	Implemented SIFT Feature Descriptor Sysgen Model in Xilinx System Generator and generate HDL Code

Project Students
B. Gururaja – 17VV1A0407
G. Krishna Rao – 18VV5A0465
K. Eshwar Ajay – 17VV1A0423
K. Sai Charan – 17VV1A0426
Md. Shoaib Shariff – 17VV1A0433

Project Guide
Dr.Ch. Srinivasa Rao
Professor
Department of ECE