Implementation of Vision for Robots

Abstract

Computer Vision[3] is an important feature for Robots in many real time applications. Object detection, recognition and tracking[5] can be done using this vision. The field of computer vision provides number of algorithms for object detection and recognition. Scale Invariant Feature Transform (SIFT)[1][4] is an efficient feature detection algorithm. The Proposed work concentrates on implementation of SIFT algorithm using sophisticated hardware on a Field Programmable Gate Array (FPGA)[2] using Xilinx Software.

The field of digital image processing refers to Processing digital images by means of a digital computer. Before 1960's, the size of a computer was as big as a room. Later due to the invention of transistors and introduction of Very Large Scale Integration (VLSI) technology has drastically changed the size and speed of a computer. The individual components of a computer like Control unit, Arithmetic and Logical Unit and memory can now be integrated on a single chip. Now the size of a computer is as small as our palm. This gives us a good scope in utilisation of these small computers in robots for performing digital image processing in real time environment.

Feature based image matching is a key task in many computer vision applications like object recognition. SIFT Proposed by David Lowe is one of the best feature recognition algorithm. The interesting points of any object in an image are extracted using feature description. This feature description extracted from a training image is then used to identify the object in a test image. The features extracted from the training image must be detectable even under changes in image scale, noise and illumination. Such points usually lie at object edges i.e. on high contrast regions. SIFT feature descriptor is invariant to uniform scaling, orientation and partially invariant to illumination changes.

The first stage in SIFT is Scale Space peak selection which consists of selection of potential interest points which are identified by scanning the image over location and scale. Second stage includes localization of candidate keypoints and are eliminated if found to be unstable. The third stage identifies the dominant orientations for each keypoint. The final stage builds a local image descriptor for each keypoint based upon the image gradients in its local neighbourhood.

Robots in real time need to capture picture using a digital camera. The captured image is to be processed using an onboard computer. This process identifies the features of the image by comparing with the images existing in the database. This robot then takes a necessary action based on the output from the image processing section. For detection of features in an image, SIFT algorithm is used. The day to day improvement in VLSI technology helps in building more efficient hardware processing units for our daily computational purposes. In our research, we will design and implement an efficient hardware on FPGA to run SIFT algorithm. The same concept can be further implemented for modified SIFT[7][8] algorithm also for video processing[6]. The coding for hardware implementation will be done in Very High Speed Integrated Circuit Hardware Description Language (VHDL) on Xilinx Integrated Software Environment(ISE).

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