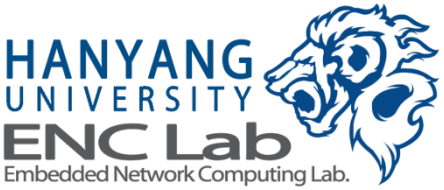
Cosmos OpenSSD Board Starter's Guide ver. 1.1



Revision history

Date	Version	Revision
2015-04-06	1.0	Initial release
2015-06-17	1.1	1.2.1: revised JTAG cable 1.2.2: updated PC ATX pin assignment in table 1 2.1: revised components name 3.1: revised datapath width 3.2: revised figure 2 3.11: updated description of SW2 and SW3 in table 25

Table of Contents

Introduction *Chapter 1*

1.1 About this guide

This document provides an introduction to using the Cosmos openSSD platform board.

This guide describes Cosmos openSSD platform board features and check list. It contains the following chapters:

• Chapter 1, provides general overview.
• Chapter 2, describes Cosmos openSSD platform board overview
• Chapter 3, provides board feature
• Chapter 4, describes jumper and switch settings

1.2 Before starting, check list

1.2.1 Gears

- Cosmos openSSD platform board
- External PCIe adapter
- External PCIe cable
- JTAG cable
  • USB type A to USB type micro B cable (for JTAG digilent module)
  • Emulator, JTAG N pin cable (N: 7, 14, 20)
- USB type A to USB type A cable (for UART)

1.2.2 Check list

Do not plug the **PC ATX power supply 6-pin connector** into J181 on the Cosmos openSSD board. (There is a difference in pin assignment between platform board ATX and PC ATX)
It will be damage the Cosmos openSSD board

Name	Pin number	Connection	
		Cosmos openSSD	PC ATX power
ATX 6pin	1	12 V	GND
	2	12 V	GND
	3	NC	GND
	4	NC	12V
	5	GND	12V
	6	GND	12V

Table 1. Compare with Cosmos openSSD power connector and PC ATX power connector

Before power up the board, check the jumper and switch. Check list is shown in Table 2.

Header	Function	Shunt Position
J177	VCC_NAND_IO voltage select	Position 1–2 = 3.3 V Position 3–4 = 2.5 V Position 5–6 = 1.8V (initial value) Position 7–8 = 1.5V ***Do not place shunt off, it will be damage the board***
J75~79	Boot mode select	Shunt ON (select boot mode using SW5)
SW5	Boot mode select	Position: all on (JTAG mode) More detail, check chapter 3.2 JTAG
SW21	JTAG select	Position 00 = 14pin JTAG Position 01 = JTAG digilent module (initial value) Position 10 = 20pin JTAG More detail, check chapter 3.2 JTAG

Table 2. Jumper and switch setting

Board description *Chapter 2*

2.1 Overview

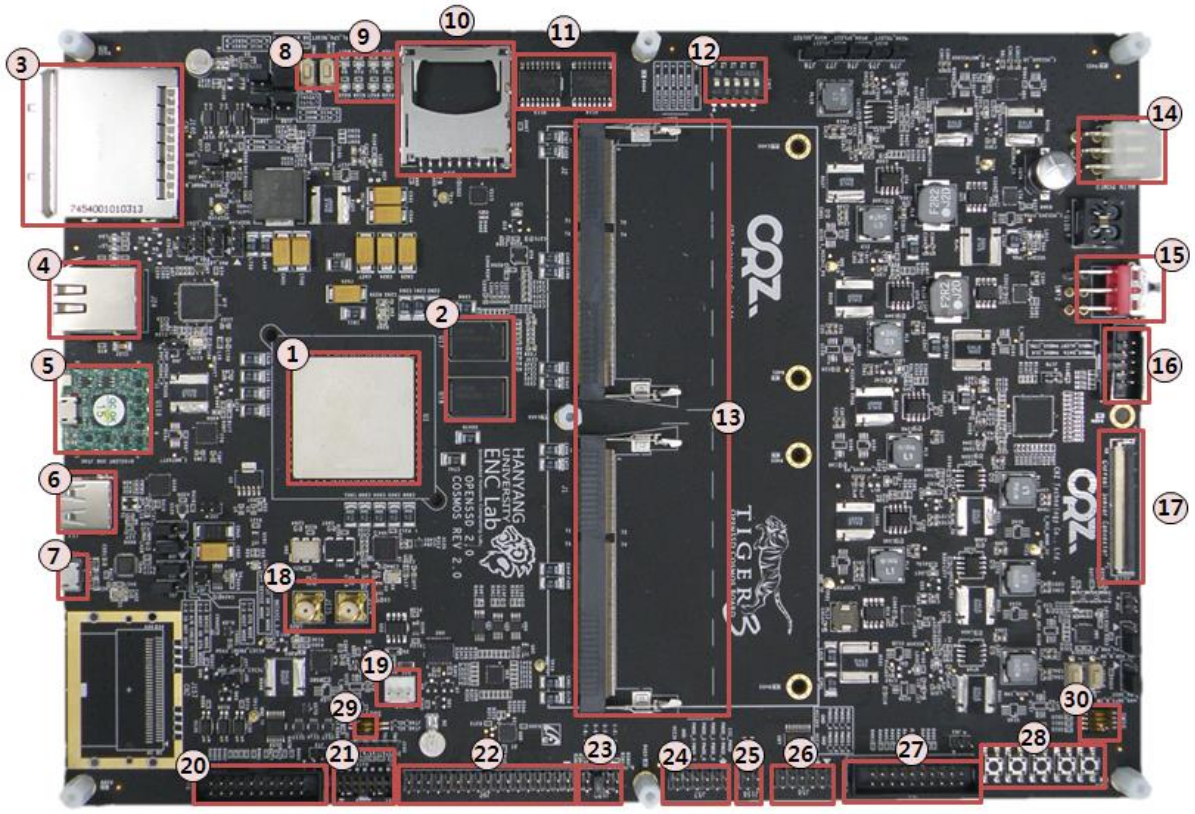


Figure 1. Cosmos openSSD board

Number	Part number	Description
1	U1	XC7Z045-3FFG900 Xilinx Zynq-7000 SoC FPGA
2	U17/U18	DDR3 DRAM
3	CN1	External PCIe connector #1 (support only endpoint)
4	J24	Ethernet connector
5	U116	JTAG digilent module
6	J33	USB connector for USB to UART bridge
7	J22	USB connector for USB 2.0 ULTP
8	SW4/SW10	FPGA_PROG_B (SW4) and PL CPU reset switch (SW10)
9	D9 to 12 D17 to 20	User LEDs
10	J34	SD card connector
11	U113/U114	128 Mb QSPI memory
12	SW5	Configuration mode select switch
13	J1/J2	NAND SO-DIMM connector
14	J181	6pin ATX power connector
15	SW12	Board power switch
16	J71	PMbus connector

17	J178	External power measure module connector
18	J174/J175	SMA connector
19	J67	Fan connector
20	J72	20 pin JTAG connector
21	J69/J180	14 pin and 7 pin JTAG connector
22	J90	User GPIO pin
23	J177	VCCO_ADJ power select pin
24	J57	IIC PMOD pin
25	J156	VCCO_ADJ voltage divide select pin
26	J58	PMOD pin
27	J84	20 pin ARM JTAG connector
28	SW14 to 18	User push buttons
29	SW21	JTAG select switch
30	SW20	User switches

Table 3. Cosmos openSSD part description

Feature description *Chapter 3*

3.1 DDR3 memory

- Part number: K4B2G1646C-HCK0 (Samsung)
- Capacity: 1 GB (4 Gbit x2)
- Datapath width: 32 bits (16 bits x2)
- Data rate: DDR 1066

The connections between the DDR3 component memory and XC7Z045 AP SoC bank 502 are listed in Table 4.

XC7Z045 Pin	Net Name	Component Memory		
		Pin Number	Pin Name	Ref. Des
F25	PS_DDR3_RESET_B	T2	RESETn	U17/U18
E25	PS_DDR3_DQ1	F7	DQL1	U17
A25	PS_DDR3_DQ0	E3	DQL0	U17
D25	PS_DDR3_DQ3	F8	DQL3	U17
B27	PS_DDR3_DM0	E7	DML	U17
C27	PS_DDR3_DQ2	F2	DQL2	U17
B26	PS_DDR3_DQS0_N	G3	DQSLn	U17
C26	PS_DDR3_DQS0_P	F3	DQSL	U17
E26	PS_DDR3_DQ5	H8	DQL5	U17
B25	PS_DDR3_DQ4	H3	DQL4	U17
E27	PS_DDR3_DQ7	H7	DQL7	U17
D26	PS_DDR3_DQ6	G2	DQL6	U17
A27	PS_DDR3_DQ9	C3	DQU1	U17
A29	PS_DDR3_DQ8	D7	DQU0	U17
A28	PS_DDR3_DQ11	C2	DQU3	U17
A30	PS_DDR3_DQ10	C8	DQU2	U17
B30	PS_DDR3_DM1	D3	DMU	U17
B29	PS_DDR3_DQS1_N	B7	DQSUn	U17
C29	PS_DDR3_DQS1_P	C7	DQSU	U17
D30	PS_DDR3_DQ13	A2	DQU5	U17
C28	PS_DDR3_DQ12	A7	DQU4	U17
D29	PS_DDR3_DQ15	A3	DQU7	U17
D28	PS_DDR3_DQ14	B8	DQU6	U17
H23	PS_DDR3_A13	T3	A13	U17/U18
J24	PS_DDR3_A14	T7	A14/NC	U17/U18

H24	PS_DDR3_A11	R7	A11	U17/U18
K23	PS_DDR3_A12	N7	A12/BCn	U17/U18
J23	PS_DDR3_A9	R3	A9	U17/U18
G26	PS_DDR3_A10	L7	A10/AP	U17/U18
K22	PS_DDR3_A7	R2	A7	U17/U18
F27	PS_DDR3_A8	T8	A8	U17/U18
G24	PS_DDR3_A5	P2	A5	U17/U18
H26	PS_DDR3_A6	R8	A6	U17/U18
G25	PS_DDR3_A3	N2	A3	U17/U18
J26	PS_DDR3_A4	P8	A4	U17/U18
K25	PS_DDR3_CLK_P	J7	CK	U17/U18
J25	PS_DDR3_CLK_N	K7	CKn	U17/U18
L27	PS_DDR3_A2	P3	A2	U17/U18
K26	PS_DDR3_A1	P7	A1	U17/U18
L25	PS_DDR3_A0	N3	A0	U17/U18
M25	PS_DDR3_BA2	M3	BA2	U17/U18
M26	PS_DDR3_BA1	N8	BA1	U17/U18
M27	PS_DDR3_BA0	M2	BA0	U17/U18
L23	PS_DDR3_ODT	K1	ODT	U17/U18
N22	PS_DDR3_CS_B	L2	CSn	U17/U18
M22	PS_DDR3_CKE	K9	CKE	U17/U18
N23	PS_DDR3_WE_B	L3	WEn	U17/U18
M24	PS_DDR3_CAS_B	K3	CASn	U17/U18
N24	PS_DDR3_RAS_B	J3	RASn	U17/U18
H27	PS_DDR3_DQ16	E3	DQL0	U18
G27	PS_DDR3_DQ17	F7	DQL1	U18
H28	PS_DDR3_DQ18	F2	DQL2	U18
E28	PS_DDR3_DQ19	F8	DQL3	U18
H29	PS_DDR3_DM2	E7	DML	U18
G29	PS_DDR3_DQS2_P	F3	DQSL	U18
F29	PS_DDR3_DQS2_N	G3	DQSLn	U18
E30	PS_DDR3_DQ20	H3	DQL4	U18
F28	PS_DDR3_DQ21	H8	DQL5	U18
G30	PS_DDR3_DQ22	G2	DQL6	U18
F30	PS_DDR3_DQ23	H7	DQL7	U18
J29	PS_DDR3_DQ24	D7	DQU0	U18
K27	PS_DDR3_DQ25	C3	DQU1	U18
J30	PS_DDR3_DQ26	C8	DQU2	U18

J28	PS_DDR3_DQ27	C2	DQU3	U18
K28	PS_DDR3_DM3	D3	DMU	U18
L28	PS_DDR3_DQS3_P	C7	DQSU	U18
L29	PS_DDR3_DQS3_N	B7	DQSUn	U18
K30	PS_DDR3_DQ28	A7	DQU4	U18
M29	PS_DDR3_DQ29	A2	DQU5	U18
L30	PS_DDR3_DQ30	B8	DQU6	U18
M30	PS_DDR3_DQ31	A3	DQU7	U18

Table 4. The connections between DDR3 component memory and FPGA

3.2 JTAG

The Cosmos openSSD development board JTAG chain is shown in Figure 2.

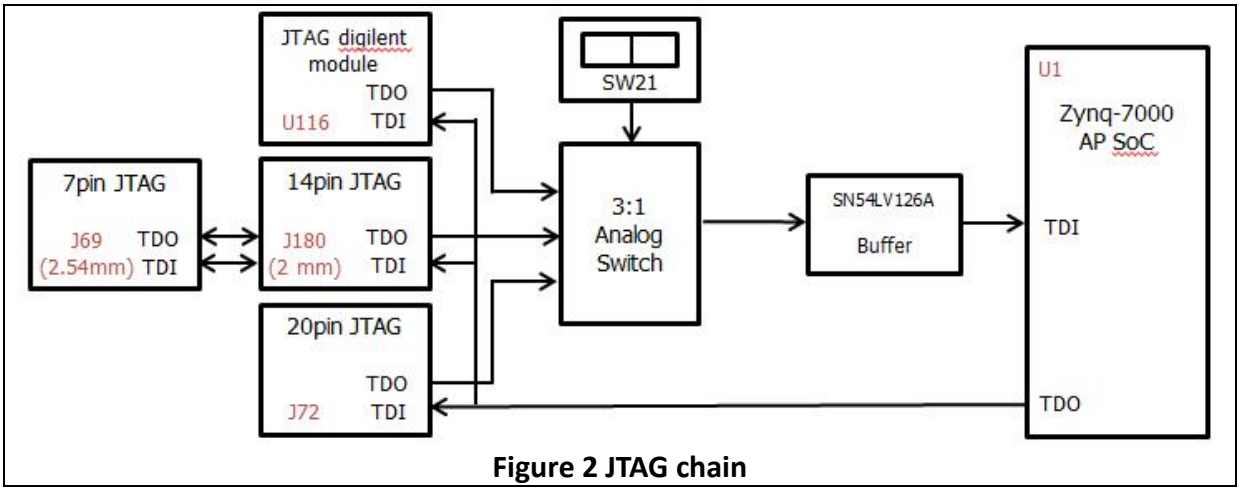


Figure 2 JTAG chain

Name	Description
J69	7pin JTAG connector (2.54 mm pitch)
J180	14pin JTAG connector (2.0 mm pitch)
J72	20pin JTAG connector
U116	JTAG digilent module
J84	20pin ARM PJTAG connector

Table 5. JTAG connector

3.2.1 Programmable logic JTAG select switch

The JTAG chain can be programmed by three different methods made available through a 3-to-1 analog switch (U45, U46, and U47) controlled by a 2-position DIP switch at SW21.

Table 6 shows the JTAG analog switches and DIP switch SW21.

Name	Value		
	14 Pin	Digilent USB	20 Pin

SW21	1	Off	Off	On
	2	Off	On	Off

Table 6. JTAG select switch

3.2.2 Boot mode select switch

Name		Value		
		JTAG	QSPI	SD card
SW5	1	On	On	On
	2	On	On	On
	3	On	On	Off
	4	On	Off	Off
	5	On	On	On
J75, J76, J77, J78, J79		On	On	On

Table 7. Boot mode select switch and jumper

3.3 USB 2.0 transceiver

- Part number: USB3302 USB 2.0 ULPI
- PHY supporting the UTMI+ low pin interface (ULPI) interface standard
- The USB3320 is clocked by a 24 MHz crystal

Table 8 describes the jumper settings for the USB 2.0 circuit.

Header	Function	Shunt Position
J32	USB PHY reset	Shunt ON = USB PHY reset Shunt OFF = USB PHY normal operation
J27	Host/OTG or device	Shunt ON = Host or OTG mode Shunt OFF = Device mode
J28	RVBUS select	Position 1–2 = Device mode (10 KΩ) Position 2–3 = Host or OTG mode (1 KΩ)
J29	CVBUS select	Position 1-2 = 1 µF to GND Position 2-3 = 120 µF to GND
J31	Cable ID select	Position 1-2 = A/B cable detect Position 2-3 = ID not used
J30	USB Type-A	Position 1-2 = Shield connected to GND Position 2-3 = Shield floating

Table 8. Jumper settings for the USB 2.0

Header		Net Name	Description	USB3320 Pin
Pin	Name			
1	VBUS	USB_VBUS_SEL	+5V from host system	22
2	D_N	USB_D_N	Bidirectional differential serial data (N-side)	19
3	D_P	USB_D_P	Bidirectional differential serial data (P-side)	18

4	GND	GND	Signal ground	33

Table 9. The connections between the USB connector () and PHY

XC7Z045			Schematic Net Name	SB3320 Pin
Pin NAME	Bank	Pin Number		
PS_MIO36	501	H17	USB_CLKOUT	1
PS_MIO31	501	H21	USB_NXT	2
PS_MIO32	501	K17	USB_DATA0	3
PS_MIO33	501	G22	USB_DATA1	4
PS_MIO34	501	K18	USB_DATA2	5
PS_MIO35	501	G21	USB_DATA3	6
PS_MIO28	501	L17	USB_DATA4	7
PS_MIO37	501	B21	USB_DATA5	9
PS_MIO38	501	A20	USB_DATA6	10
PS_MIO39	501	F18	USB_DATA7	13
PS_MIO30	501	L18	USB_STP	29
PS_MIO29	501	H22	USB_DIR	31
PS_MIO7	501	B24	USB_RESET_B_AND	27

Table 10. The connections between USB PHY and FPGA

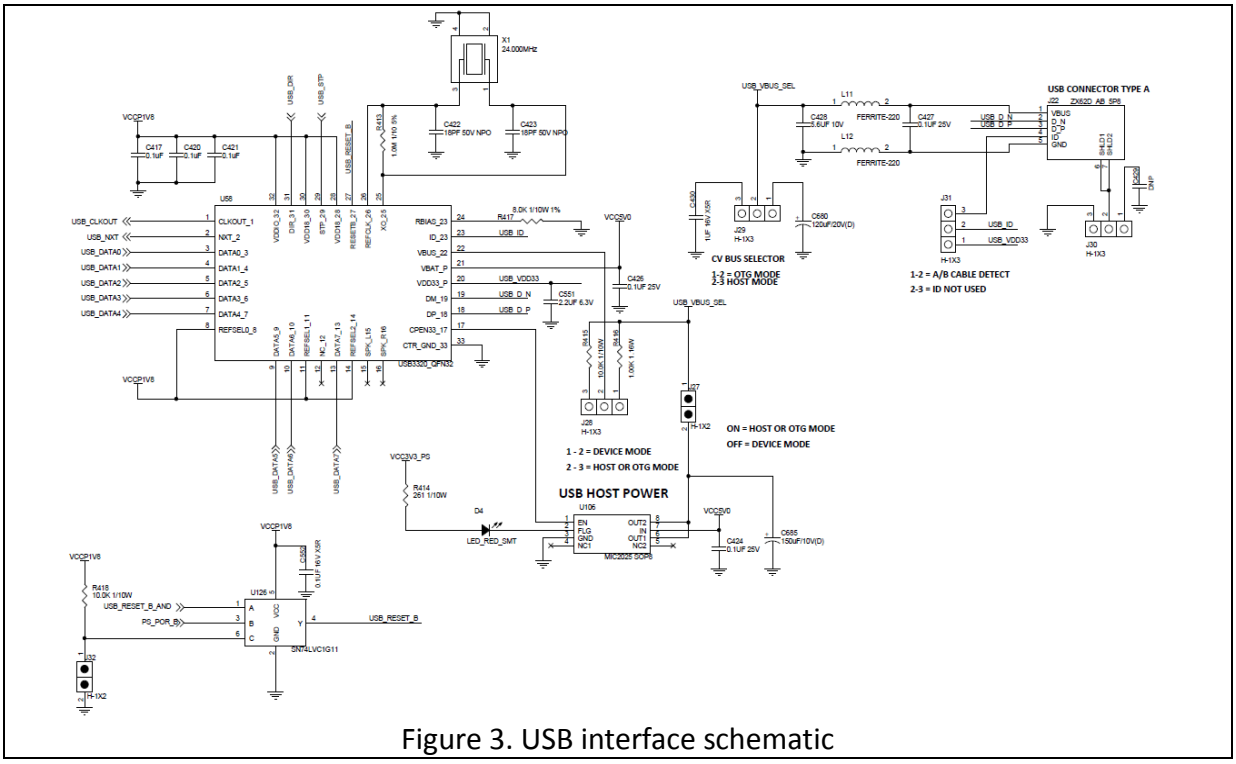


Figure 3. USB interface schematic

3.4 SD card interface

Figure 4 shows the connections of the SD card interface on the Cosmos openSSD

development board

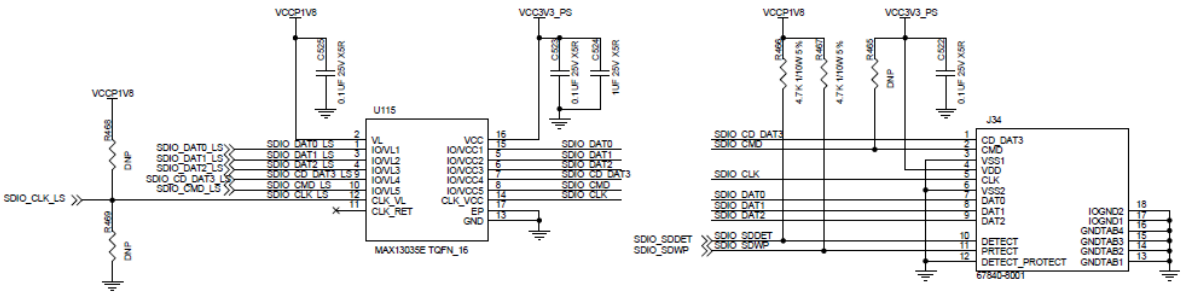


Figure 4 SD card interface schematic

XC7Z045			Schematic Net Name	Level Shifter		SDIO Connector	
Pin NAME	Bank	Pin Number		1.8V Side Pin	3.3V Side Pin	Pin Number	Pin Name
PS_MIO15	500	C22	SDIO_SDWP	N/A	N/A	11	PROTECT
PS_MIO14	500	B22	SDIO_SDDET	N/A	N/A	10	DETECT
PS_MIO41	501	J18	SDIO_CMD_LS	10	8	2	CMD
PS_MIO40	501	B20	SDIO_CLK_LS	12	14	5	CLK
PS_MIO44	501	E20	SDIO_DAT2_LS	4	6	9	DAT2
PS_MIO43	501	E18	SDIO_DAT1_LS	3	5	8	DAT1
PS_MIO42	501	D20	SDIO_DAT0_LS	1	15	7	DAT0
PS_MIO45	501	H18	SDIO_CD_DAT3_LS	9	7	1	CD_DAT3

Table 11. The connections between SD card and FPGA

3.5 Quad-SPI flash memory

- Part number: S25FL128SAGMFIR01 (Spansion)
- Supply voltage: 1.8V
- Datapath width: 4 bits
- Data rate: Various depending on Single/Dual/Quad mode

The connections between the SPI flash memory and the XC7Z045 AP SoC are listed in Table 12.

XC7Z045 (U1)			Schematic Net Name	Quad-SPI Flash memory		QSPI Device	MIO Select Header
Pin name	Bank	Pin Number		Pin number	Pin name	Ref.Des	
PS_MIO1	500	D23	QSPI0_CS_B	7	CS_B	U113	N/A
PS_MIO6	500	D24	QSPI0_CLK	16	SCK	U113	J79.1
PS_MIO2	500	F23	QSPI0_IO0	15	SI_IO0	U113	J78.1
PS_MIO3	500	C23	QSPI0_IO1	8	SO_IO1	U113	J77.1
PS_MIO4	500	E23	QSPI0_IO2	9	WP_B_IO2	U113	J76.1
PS_MIO5	500	C24	QSPI0_IO3	1	HOLD_B_IO3	U113	J75.1
PS_MIO0	500	F24	QSPI1_CS_B	7	CS_B	U114	N/A
PS_MIO9	500	A24	QSPI1_CLK	16	SCK	U114	N/A
PS_MIO10	500	E22	QSPI1_IO0	15	SI_IO0	U114	N/A
PS_MIO11	500	A23	QSPI1_IO1	8	SO_IO1	U114	N/A
PS_MIO12	500	E21	QSPI1_IO2	9	WP_B_IO2	U114	N/A
PS_MIO13	500	F22	QSPI1_IO3	1	HOLD_B_IO3	U114	N/A

Table 12. The connection between QSPI flash memory and FPGA

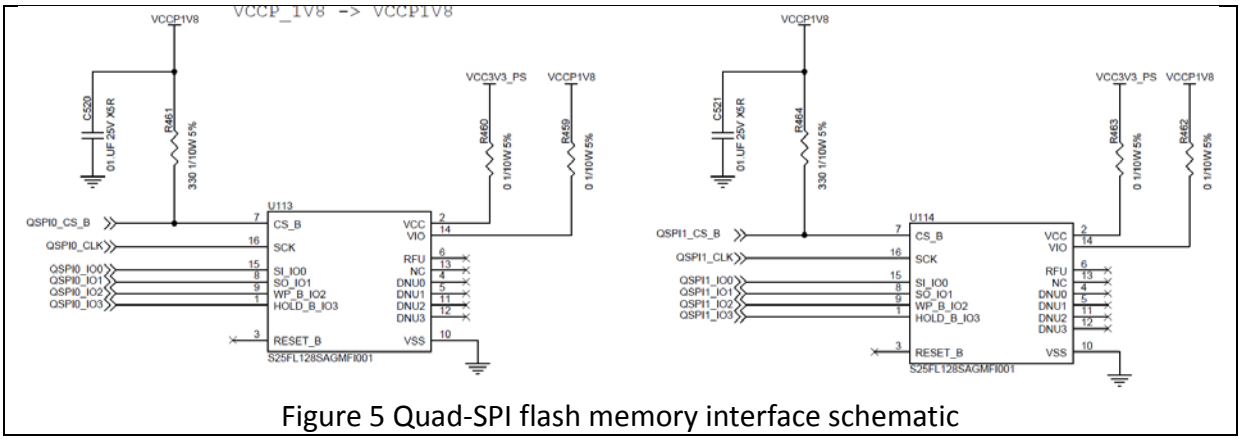


Figure 5 Quad-SPI flash memory interface schematic

3.6 Clock

The Cosmos openSSD development board provides five clock sources for the XC7Z045 AP SoC. Table 13 lists the source devices for each clock.

Clock Name	Clock Source	Description
System Clock	U61	SiT9102 2.5V LVDS 200 MHz fixed-frequency oscillator (SiTime).
User Clock	U62	Si570 3.3V LVDS I2C programmable oscillator, 156.250 MHz default(Silicon Labs).
SMA clock	J174/J175	User clock input SMAs.
PS Clock	U63	SIT8103 1.8V single-ended CMOS 33.3333 MHz fixed frequency oscillator (SiTime).
Jitter Attenuated Clock	U54	Si5324C LVDS precision clock multiplier/jitter attenuator (Silicon Labs).

Table 13. Cosmos openSSD clock source list

Clock Source Pin	Net Name	XC7Z045 Pin
U61.4	SYSCLK_P	AG17
U61.5	SYSCLK_N	AG16
U62.4	USRCLK_P	AF14
U62.5	USRCLK_N	AG14
U63.3	PS_CLK	A22
U54.28	SI5324_OUT_P	AC8
U54.29	SI5324_OUT_N	AC7
J174.1	SMA_MGT_REFCLK_P	AD10
J175.1	SMA_MGT_REFCLK_N	AD9

Table 14. Lists the pin to pin connections from each clock source to the FPGA

3.6.1 System clock

- Oscillator: SiTime SiT9102AI-243N25E200.00000 (200 MHz)
- Frequency jitter: 50 ppm
- LVDS Differential Output

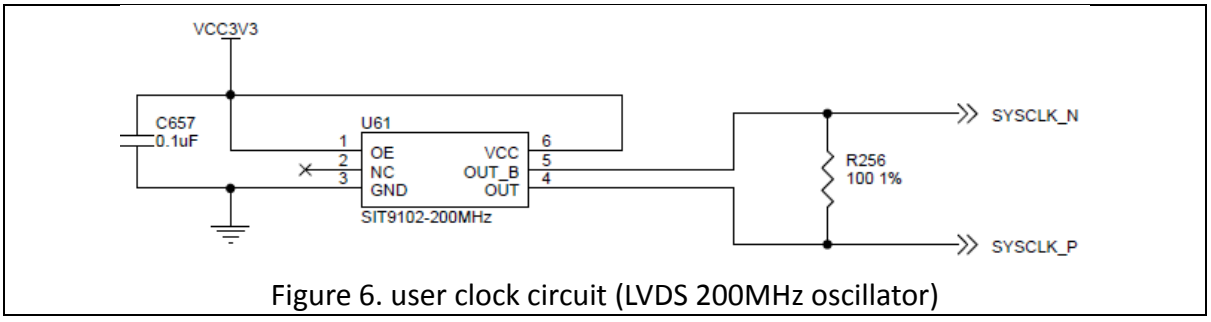


Figure 6. user clock circuit (LVDS 200MHz oscillator)

3.6.2 Programmable user clock

- Programmable Oscillator: Silicon Labs Si570BAB0000544DG (10 MHz–810 MHz)
- Default frequency: 156.250 MHz
- Frequency jitter: 50 ppm
- LVDS Differential Output

The user clock circuit is shown in Figure 7.

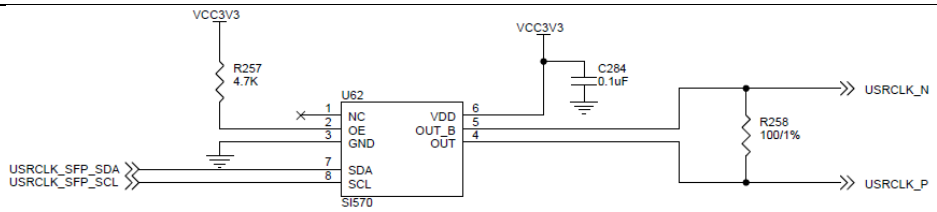


Figure 7. user clock circuit (configurable LVDS up to 810Mhz oscillator)

3.6.3 Processing system clock

- Oscillator: SiTime SiT8103AC-23-18E-33.33333 (33.3 MHz)
- Frequency jitter: 50 ppm
- Single-ended output (LVCMOS 1.8V)

The system clock circuit is shown in Figure 8.

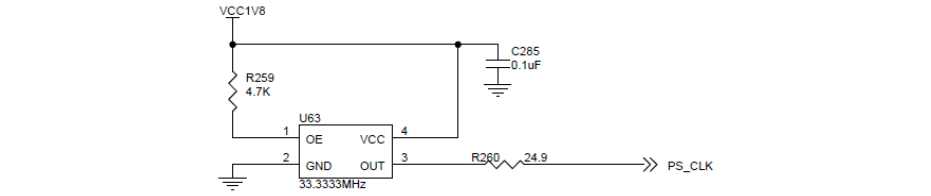


Figure 8. PS system clock circuit

3.6.4 GTX SMA clock

- External user-provided GTX reference clock on SMA input connectors
- Differential Input

Figure 9 shows this AC-coupled clock circuit.

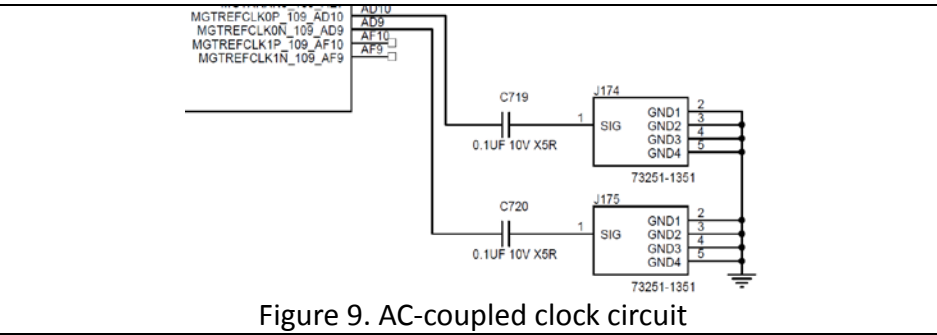


Figure 9. AC-coupled clock circuit

3.6.5 Jitter attenuated clock

The Cosmos SSD development board a Silicon Labs Si5324 jitter attenuator U60 on the back side of the board. AP SoC user logic can implement a clock recovery circuit and then output this clock to a differential I/O pair on I/O bank 9 (REC_CLOCK_C_P, AP SoC U1 pin AD20 and REC_CLOCK_C_N, AP SoC U1 pin AE20) for jitter attenuation. The jitter attenuated clock (Si5324_OUT_C_P, Si5324_OUT_C_N) is then routed as a reference clock to GTX Quad 110 inputs MGTREFCLK1P (AP SoC U1 pin AC8) and MGTREFCLK1N (AP SoC U1 pin AC7).
The primary purpose of this clock is to support CPRI/OBSAI applications that perform clock recovery from a user-supplied SFP/SFP+ module and use the jitter attenuated recovered clock to drive the reference clock inputs of a GTX transceiver. The jitter attenuated clock circuit is shown in Figure 10.

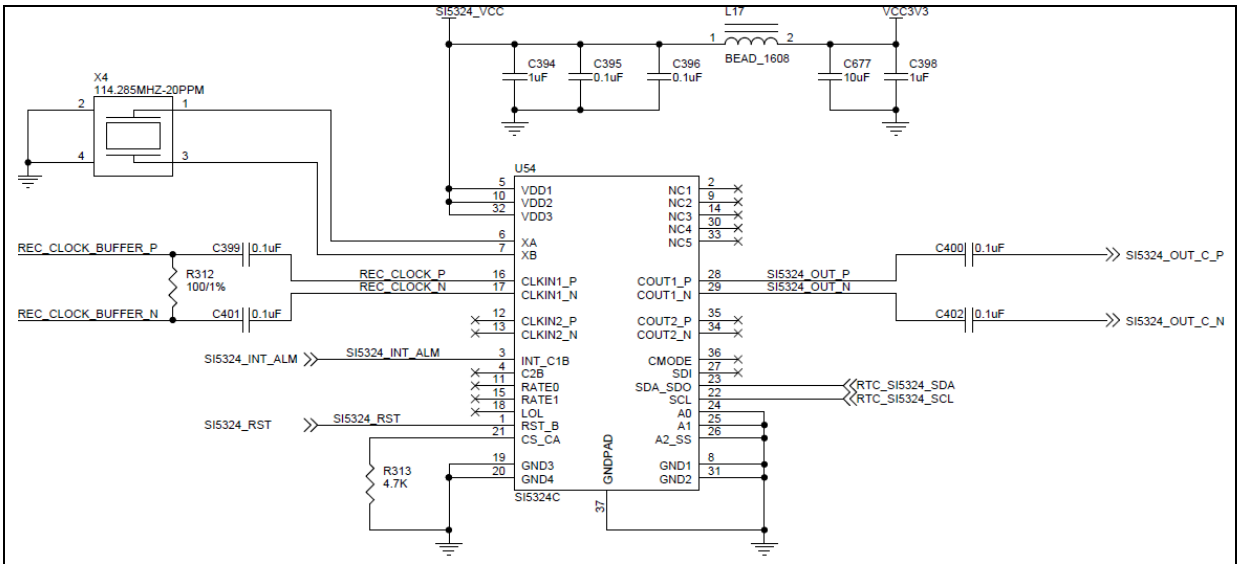


Figure 10. The jitter attenuated clock circuit

3.7 GTX transceivers

The Cosmos SSD development board provides access to 16 GTX transceivers:
• Eight of the GTX transceivers are wired to the External PCI Express x8 endpoint edge connector (CN1) fingers
• Eight of the GTX transceivers are wired to the External PCI Express x8 endpoint edge connector (CN2) fingers

The GTX transceivers in Zynq-7000 series AP SoCs are grouped into four channels described as Quads. The reference clock for a Quad can be sourced from the Quad above or Quad below the GTX Quad of interest. There are four GTX Quads on the Cosmos SSD development board with connectivity as shown here:

Bank	Connectivity
Bank 109	MGTREFCLK0 – SMA Clock

	MGTREFCLK1 - not connected
	Contains 4 GTX transceivers allocated to PCIE2[4:7]
Bank 110	MGTREFCLK0 – PCIE2_CLK_Q0 PCIE Reference clock
	MGTREFCLK1 - SI5324_OUT_C_P/N jitter attenuator clock
	Contains 4 GTX transceivers allocated to PCIE2[0:3]
Bank 111	MGTREFCLK0 - not connected
	MGTREFCLK1 - not connected
	Contains 4 GTX transceivers allocated to PCIE1[4:7]
Bank 112	MGTREFCLK0 – PCIE1_CLK_Q0 PCIE Reference clock
	MGTREFCLK1 - not connected
	Contains 4 GTX transceivers allocated to PCIE1[0:3]

Table 15. The connections between GTX Quad and Cosmos openSSD board

Table 16 to 19 lists the GTX Banks 109 and 110 interface connections between the FPGA and External PCIE Connector.

Transceiver Bank	FPGA Pin Number	Schematic Net Name	Connected Pin	Connected Device
GTX_BANK_109	AK10	PCIE2_TX7_P	A32	External PCIE Connector
	AK9	PCIE2_TX7_N	A33	
	AH10	PCIE2_RX7_P	B32	
	AH9	PCIE2_RX7_N	B33	
	AK6	PCIE2_TX6_P	A29	
	AK5	PCIE2_TX6_N	A30	
	AJ8	PCIE2_RX6_P	B29	
	AJ7	PCIE2_RX6_N	B30	
	AJ4	PCIE2_TX5_P	A26	
	AJ3	PCIE2_TX5_N	A27	
	AG8	PCIE2_RX5_P	B26	
	AG7	PCIE2_RX5_N	B27	
	AK2	PCIE2_TX4_P	A23	
	AK1	PCIE2_TX4_N	A24	
	AE8	PCIE2_RX4_P	B23	
	AE7	PCIE2_RX4_N	B24	
	AD10	SMA_CLK_P	-	SMA
	AD9	SMA_CLK_N	-	SMA
	AF10	NC		
	AF9	NC		

Table 16. The GTX bank 109 connections between FPGA and external PCIe connecter

Transceiver Bank	FPGA Pin Number	Schematic Net Name	Connected Pin	Connected Device

GTX_BANK_110	AH2	PCIE2_TX3_P	A11	External PCIE Connector
	AH1	PCIE2_TX3N	A12	
	AH6	PCIE2_RX3_P	B11	
	AH5	PCIE2_RX3_N	B12	
	AF2	PCIE2_TX2P	A8	
	AF1	PCIE2_TX2N	A9	
	AG4	PCIE2_RX2_P	B8	
	AG3	PCIE2_RX2_N	B9	
	AE4	PCIE2_TX1_P	A5	
	AE3	PCIE2_TX1_N	A6	
	AF6	PCIE2_RX1_P	B5	
	AF5	PCIE2_RX1_N	B6	
	AD2	PCIE2_TX0_P	A2	
	AD1	PCIE2_TX0_N	A3	
	AD6	PCIE2_RX0_P	B2	
	AD5	PCIE2_RX0_N	B3	
	AA8	PCIE2_CLK_Q0_P	A14	
	AA7	PCIE2_CLK_Q0_N	A15	
	AC8	SI5324_OUT_C_P	28	SI5324
	AC7	SI5324_OUT_C_P	29	

Table 17. The GTX bank 110 connections between FPGA and external PCIe connecter

Transceiver Bank	FPGA Pin Number	Schematic Net Name	Connected Pin	Connected Device
GTX_BANK_111	AB2	PCIE_TX7_P	A32	External PCIE Connector
	AB1	PCIE_TX7_N	A33	
	AC4	PCIE_RX7_P	B32	
	AC3	PCIE_RX7_N	B33	
	Y2	PCIE_TX6_P	A29	
	Y1	PCIE_TX6_N	A30	
	AB6	PCIE_RX6_P	B29	
	AB5	PCIE_RX6_N	B30	
	W4	PCIE_TX5_P	A26	
	W3	PCIE_TX5_N	A27	
	Y6	PCIE_RX5_P	B26	
	Y5	PCIE_RX5_N	B27	
	V2	PCIE_TX4_P	A23	
	V1	PCIE_TX4_N	A24	
	AA4	PCIE_RX4_P	B23	

	AA3	PCIE_RX4_N	B24	
	U8	NC		
	U7	NC		
	W8	NC		
	W7	NC		

Table 18. The GTX bank 111 connections between FPGA and external PCIe connecter

Transceiver Bank	FPGA Pin Number	Schematic Net Name	Connected Pin	Connected Device
GTX_BANK_112	T2	PCIE_TX3_P	A11	External PCIE Connector
	T1	PCIE_TX3N	A12	
	V6	PCIE_RX3_P	B11	
	V5	PCIE_RX3_N	B12	
	R4	PCIE_TX2P	A8	
	R3	PCIE_TX2N	A9	
	U4	PCIE_RX2_P	B8	
	U3	PCIE_RX2_N	B9	
	P2	PCIE_TX1_P	A5	
	P1	PCIE_TX1_N	A6	
	T6	PCIE_RX1_P	B5	
	T5	PCIE_RX1_N	B6	
	N4	PCIE_TX0_P	A2	
	N3	PCIE_TX0_N	A3	
	P6	PCIE_RX0_P	B2	
	P5	PCIE_RX0_N	B3	
	N8	PCIE_CLK_Q0P	A14	
	N7	PCIE_CLK_Q0N	A15	
	R8	NC		
	R7	NC		

Table 19. The GTX bank 109 connections between FPGA and external PCIe connecter

3.8 External PCI Express

The 8-lane External PCI Express connector performs data transfers at the rate of 2.5 GT/s for a Gen1 application and 5.0 GT/s for a Gen2 application. The PCIe transmit and receive signal data paths have a characteristic impedance of 85Ω ±10%. The PCIe clock is routed as a 100Ω differential pair.

The XC7Z045-3FFG900C AP SoC (-3 speed grade) included with the The Cosmos SSD development board supports up to 2ea Gen2 x8. The PCIe clock is input from the edge connector. It is AC coupled to the AP SoC through the MGTREFCLK0 pins of Quad 112. PCIE_CLK_Q0_P is connected to AP SoC U1 pin N8, and the _N net is connected to pin N7. The PCI Express clock circuit is shown in Figure 11.

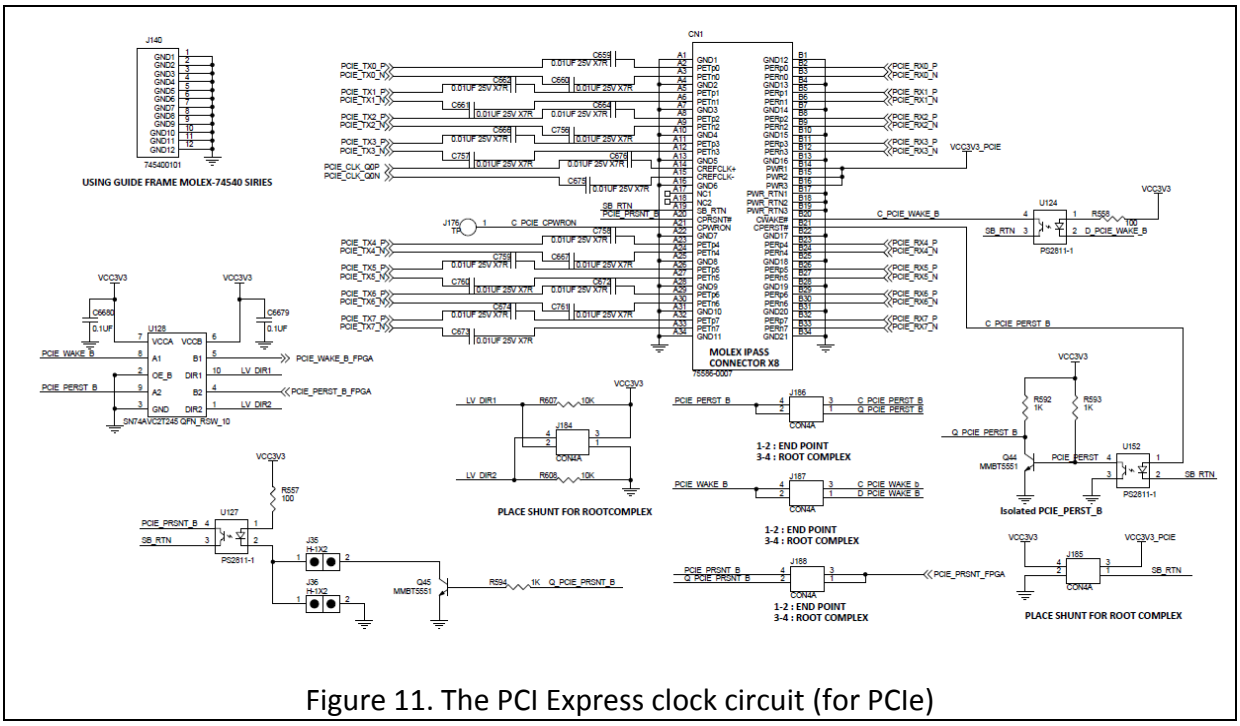


Figure 11. The PCI Express clock circuit (for PCIe)

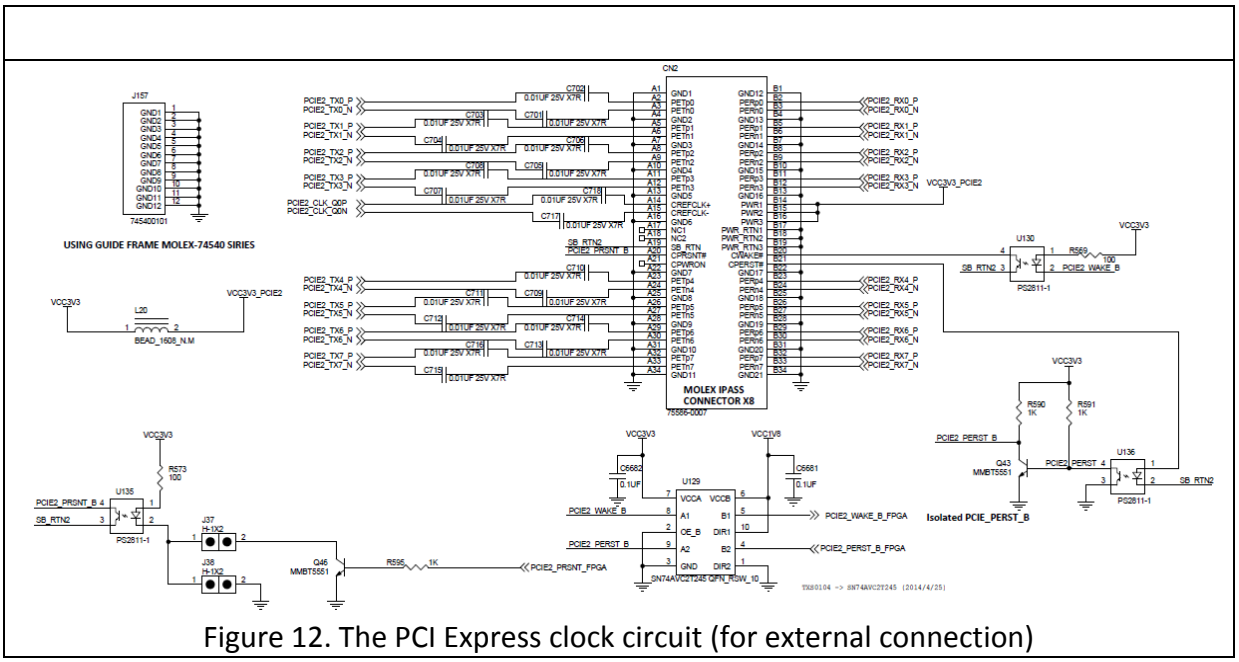


Figure 12. The PCI Express clock circuit (for external connection)

3.9 USB to UART bridge

The Cosmos SSD development board contains a Silicon Labs CP2103GM USB-to-UART bridge device (U52) which allows a connection to a host computer with a USB port. The

CP2103GM is powered by the USB 5V provided by the host PC when the USB cable is plugged into the USB port on the Cosmos SSD development board.

The CP2013GM TX and RX pins are wired to the UART_1 IP block within the XC7Z045 AP SoC PS I/O Peripherals set. The XC7Z045 AP SoC supports the USB-to-UART bridge using two signal pins: Transmit (TX) and Receive (RX).

Silicon Labs provides royalty-free Virtual COM Port (VCP) drivers for the host computer. These drivers permit the CP2103GM USB-to-UART bridge to appear as a COM port to communications application software that runs on the host computer. The VCP device drivers must be installed on the host PC prior to establishing communications with the Cosmos SSD development board.

USB Connector		Net Name	Description	CP2103GM	
Pin	Name			Pin	Name
1	VBUS	USB_UART_VBUS	+5V VBUS POWERED	7	REGIN
				8	VBUS
2	D_N	USB_UART_D_N	Bidirectional differential serial data (N-side)	4	D-
3	D_P	USB_UART_D_P	Bidirectional differential serial data (P-side)	3	D+
5	GND	USB_UART_GND	Signal ground	2	GND1
				29	CNR_GND

Table 20. The USB Connector pin assignments and signal definitions

XC7Z045 AP SoC						Schematic Net Name	CP2103GM Device		
Pin Name	Bank	Pin	Fucntion	Direction	IOSTANDARD		Pin	Function	Direction
PS_MIO48	501	C19	TX	Output	LVCMOS18	USB_UART_RX	24	RXD	Input
PS_MIO49	501	D18	RX	Input	LVCMOS18	USB_UART_TX	25	TXD	Output

Table 21. The USB connections between CP2103 UART bridge and FPGA

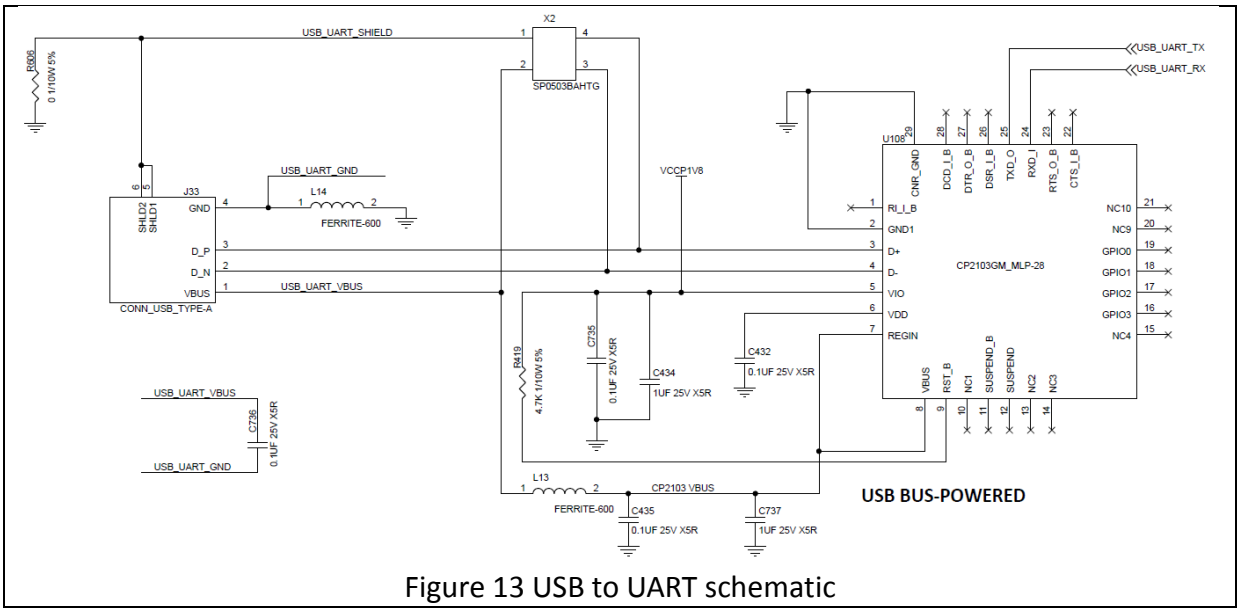


Figure 13 USB to UART schematic

3.10 I2C bus

The Cosmos SSD development board implements two I2C ports on the XC7Z045 AP SoC. The PL-side I2C port (IIC_SDA and _SCL_MAIN) is routed to level shifter U89. The PS-side I2C port (PS_SDA and _SCL_MAIN) is routed to level shifter U90. The "output" side of the two level shifters are wired to the common I2C bus IIC_SDA and _SCL_MAIN which is connected to TI Semiconductor PCA9548 1-to-8 channel I2C bus switch (U93). The bus switch can operated at speeds up to 400 kHz.

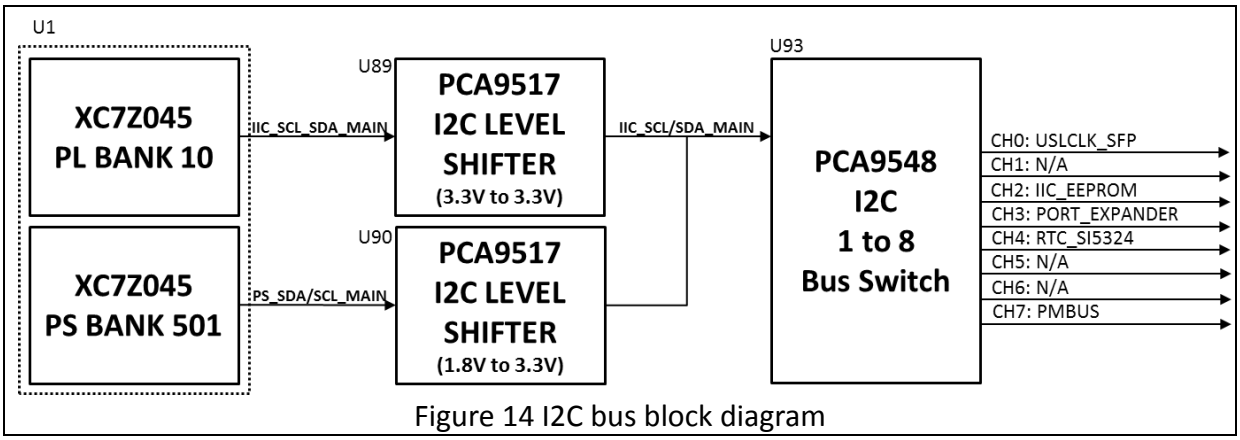


Figure 14 I2C bus block diagram

I2C Bus	I2C Switch Position	I2C Address	Device
PCA9648 8 Channel bus swtich	NA	0b1110100	PCA9548 (U93)
USRCLK_SFP	0	0b1011101	Si570 (U62)
IIC_EEPROM	2	0b1010100	M24C08 (U91)
PORT_EXPANDER	3	0b1000000	Port Expander (U20)
RTC_SI5324	4	0b1010001	RTC8564JE (U92)
		0b1101000	SI5324 (U54)
PMBUS	7	0b1100101	UCD90120A (U102)

Table 22. I2C Switch

3.11 Status, User LEDs and Switches

Reference Designator	Net Name	LED Color	Description
LD11	POR	GREEN	Processor System
LD5	FPGA_INIT_B	GREEN/ RED	Green: FPGA initialization was Successful Red: FPGA initialization is in progress
LD1	DONE	GRREN	FPGA bit file download is complete
LD25	MGTAVCC	GREEN	MGTAVCC Power on indicator LED

LD19	MGTAVTT	GREEN	MGTAVTT Power on indicator LED
LD24	VCCAUX_IO	GREEN	VCCAUX_IO Power on indicator LED
LD21	MGTVCCAUX	GREEN	MGTVCCAUX Power on indicator LED
LD6	LINEAR_POWER_GOOD	GREEN	LINEAR_POWER_GOOD Power on indicator LED
LD23	VCC_NAND	GREEN	VCC_NAND Power on indicator LED
LD26	VCC_NAND_IO	GREEN	VCC_NAND_IO Power on indicator LED
LD27	VCCO_ADJ	GREEN	VCCO_ADJ Power on indicator LED
LD22	VCC3V3_FPGA	GREEN	VCC3V3_FPGA Power LED
LD26	VCC3V3	GREEN	VCC3V3 Power on indicator LED
LD29	VCC5V0	GREEN	VCC5V0 Power on indicator LED
LD20	VCCINT	GREEN	VCCINT Power on indicator LED
LD30	VCCAUX	GREEN	VCCAUX Power on indicator LED
LD15	VCC12_P	GREEN	VCC12_P Power on indicator LED
LD17	CTRL1_PWRGOOD	GREEN	Power Controller controlled voltage regulator outputs are all ≥ their minimum "good" threshold
LD16	VCCPINT	GREEN	VCCPINT Power LED
LD13	VCCP1V8_FPGA	GREEN	VCCP1V8_FPGA Power LED
LD8	VCC3V3_PS	GREEN	VCC3V3_PS Power LED
LD10	PS_DDR_LINEAR_PG	GREEN	PS_DDR_LINEAR_PG Power LED
LD12	VCC1V5_PS	GREEN	VCC1V5_PS Power LED
LD2	PHY_LED0	GREEN	Ethernet PHY LED0
LD3	PHY_LED1	GREEN	Ethernet PHY LED1
LD4	PHY_LED2	GREEN	Ethernet PHY LED2
D4	U106_FLG	RED	USB 2.0 MOSFET Power switch fault

Table 23. Status LEDs

Reference Designator	Net Name	LED Color	Description
D9	USER_LED_R_0	RED	General Purpose user LED 0
D10	USER_LED_R_1	RED	General Purpose user LED 1
D11	USER_LED_R_2	RED	General Purpose user LED 2
D12	USER_LED_R_3	RED	General Purpose user LED 3
D17	USER_LED_G_0	GREEN	General Purpose user LED 4
D18	USER_LED_G_1	GREEN	General Purpose user LED 5
D19	USER_LED_G_2	GREEN	General Purpose user LED 6
D20	USER_LED_G_3	GREEN	General Purpose user LED 7

Table 24. User LEDs

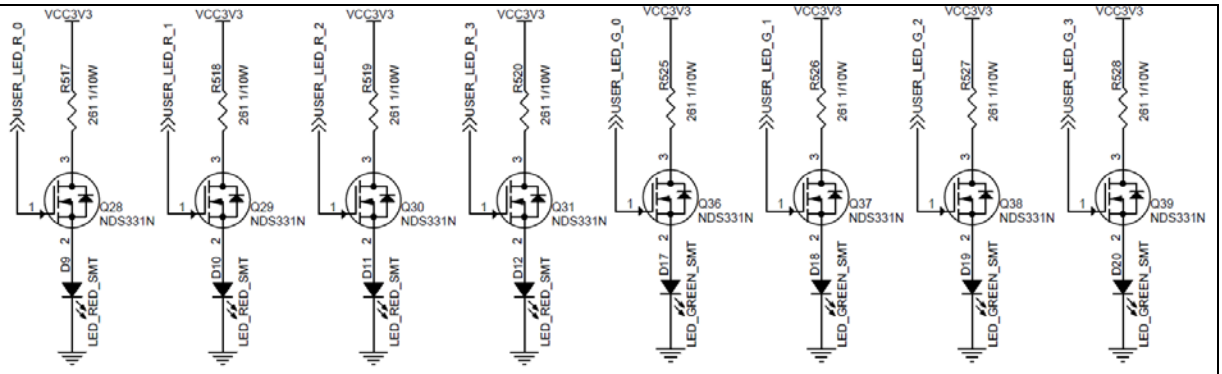


Figure 15. User LEDs schematic

Reference Designator	Net Name	Switch Type	Description
SW12	-	SLIDE	Board main power switch
SW4	FPGA_PROG_B	Push	Clear the programmable logic configuration
SW2	PS_POR_B	Push	The master reset of the entire chip. It must be held low through PS power-up
SW3	PS_SRST_B	Push	Reset all of the functional logic
SW10	PL_CPU_RESET	Push	PL CPU Reset
SW14	PUSH_SW0	Push	User Push Switch 0
SW15	PUSH_SW1	Push	User Push Switch 1
SW16	PUSH_SW2	Push	User Push Switch 2
SW17	PUSH_SW3	Push	User Push Switch 3
SW18	PUSH_SW4	Push	User Push Switch 4
SW20	SLIDE_SW0	SLIDE	User Slide Switch 0
SW20	SLIDE_SW1	SLIDE	User Slide Switch 1
SW20	SLIDE_SW2	SLIDE	User Slide Switch 2
SW20	SLIDE_SW3	SLIDE	User Slide Switch 3

Table 25. Switches

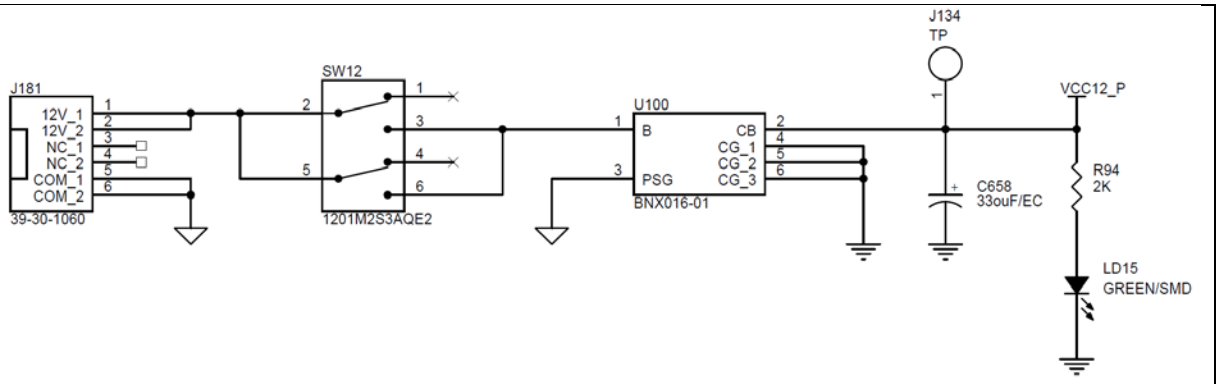


Figure 16. Board main power switch schematic

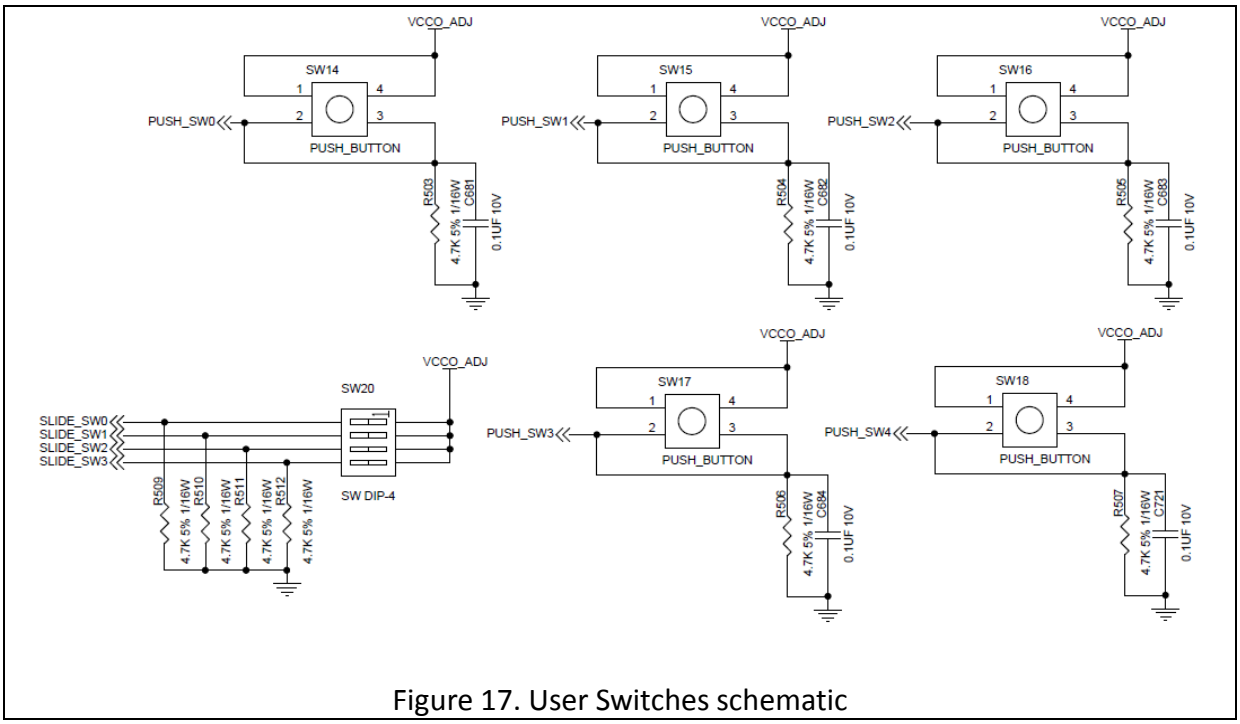


Figure 17. User Switches schematic

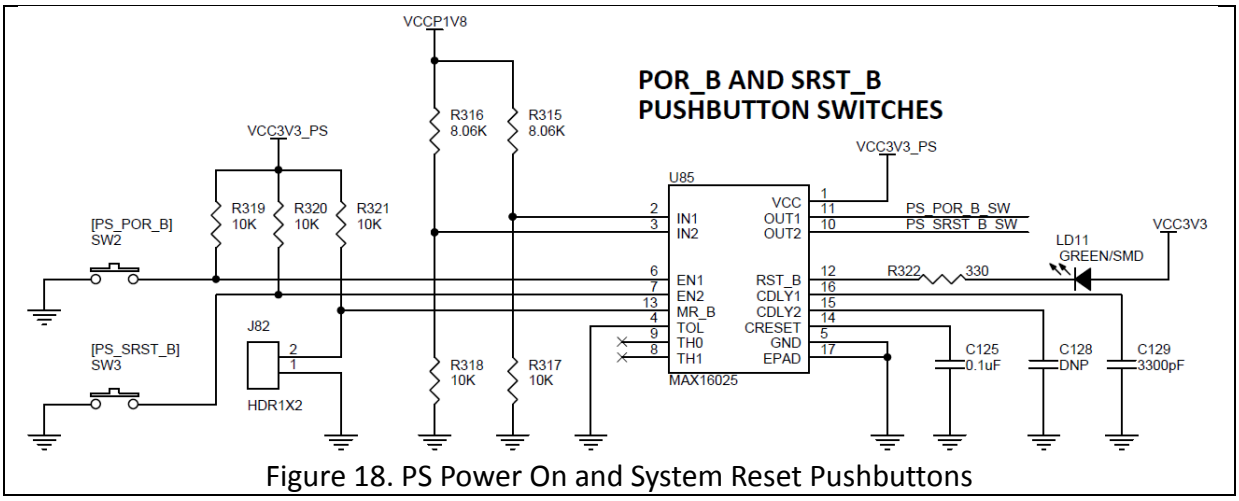


Figure 18. PS Power On and System Reset Pushbuttons

Depressing and then releasing pushbutton SW2 causes PS_POR_B_SW to strobe low.
PS_POR_B: This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B should be generated by the power supply power-good signal.

Depressing and then releasing pushbutton SW3 causes PS_SRST_B_SW (connected to the XC7Z045 AP SoC U1 dedicated PS Bank 500 pin D21) to strobe low.
PS_SRST_B: This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps.
See Zynq-7000 All Programmable SoC Technical Reference Manual (UG585) for information concerning the resets.

PCA9555BS	Net Name	Pin
I/O_2.7	IIC_PMOD0	J57.1
I/O_2.6	IIC_PMOD1	J57.3
I/O_2.5	IIC_PMOD2	J57.5
I/O_2.4	IIC_PMOD3	J57.7
I/O_2.3	IIC_PMOD4	J57.2
I/O_2.2	IIC_PMOD5	J57.4
I/O_2.1	IIC_PMOD6	J57.6
I/O_2.0	IIC_PMOD7	J57.8

Table 26. IIC PMOD header

XC7Z045 U1	Net Name	Pin
Y20	PMOD1_0_LS	J58.1
AA20	PMOD1_1_LS	J58.3
AA19	PMOD1_2_LS	J58.5
AA18	PMOD1_3_LS	J58.7
AD19	PMOD1_4_LS	J58.2
AD18	PMOD1_5_LS	J58.4
AC19	PMOD1_6_LS	J58.6
AC18	PMOD1_7_LS	J58.8

Table 27. The connection between PMOD header and FPGA

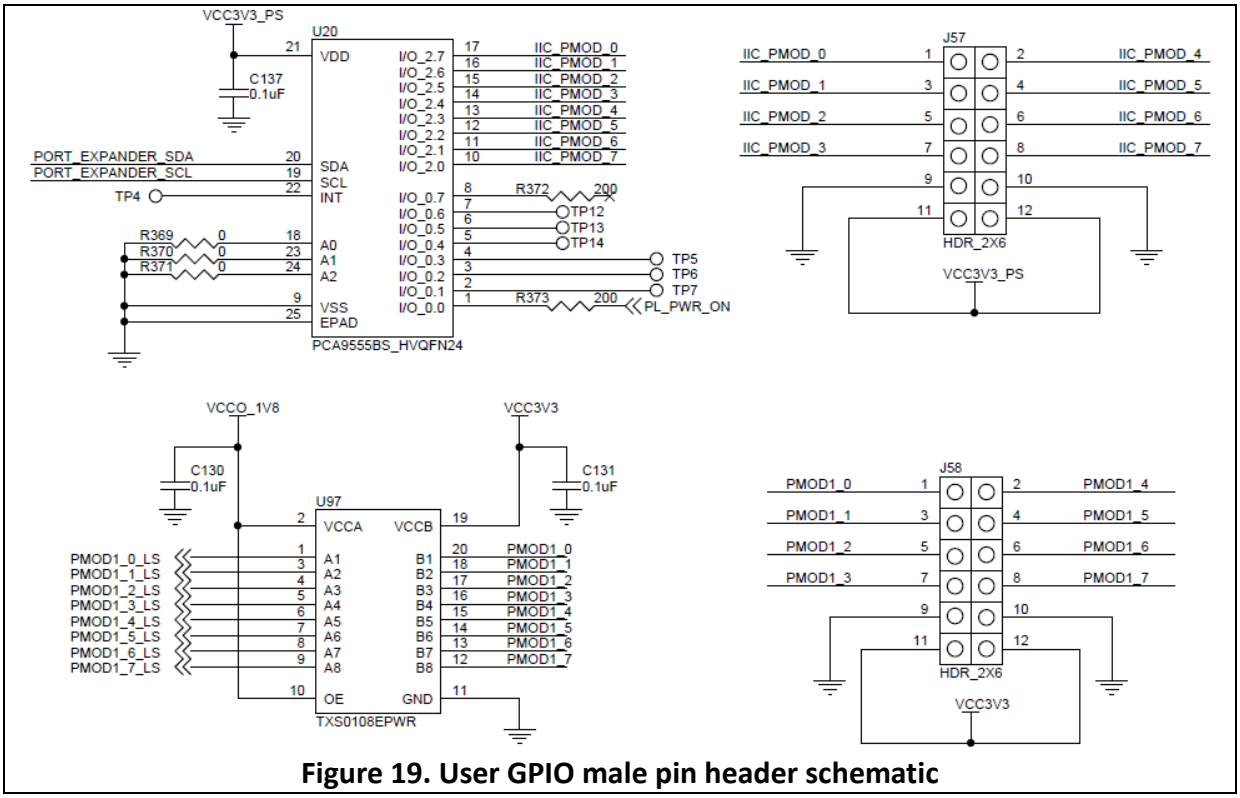


Figure 19. User GPIO male pin header schematic

Switch and jumper settings Chapter 4

The default switch and jumper settings for the Cosmos openSSD board are provided in this chapter.

4.1 Switch

Header	Function	Description
SW2	PS_POR_B	This reset is used to hold the PS in reset until all PS power supplies are at the required voltage levels. It must be held Low through PS power-up. PS_POR_B should be generated by the power supply power-good signal.
SW3	PS_SRST_B	This reset is used to force a system reset. It can be tied or pulled High, and can be High during the PS supply power ramps. See Zynq-7000 All Programmable SoC Technical Reference Manual (UG585) for information.
SW4	Program_B Pushbutton	Switch SW4 grounds the XC7Z045 AP SoC PROG_B pin when pressed. This action clears the programmable logic configuration. The FPGA_PROG_B signal is connected to XC7Z045 AP SoC U1 pin Y9. See 7 Series FPGAs Configuration User Guide for further details on configuring the 7 series FPGAs (UG470).
SW5	5-pole DIP Switch	PS Boot Mode select signals MIO[6:2]_SELECT. More detail is shown in Table 28.
SW10	Reset	PL CPU reset push button
SW12	Power switch	Main Power On/Off Slide Switch
SW[18:14]	User button	User push buttons. The connection detail is shown in Table 29.
SW20	Switch	GPIO DIP switch for general I/O The connection detail is shown in Table 30.
SW21	JTAG select	Programmable Logic JTAG Select Switch More detail is shown in Table 31.

Mode	Pin number				
	1	2	3	4	5
JTAG Boot	On	On	On	On	On
SD Boot	On	On	Off	Off	On
QSPI Boot	On	On	On	Off	On

Table 28. SW5, PS Boot Mode select signals MIO[6:2]_SELECT

Push Button	XC7Z045 Pin	Net Name
SW14	R22	PUSH_SW0
SW15	R23	PUSH_SW1
SW16	U22	PUSH_SW2
SW17	V22	PUSH_SW3
SW18	V21	PUSH_SW4

Table 29. SW[18:14]: five user push buttons

No	XC7Z045 Pin	Net Name
1	U24	SLIDE_SW0
2	V24	SLIDE_SW1
3	V23	SLIDE_SW2
4	W24	SLIDE_SW3

Table 30. SW20 : GPIO DIP Switch for general I/O

Configuration Source	DIP Switch SW21	
	Switch 1	Switch 2
None	0	0
Cable Connector J69	1	0
Digilent USB-to-JTAG interface U116	0	1
JTAG(flying lead) Header J72	1	1

Table 31 SW21 : Programmable Logic JTAG Select Switch

4.2 Jumper description

Header	Function	Description
J1	Connector	1st SODIMM connector for NAND option module
J2	Connector	2nd SODIMM connector for NAND option module
J24	Connector	RJ45 Ethernet connector, R18101DBG_LC
J22	Connector	Micro-B USB connector, USB2.0 ULPI Controller
J34	Connector	SD card connector
J57	Connector	PMOD1 Header, 2x6 0.1 in. pitch
J58	Connector	The PMOD nets connected to these headers are accessed via I²C bus expander U20 (PMOD0 J57) and level-shifter U97 (PMOD1 J58).
J84	Connector	ARM core PJTAG Header, HEADER_2.54mm_20P
J67	Connector	FAN Header
J69	Connector	2x7 2mm shrouded JTAG cable connector
J71	Connector	PM bus connector
J72	Connector	FPGA JTAG connector - JTAG flying lead header

		- 2x10 0.1 inch male header
J178	Connector	60-pin connector for current sensing
J90	Connector	General I/O expansion for debug
J177	Connector	VADJ voltage select
J85	Connector	U3 Ethernet PHY CONFIG3 pin 3 1K pull-up to 1.8V or 1K pull-down to GND Select
J86	Connector	U3 Ethernet PHY CONFIG3 pin 3 LED1 or LED0 Select
J87	Connector	Ethernet PHY CONFIG2 pin 2 tie to 1.8V or LED0 Select Header
J88	Connector	U19 Ethernet PHY CONFIG2 pin 2 1K pull-down to GND Select
J74	Connector	PS_SRST_B Select
J75	Connector	MIO Select Header MIO5
J76	Connector	MIO Select Header MIO4
J77	Connector	MIO Select Header MIO3
J78	Connector	MIO Select Header MIO2
J79	Connector	MIO Select Header MIO6
J80	Connector	PS_POR_B Select
J27	Connector	U58 USB3320 2.0 Host/OTG or Device Select
J28	Connector	RVBUS select
J29	Connector	USB_VBUS_SEL capacitor to GND Select
J30	Connector	USB 2.0 Micro-B connector J2 ID shield pins connection Select
J31	Connector	USB 2.0 Micro-B connector J2 ID pin 4 function Select
J32	Connector	U58 USB3320 2.0 RESET Header
J83	Connector	ARM PJTAG Header J64 pin 2 can be connected to VADJ
J179	Connector	PL_PWR_ON Header

Table 32. Jumper description

4.3 Jumper setting

4.3.3 Default jumper setting

Jumper	Function	Default	Selects
J85	U3 Ethernet PHY CONFIG3 pin 3 1K pull-up to 1.8V or 1K pull-down to GND Select	1-2	CONFIG3 = 1 (p/u to 1.8V)
J86	U3 Ethernet PHY CONFIG3 pin 3 LED1 or LED0 Select	OPEN	J44 sets CONFIG3 condition
J87	Ethernet PHY CONFIG2 pin 2 tie to 1.8V or LED0 Select Header	OPEN	J45 sets CONFIG2 condition
J88	U19 Ethernet PHY CONFIG2 pin 2 1K pull-down	1-2	CONFIG2 = 0 (p/d to

	to GND Select		GND)
J74	PS_SRST_B Select	1-2	Sourced by U85 POR MAX16025
J75	MIO Select Header MIO5 (Note: DIP SW11 pole 1 affects this signal)	1-2	QSPI0_IO3 = MIO5_SELECT
J76	MIO Select Header MIO4 (Note: DIP SW11 pole 2 affects this signal)	1-2	QSPI0_IO2 = MIO4_SELECT
J77	MIO Select Header MIO3 (Note: DIP SW11 pole 5 affects this signal)	1-2	QSPI0_IO1 = MIO3_SELECT
J78	MIO Select Header MIO2 (Note: DIP SW11 pole 3 affects this signal)	1-2	QSPI0_IO0 = MIO2_SELECT
J79	MIO Select Header MIO6 (Note: DIP SW11 pole 4 affects this signal)	1-2	QSPI0_CLK = MIO6_SELECT
J80	PS_POR_B Select	1-2	Sourced by U85 POR MAX16025
J27	U58 USB3320 2.0 Host/OTG or Device Select	1-2	HOST sources VBUS power
J28	RVBUS select	1-2	Position 1–2 = Device mode (10 KΩ) Position 2–3 = Host or OTG mode (1 KΩ)
J29	USB_VBUS_SEL capacitor to GND Select	2-3	120uF to GND
J30	USB 2.0 Micro-B connector J2 ID shield pins connection Select	1-2	J2 shield pins to GND
J31	USB 2.0 Micro-B connector J2 ID pin 4 function Select	1-2	Function = USB ID
J32	U58 USB3320 2.0 RESET Header	OPEN	U58 not held in RESET
J83	ARM PJTAG Header J64 pin 2 can be connected to VADJ	1-2	OPEN J64.2 not conn. To VADJ
J179	PL_PWR_ON Header	OPEN	PL power enabled

Table 33 Default jumper setting

PCA9555BS(U4) PORT: Pin	Net Name	Pin
I/O_2_7:17	IIC_PMOD_0	J57.1
I/O_2_6:16	IIC_PMOD_1	J57.3
I/O_2_5:15	IIC_PMOD_2	J57.5
I/O_2_4:14	IIC_PMOD_3	J57.7
I/O_2_3:13	IIC_PMOD_4	J57.2
I/O_2_2:12	IIC_PMOD_5	J57.4
I/O_2_1:11	IIC_PMOD_6	J57.6
I/O_2_0:10	IIC_PMOD_7	J57.8

Table 34. IIC PMOD header

XC7Z045 AP SoC	Net Name	Pin
Y20	PMOD1_0	J58.1
AA20	PMOD1_1	J58.3
AA19	PMOD1_2	J58.5
AA18	PMOD1_3	J58.7
AD19	PMOD1_4	J58.2
AD18	PMOD1_5	J58.4
AC19	PMOD1_6	J58.6
AC18	PMOD1_7	J58.8

Table 35. PMOD Header connections to XC7Z045 AP SoC

Pin number	XC7Z045 Pin	Pin number	XC7Z045 Pin
1	AJ13	2	AG15
3	AJ16	4	AF18
5	AJ15	6	AF17
7	AK16	8	AE16
9	AK15	10	AE15
11	AH17	12	AE18
13	AH16	14	AE17
15	AE12	16	AD16
17	AF12	18	AD15
19	AH14	20	AC14
21	AH13	22	AC13
23	AD14	24	AA15
25	AD13	26	AA14
27	AE13	28	AB12
29	AF13	30	AC12
31	AF15	32	AB15
33	GND	34	GND

Table 36. J90, General I/O Expansion for DEBUG

Header	Function	Shunt Position
J177	VCC_NAND_IO voltage select	Position 1–2 = 3.3 V Position 3–4 = 2.5 V Position 5–6 = 1.8V (initial value) Position 7–8 = 1.5V

Table 37. VADJ voltage select