PCIe® Cable Update

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Disclaimer:

Some of the information in this presentation refers to specifications still in the development process. This presentation reflects the current thinking of various PCI-SIG® workgroups, but all material is subject to change before the specifications are released.

Agenda:

- **ECNs & Errata Completed Against OCuLink 1.0:**
  - Pin Sequencing Errata
  - Memory Map Errata
  - Server Space ECN
  - Skew ECN
  - CPRSNT# ECN
  - BP Type ECN
  - Wiring Chart ECN
  - Performance Table ECN
  - Cable SI ECN
- **Open Items:**
  - Port & Cable Aggregation ECR
  - Power Appendices ECR
  - X4 Drawing Corrections ECR
  - 16.0 GT/s Performance ECR

ECNs & Errata Completed Against OCuLink 1.0

- **Pin Sequencing Errata:**
  - Contains one pin sequencing erratum against PCIe® OCuLink 1.0, correcting a single entry in a table showing the pin sequencing for a ground pin as second mate
  - Completed: 11/04/2016
- **Memory Map Errata:**
  - Modifies the cable assembly memory map; reorganizes bytes for external cable assemblies and modifies fields as needed to align with SFF-8636
  - Impact: Existing external OCuLink cables and ports must be modified to accept the new memory map
  - Completed: 12/13/2016

ECNs & Errata Completed Against OCuLink 1.0

- **Server Space ECN:**
  - Adds environmental requirements for enterprise applications to *OCuLink 1.0* specification:
    - 5 year field life
    - 65°C operating temperature
      (May be modified in the future to accommodate active cables)
  - Impact: Environmental & mechanical requirements for OCuLink connectors and cables are identified for use in enterprise applications
  - Completed: 12/13/2016

ECNs & Errata Completed Against OCuLink 1.0

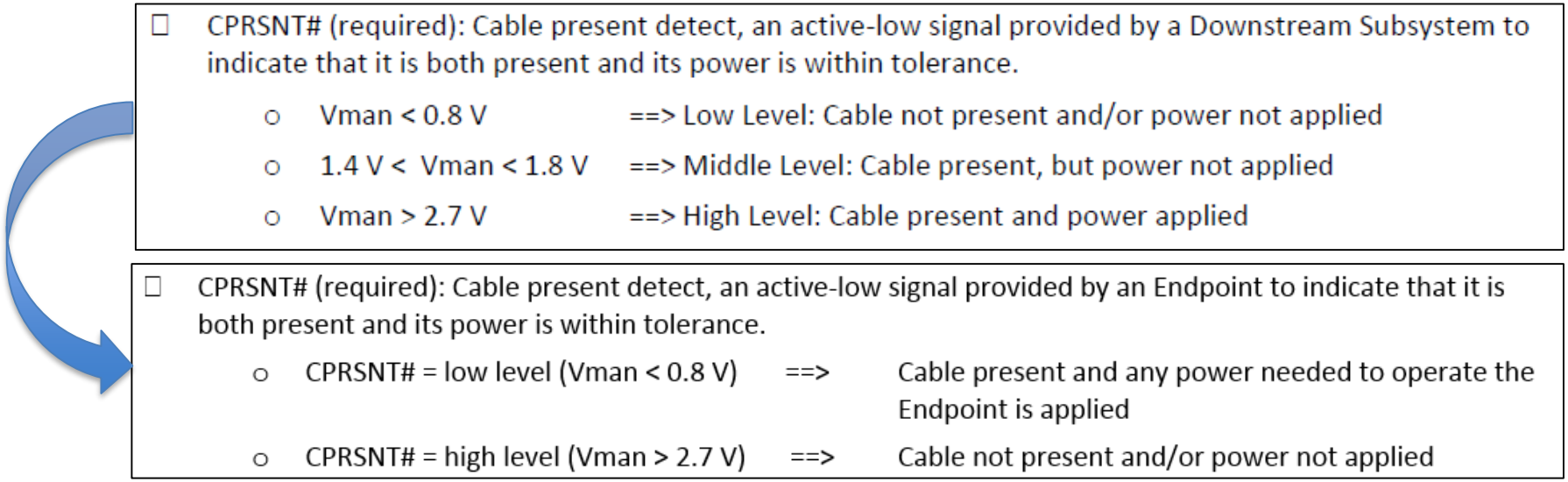
- **Skew ECN:**
  - Corrects maximum skew permitted in OCuLink cables to coincide with requirements in *CEM* specification
  - Impact: (Minimal) Manufacture of compliant cable assemblies may be more challenging
  - Completed: 12/13/2016

Table 7-1. Cable Assembly Differential Characteristics Summary

Description	Reference	Value	Unit
Maximum insertion loss	7.3.2	15	dB
Minimum insertion loss	7.3.2	0	dB
Minimum return loss	7.3.3	Equation (7-5)	dB
Differential to common-mode return loss	7.3.4	Equation (7-6)	dB
Differential to common-mode conversion loss minus Insertion Loss	7.3.5	Equation (7-7)	dB
Common-mode to common-mode return loss	7.3.6	Equation (7-8)	dB
MDNEXT loss	7.3.7	Equation (7-9)	dB
MDFEXT loss	7.3.7	Equation (7-10)	dB
OCuLink Total Cable Assembly Skew (Sc)	7.3.8	~~6~~0.9 (max)	ns ~~MAX~~

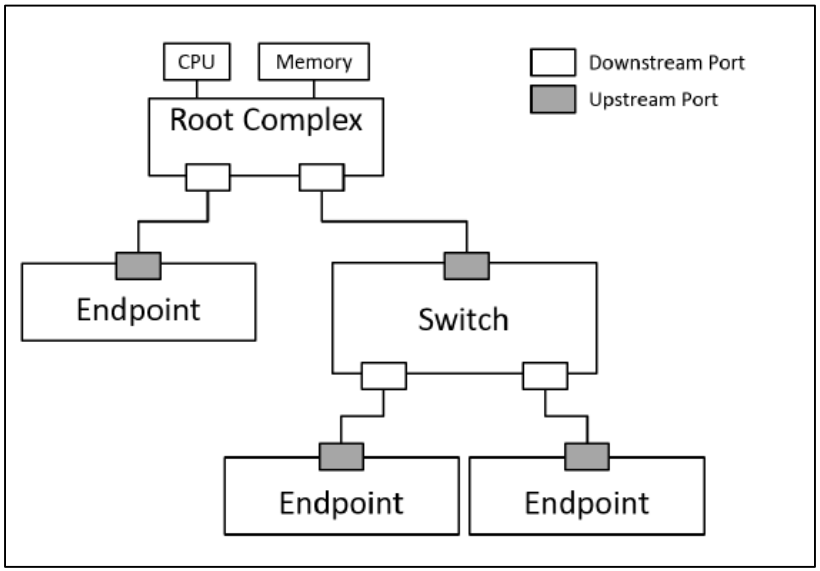
ECNs & Errata Completed Against OCuLink 1.0

- **CPRSNT# ECN:**
  - Fully defines the cable presence (CPRNST#) signal that was incompletely and inaccurately defined in *OCuLink 1.0*
  - Impact: CPRNST# supported 3 states in *OCuLink 1.0*; it now only supports 2 states
  - Completed: 5/31/2017



ECNs & Errata Completed Against OCuLink 1.0

- **BP Type ECN:**
  - Fully defines the Backplane (BP) Type signal that was incompletely defined in the *OCuLink 1.0* release
  - Added figure below to clarify Upstream Port/ Downstream Port
  - Impact: BP Type pin may be used for VSP after BP Type is established
  - Completed: 10/6/2017



ECNs & Errata Completed Against OCuLink 1.0

- **Wiring Chart ECR:**
  - Connector and cable assembly pinout tables have been revised to show complete pinout assignments for all applications
  - Impact: Decreases errors misinterpreting wiring diagrams
  - Completed: 10/6/2017

Table 6-9. Wiring Chart for x4 Internal Passive and Active Crossover Cables

P1 Row Position	Downstream Port	Cable Termination & Signal Direction	Upstream Port	P2 Row Position
A1 (Bevel)	POWER 3.3 Vact #1 (see Note 1)	NO WIRE	POWER 5V #1 (see Note 5)	B1
A2	GROUND	———	GROUND	B2
A3	PERp0	←	PETp0	B3
A4	PERn0	←	PETn0	B4
A5	GROUND	———	GROUND	B5
A6	PERp1	←	PETp1	B6
A7	PERn1	←	PETn1	B7
A8	GROUND	———	GROUND	B8

ECNs & Errata Completed Against OCuLink 1.0

- **Performance Table ECN:**
  - Reorganizes and clarifies mechanical and environmental performance criteria required of OCuLink connectors and cables
  - Impact: Test requirements adhere to EIA test methodology
  - Completed: 3/15/2018

Table 6-12. EIA-364-1000A Test Sequences for Test Groups 1, 2, 3, 4 and 7

Test (see Note 1)	Test Group 1	2	3	4	7
Low Level Contact Resistance	1, 4, 6	1, 4, 6, 8	1, 4, 6	1, 4, 6, 8, 10	2, 4
Durability (preconditioning)	2	2	2	2	
Temperature Life	3				
Reseating	5	7		9	
Thermal Shock		3			
Cyclic Temperature and Humidity		5			
Temperature Life (preconditioning)			3		
Vibration			5		
Mixed Flowing Gas					
Thermal Cycling (disturbance)					
Dielectric Withstanding Voltage					
Durability					

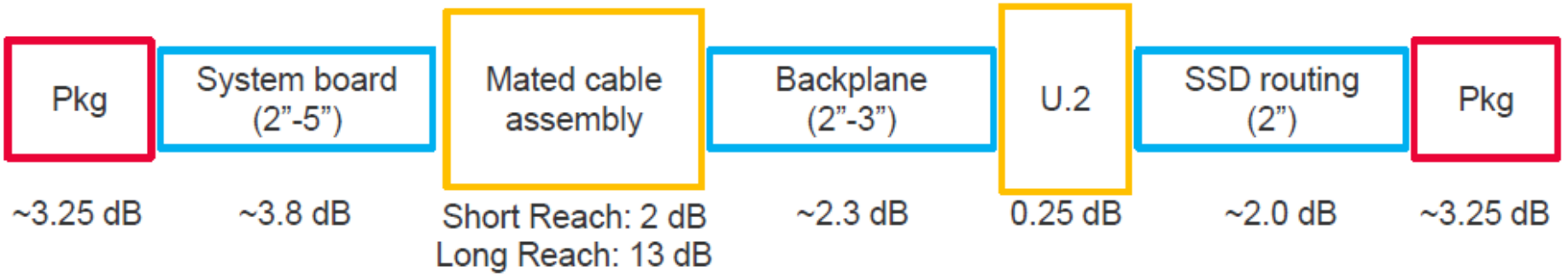
Notes:
1. Intermediate LLCR measurements may be taken during any test sequ tester, but are not required.

Table 6-13. EIA-364-1000A Test Details

Test	Test Procedure	Test Criteria
Durability (preconditioned)	See Note 1	No intermediate requirements during *EIA-364-1000A* testing
Durability	Cycle rate: 200 cycles/ hour (see Notes 1 & 2)	
Mixed Flowing Gas	Class IIA (see Note 3)	
Temperature Life	See Note 4	
Cyclic Temperature and Humidity		

ECNs & Errata Completed Against OCuLink 1.0

- **Cable SI ECN:**
  - Clarifies SI requirements
  - Existing limits were validated using an internal reference topology (most common application) & Seasim
  - This ECR will act as the starting point for defining 16 GT/s requirements (first priority for 2.0 release)
  - Impact: IL limit justifiably accommodates 2m cables
  - Completed: 4/13/2018



Open Items:

- **Port & Cable Aggregation ECR:**
  - Addresses sideband management for aggregated ports/ cables
  - Additions made to the memory map to address issues
  - Impact: Additional entries are needed in the memory map of cables that are to be aggregated
  - Expected to be completed: Q2 2018 (in 60-day review)
- **Power Appendices ECR:**
  - General clean up/ reorganization of power appendices (C & E)
  - Workgroup currently addressing comments received
  - Impact: User is pointed to SFF-8449 for power requirements
  - Expected to be completed: Q2 2018 (in 60-day review)

Open Items (Continued):

- **x4 Figure clean-up ECR:**
  - Replaced drawings showing SMT hold-downs with drawings showing through-hole hold downs to reflect the industry's preference
  - Corrects dimensions and tolerances based on industry feedback
  - Impact: Accurate and concise representation of x4 form factor
  - Expected to be completed: Q3 2018
- **16.0 GT/s Performance ECR**
  - Adds signal integrity performance requirements necessary to allow OCuLink cables to meet PCIe-4.0 system requirements
  - Impact: OCuLink cables may be used in PCIe-4.0 systems
  - Expected to be completed: Q4 2018

PCIe Cable Update

Lee Mohrmann

External Cabling WG Chair

National Instruments

Quick Overview

- **New Connector- based on SFF-8644**
- **Independent Clocking**
- **New Sideband Implementation**
  - Includes provision for Vendor Specific Communications via 2-wire interface
- **Configuration of PCIe device required before Link Training begins**
- **Port Flexibility**
- **Cable Flexibility**

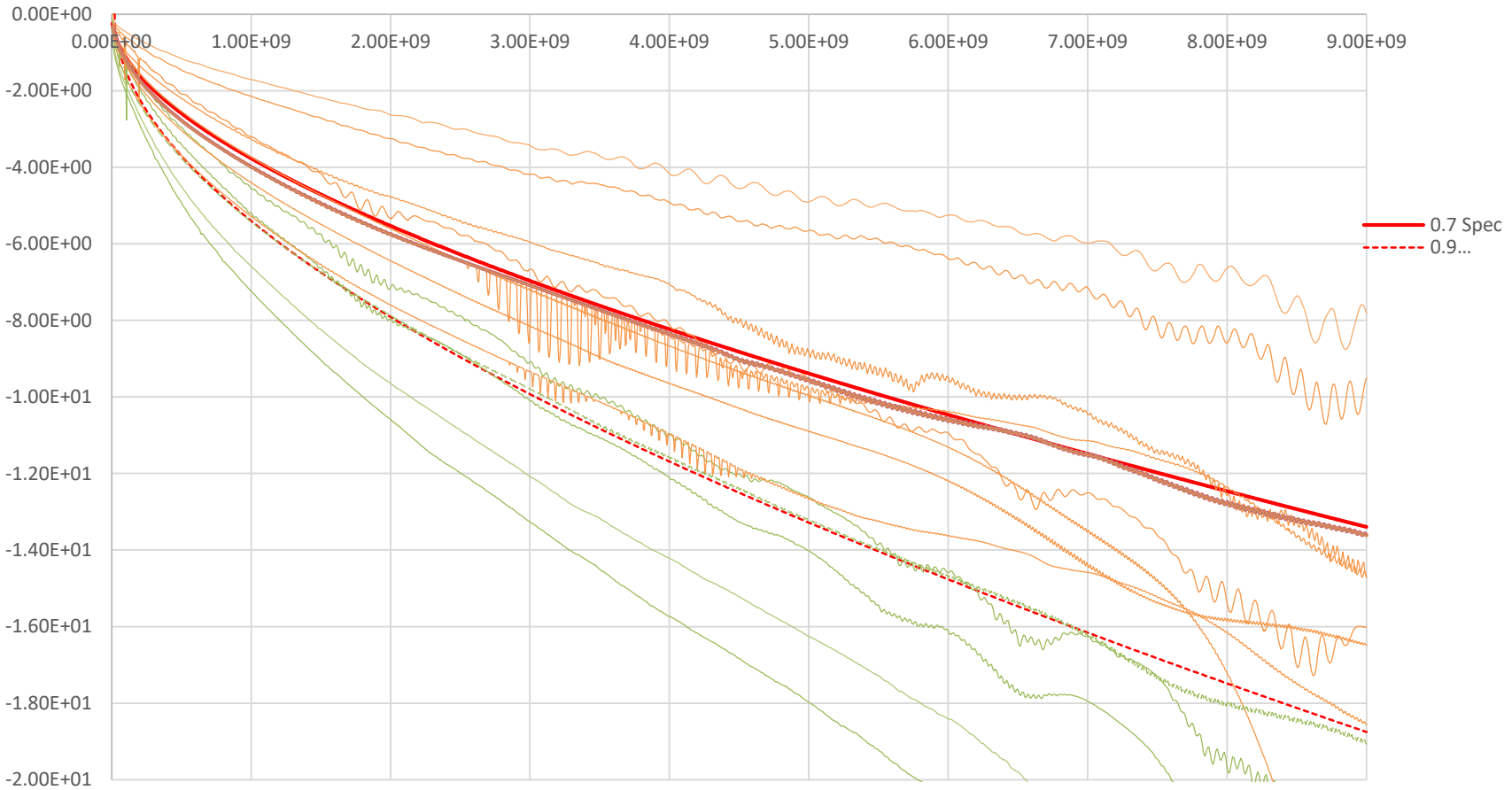
PCIe vs. SFF-8644

- **Pinout**
  - PCIe cables facilitates a x4 routing solution
  - SAS cables route 4 independent x1 links
- **Sidebands**
  - PCIe supports End-to-End 2-wire interface, SFF-8449 supports interface to cable assembly plug only
  - SFF-8449 Rsvd pin used for CADDR in PCIe cables, allows for address modification of 2-wire devices
- **Memory Map**
  - 2 locations reserved in SFF-8639 specifically for PCIe cables
  - Definitions change for some fields, though they are similar information

Cable Performance Updates

- **The WG has been finalizing cable performance parameters for:**
  - Insertion Loss
  - Return Loss
  - Crosstalk Limits

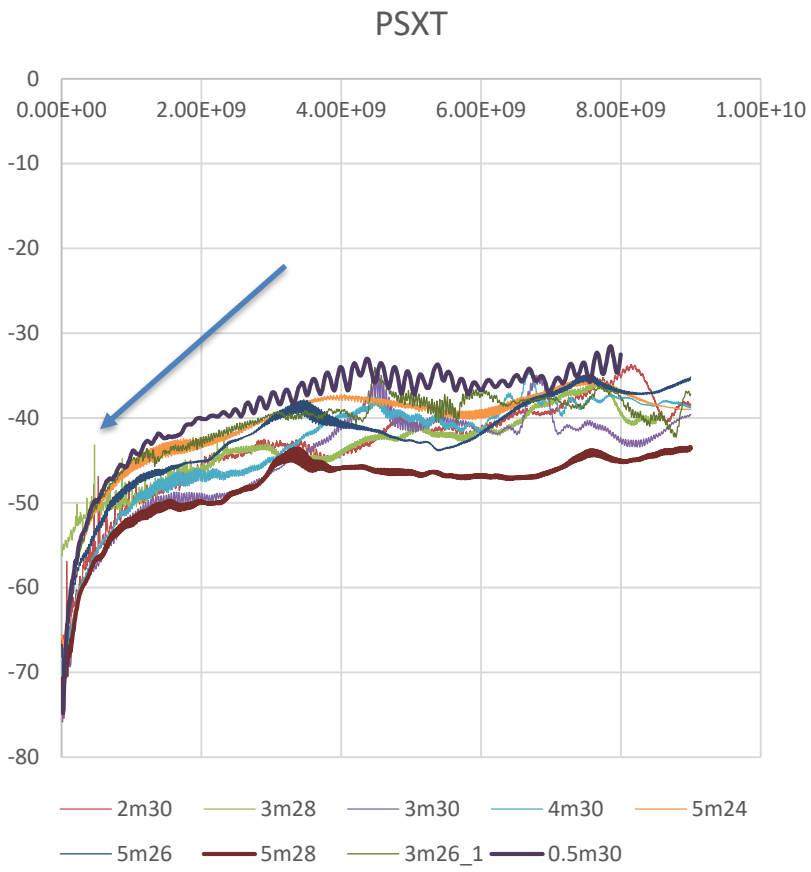
Insertion Loss (Update colors)



Crosstalk

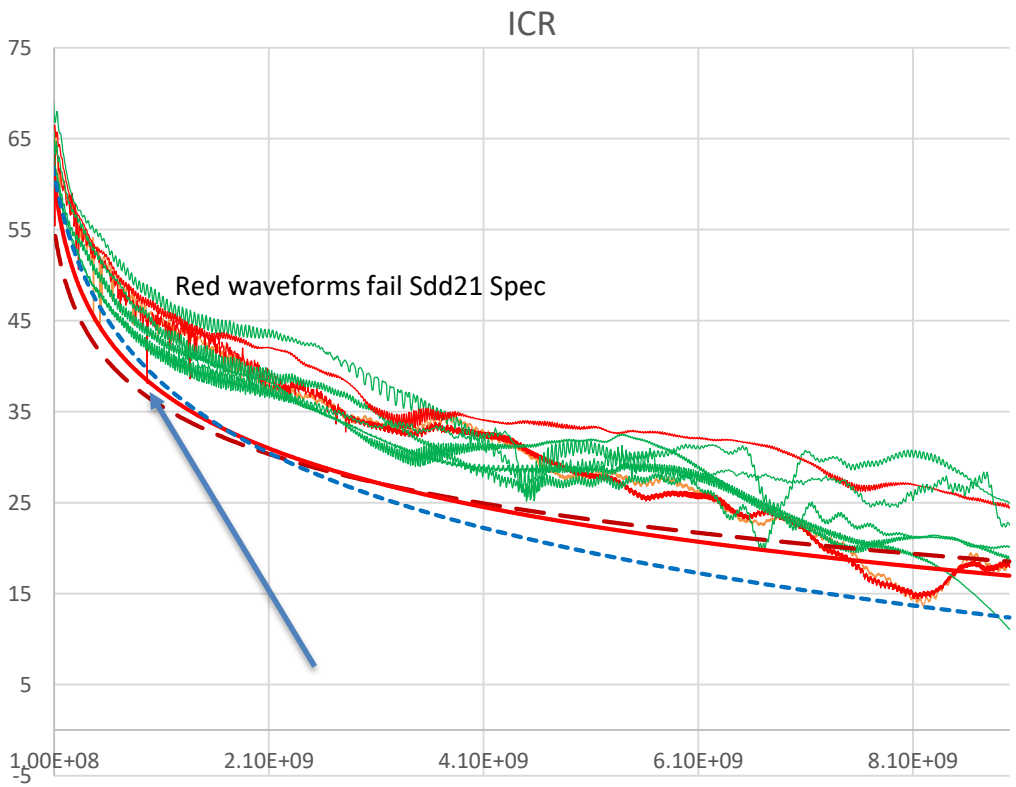
- **MDNEXT**
  - Sum of all Near-End Crosstalk Members
- **MDELFEXT**
  - Sum of all Far-End Crosstalk Members-Insertion Loss
- **MDELFEXT can scale for insertion loss, but MDNEXT does not**

PSXT



- **PowerSum Crosstalk**
  - Combines NEXT & FEXT
- **Does not scale with Insertion Loss**
- **Questions arise about Pass/Fail limits vs functionality based on singular “spike”**

ICR



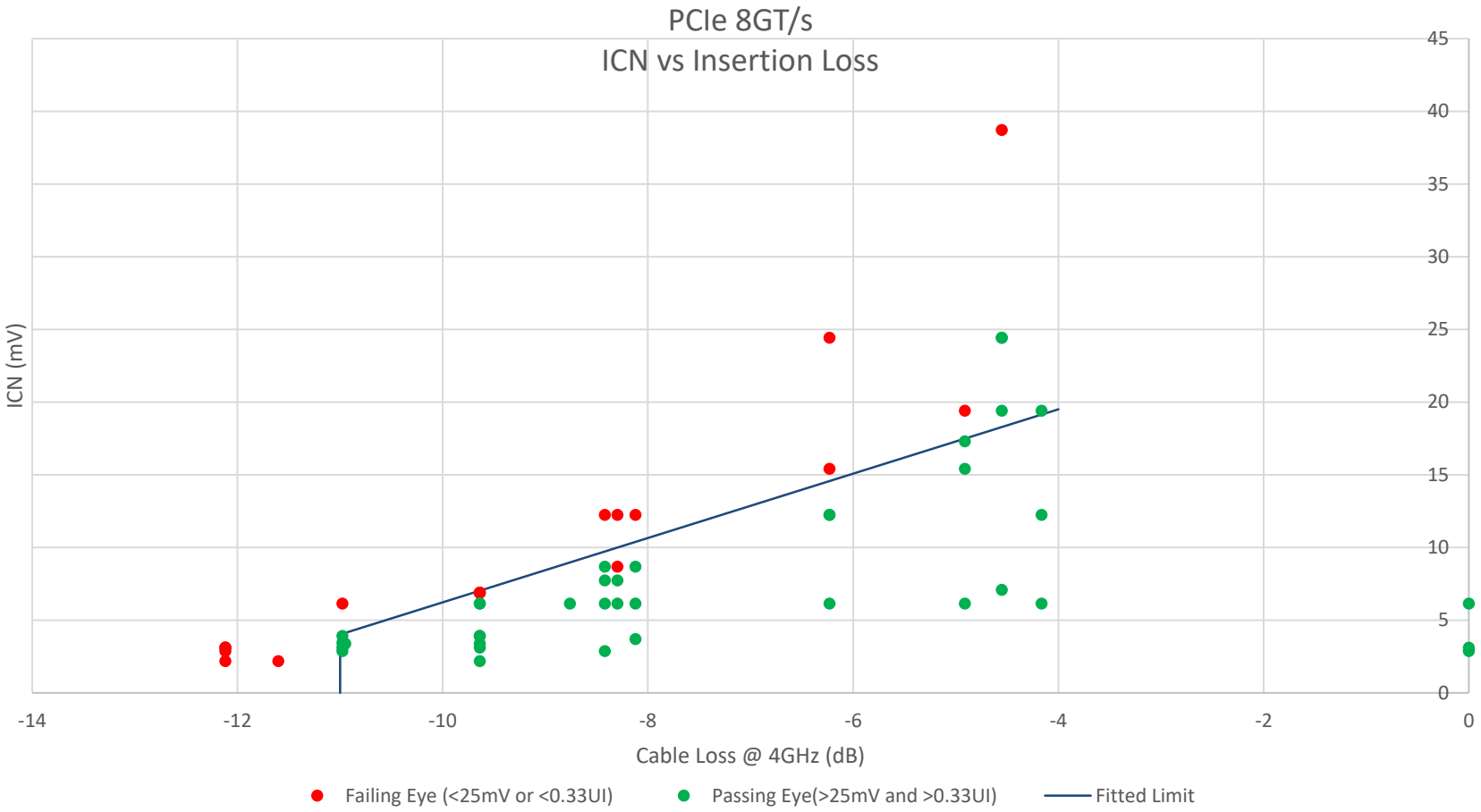
- **Insertion Crosstalk Ratio**
  - ICR = (PSXT – Insertion Loss)
- **Scales with Crosstalk**
- **Still requires separate Pass/Fail limit for Insertion loss**
- **Susceptible to spikes & excursions in frequency curves**

ICN

- **Integrated Crosstalk Noise**
  - Use cable assembly PSNEXT and PSFEXT
  - Create signal filters based on signal characteristics
    - Filters create the weighting function
  - Combine the weighting function with crosstalk curves
  - PowerSum the NEXT and FEXT combinations

  - The frequency-domain weighting functions are based on Baud Rate, aggressor amplitude, aggressor edge rate, and receiver bandwidth
  - Does not scale with Insertion Loss
    - Must create curve of ICN vs Insertion loss
  - Used by other organizations for similar speed interfaces

ICN (need to update)



Status (need to update)

- **We have updated the aforementioned curves**
- **Awaiting to approval 0.9 draft**
- **Please review the specification when it becomes available!**

Looking Ahead

- **Preliminary PCIe 4.0 simulations indicate passive 1m cables will work.**
  - This included PCIe 4.0 Pkgs provided by the Fixed-Side models used in PCIe 3.0 specification
  - Longer cables will need to be updated with better cable terminations
  - Approximate loss at 8 GHz is -9 dB, subject to change

- **Architectural changes needed**
  - Update the cable memory map to include PCIe 4.0 identifier
  - Optionally update CMI to 400kHz operation for quicker cable configuration reads and sideband messaging operations

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