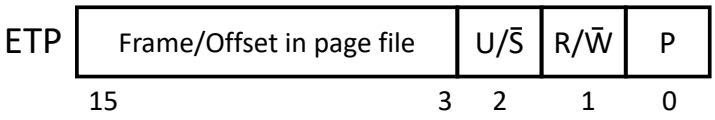
General instructions

Answers must be written in the boxes after each question. Each wrong, illegible or blank answer does not increase or decrease the final mark. In the case of theoretical questions, the capacity for synthesis will be assessed. The score for each question is indicated in parentheses.

❑ **1**. A computer with virtual memory using paging has the following features: 24-bit virtual addresses, 24-bit physical addresses, memory pages of 2 KiB and byte addressing. This computer uses a single level of translation and the structure of its page table entries is as follows:



The presence bit is represented by P. Code pages have the bit R/$\overline{\text{W}}$ set to 1 and data pages set to 0. User privilege pages have the bit U/$\overline{\text{S}}$ set to 1 and operating system pages set to 0.

The MMU has a TLB with 12 entries, shown in the following figure and divided into 3 columns for formatting convenience. Note that the TLB only refers to pages that are in memory or in disk.

	V	Task	VirPag	PTE
0	0	7Fh	09C0h	B23Ah
1	1	21h	1000h	253Bh
2	1	00h	1F2Ah	23B1h
3	1	10h	15F3h	1A35h

	V	Task	VirPag	PTE
4	1	10h	15B1h	643Dh
5	0	07h	1398h	01F7h
6	1	21h	0E62h	12A5h
7	1	04h	0F1Ch	1A35h

	V	Task	VirPag	PTE
8	1	04h	13B7h	21AFh
9	1	00h	1F31h	4523h
A	1	10h	012Bh	8127h
B	1	04h	01E3h	23FCh

Each TLB entry contains a valid bit, `V`, an 8-bit task identifier, `Task`, a virtual page number, `VirPag`, and the page table entry, `PTE`, associated with the virtual page. A task identifier set to zero indicates that the TLB entry is valid for all tasks. The LRU bits associated with each TLB entry are not shown, as they are not needed for solving this problem.

— **(1 point)** What is the physical address associated with virtual address 7312A7h for the tasks with identifiers 21h and 2Ah? Express the result in hexadecimal. If the physical address cannot be known from the TLB information, you must answer `TLB fault`.

Task 21h: 12A2A7h Task 2A: TLB fault

— **(1 point)** If all running tasks have at least one valid entry in the TLB, what is the total size in bytes occupied by the page tables of all running tasks?

Size in bytes: 48 KiB

— **(1,5 points)** From the information displayed in the TLB, identify a memory frame shared by two tasks, indicating the associated physical address range in hexadecimal, as well as the task identifier and virtual page of each task, also in hexadecimal.

Range: 1A3000h 1A37FFh Task ID / Page: 10h, 15F3h Task ID / Page: 04h, 0F1Ch

— **(1 point)** Indicate a task and a virtual address of this task whose access provokes a recoverable page fault. Express the result in hexadecimal.

Task ID: 04h Virtual address: Any in the range 0F1800h 0F1FFFh

— **(1 point)** At least one of the TLB entries is known to correspond to an operating system code page. Indicate in hexadecimal the range of physical addresses of the page.

Range: 452000h 4527FFh

— **(1 point)** The computer uses a L1 separated cache, consisting of an 8 KiB for data and a 16 KiB for code. Both caches use physical tagging and virtual indexing to solve the synonym problem. What is the minimum possible number of ways for each cache?

L1 data cache: 8Ki/2Ki = 4 L1 code cache: 16Ki/2Ki = 8

❏ **2**. **(1 point)** A disk interface uses DMA for its I/O operations. The interface transfers 512-byte blocks to memory and each time a block is transferred, the interface requests an interrupt. The interrupt service routine consumes 100 clock cycles in a 2 GHz CPU. It is also known that the disk interface at its maximum transfer speed is capable of reading 200 MBytes/s. What is the percentage of the CPU time consumed by the interface at that maximum speed? Answer with two decimal digits indicating the expression used to calculate the result. (Assume 1 M = 10^6).

(200000000/512)*100/2000000000*100 % = 1.95 %

❏ **3**. Modern graphical interfaces, such as HDMI and DisplayPort, use multiple TMDS channels for video transmission between a computer and its monitor. Each TMDS channel is unidirectional and they are all synchronized using a common clock signal. In each clock cycle, 10 bits are transferred using 8b/10b encoding.

— **(0.5 points)** To watch a high quality 4K video, a monitor with a resolution of 4096×2160 pixels with a refresh rate of 60 Hz is used. Considering that 24 bits are generally used to represent a pixel in high quality videos, what is the maximum bandwidth supported by the monitor? Answer in MBytes/s with two decimal digits indicating the expression used to calculate the result. (Assume 1 M = 10^6).

$4096 \times 2160 \times 3 \times 60 = 1592.52$ MB/s

— **(1 point)** For the interconnection between the computer and the monitor, the **HDMI 2.0** interface is used. This interface employs three TMDS channels for video transmission and uses a standard connector with a clock frequency of 600 MHz. Would it be possible to use this interface to transmit high quality video with the maximum bandwidth supported by the monitor? Indicate the expression used to justify your answer.

Si $600 \times 3 \times 10/8 \times 8/10 = 1800$ MB/s ≥ 1592.52 MB/s

— **(1 punto)** To connect the above HDMI 2.0 interface to the computer, the **PCI Express 5.0** interface is proposed to use. This interface is characterized by transferring 1 bit for reading and 1 bit for writing in each channel per clock cycle at a frequency of 32 GHz. In addition, it uses an 128b/130b encoding. How many channels should be used to transmit high quality video with the maximum bandwidth supported by the monitor? Indicate the expression used to calculate the result.

$1592.52/(32000 \times 1/8 \times 128/130) = 0.40$ >1 canal