Time										1 us
ent_b										
saida										
car_in										
car_out										
ent_a										
ent_b										
saida										
saida[15:0]	0000			0005	0000	0010		0000		
zero										
ulaenta_s[15:0]	0000			0005	0000	0010		0000		
ulaentb_s[15:0]	0000									
ulaop_s[1:0]	00									
ulaout[15:0]	0000			0005	0000	0010		0000		
ulaout_s[15:0]	0000			0005	0000	0010		0000		
reg1_data[15:0]	uuuu		C305		C410			4800		
reg2_data[15:0]	0000			0005	0000	0010		0000		
rst										
state[1:0]	00		01	10	00	01	10	00	01	10
ulaout[15:0]	0000									