Introduction to the course of

Computer architecture, RISC-V and vector computing

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Agenda

Master in HPC, ICTP - Trieste (3-7 Feb 2025)

Start	End	Mon 3	Tue 4	Wed 5	Thu 6	Fri 7
9:00	9:15	Introduction (F. Mantovani)	Data Level Parallelism (P. Vizcaino)	EPI, EPAC and SDV (F. Mantovani)	Thread Level Parallelism (F. Banchelli)	Presentation #1
9:15	9:30	Computer Architecture 101: ISAs and pipelines (F. Banchelli)				
9:30	9:45					Presentation #2
9:45	10:00					
10:00	10:15	Break	Break	Break	Break	Presentation #3
10:15	10:30	Instruction Level Parallelism (F. Banchelli)	The RISC-V ISA (F. Mantovani)	Use cases: Alya, SeisSol, and MiniFALL3D (F. Mantovani)	Distributed Memory (F. Banchelli)	
10:30	10:45					Presentation #4
10:45	11:00					
11:00	11:15	Break	Break	Break	Break	Presentation #5
11:15	11:30	Memory Hierarchy (P. Vizcaino)	RISC-V "V" Extension and Long Vector Architectures (F. Mantovani)	Performance analysis tools for RISC-V (F. Mantovani)	HPC System Architecture (F. Mantovani)	
11:30	11:45					Presentation #6
11:45	12:00					
12:00	12:15	Lunch break	Lunch break	Lunch break	Lunch break	Presentation #7
12:15	12:30					
12:30	12:45					Presentation #8
12:45	13:00					
13:00	13:15	Lab #0: HCA Infrastructure (F. Banchelli, P. Vizcaino, F. Mantovani)	Lab #2a: Tools for rvv (F. Banchelli, P. Vizcaino, F. Mantovani)	Lab #3: Visualizing RAVE traces (P. Vizcaino)	Lab #4: Visualizing OpenMP and MPI traces (F. Banchelli)	Presentation #9
13:15	13:30					
13:30	13:45					
13:45	14:00	Break	Break	Break	Break	
14:00	14:15	Lab #1: Measuring single-core performance (F. Banchelli, P. Vizcaino, F. Mantovani)	Lab #2b: Vectorization techniques with RAVE and Compiler Explorer (F. Banchelli, P. Vizcaino, F. Mantovani)	Task #1: Vectorizing a scientific code (F. Banchelli, P. Vizcaino, F. Mantovani)	Task #2: Leveraging tracing tools to gain micro-architectural insight (F. Banchelli, P. Vizcaino, F. Mantovani)	
14:15	14:30					
14:30	14:45					
14:45	15:00					
15:00	15:15					
15:15	15:30					
15:30	15:45					

Why are you here?

…and not paying 20$ for the monthly subscription to ChatGPT

(or even less for DeepSeek)

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Added values of being here:

1. **Share the experience of/with other people**
2. **Hands-on session (aka learn from errors!)**
3. **VIP pass to 'special' HPC systems**

Speakers, Prototypes and Technology Readiness Level

Let's get to know each other

Barcelona Supercomputing Center

60% Spanish Government, 30% Catalan Government, 10% University Politécnica de Catalunya

Barcelona Supercomputing Center

- Supercomputing Services
- Reasearch
- Higher Education

Computer Science	Earth Science	Life Science	CASE	Operations	Administration

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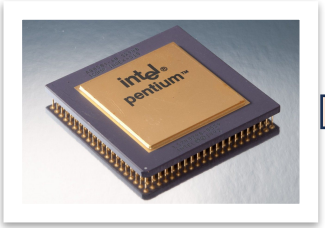
Mobile and Embedded Based HPC lab

Mobile and Embedded based HPC lab

HPC systems are historically “recycling” ideas and technologies from larger markets

1990 2000 2010 2020



Microprocessor CPUs

Graphic Processing Units (GPU)

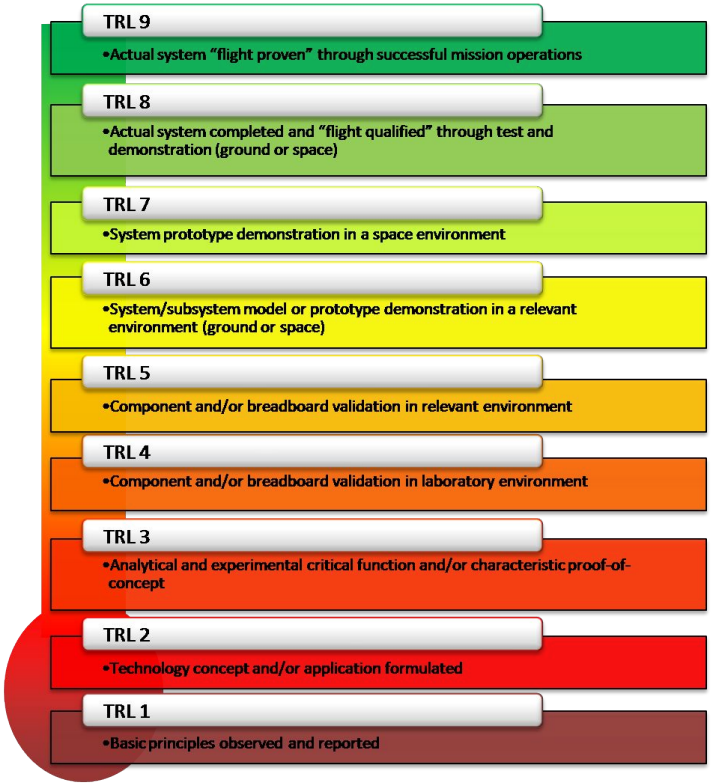
Mobile and tablet system on chips

What’s next?

Mobile and Embedded based HPC lab

Install and operate prototypes

- Based on “emerging technologies”
  - 2012 – 2019 Arm based
  - 2018 – present RISC-V based
- With mid-low Technology Readiness Level (in High Performance Computing)



Mobile and Embedded based HPC lab

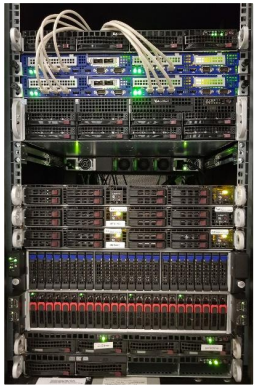
- Current systems
  - Based on unconventional architectures
    - ARM, RISC-V
  - Implemented on commercial platforms
  - Implemented on FPGAs
  - Handled as HPC compute nodes

📝 Mantovani, F., Garcia-Gasulla, M., Gracia, J., Stafford, E., Banchelli, F., Josep-Fabrego, M., Criado-Ledesma, J. and Nachtmann, M., 2020. **Performance and energy consumption of HPC workloads on a cluster based on Arm ThunderX2 CPU**. Future generation computer systems, 112, pp.800-818.

📝 Banchelli, F., Peiro, K., Querol, A., Ramirez-Gargallo, G., Ramirez-Miranda, G., Vinyals, J., Vizcaino, P., Garcia-Gasulla, M. and Mantovani, F., 2020, March. **Performance study of HPC applications on an Arm-based cluster using a generic efficiency model**. In 2020 28th Euromicro International Conference on Parallel, Distributed and Network-Based Processing (PDP) (pp. 167-174). IEEE.

Research Gate

Arm Embedded Boards
2017



Arm Server Systems
2019

RISC-V Embedded Boards
2021

RISC-V FPGA prototype
2022

RISC-V Commercial PC
2024