A Fully-Differential Folded-Cascode Operational Amplifier in IBM $0.18\mu m$ process

Gustavo C. Martins

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Abstract

A fully-differential folded-cascode operational amplifier was designed with IBM $0.18\mu m$ 7RF process. The amplifier has $85.3dB$ differential gain, cut-off frequency equal to $2.2MHz$ and differential output signal excursion greatear than $1V$, operating with an $1.8V$ power supply.

1 Introduction

The operational amplifier (OpAmp) is one of the basic building blocks of analog circuits. The main characteristics of OpAmps are differential input, high gain, low output impedance and high input impedance. They have several applications, such as A/D and D/A converters, voltage regulators, signal generators, signal processing and intrumentation amplifiers.

The goal of this work is to design a Fully-Differential Folded-Cascode OpAmp, in IBM $0.18\mu m$ (CRF7SF) process, that meet the specifications presented in Table 1. Where the settling time is the time in which the difference between output and input signal reaches 1% of the initial difference. For this measurement, the input is a small signal. The settling time and total harmonic distortion (THD) are measured with the OpAmp in unity gain configuration.

The next section discuss some details of the transistor's parameter extraction. The third section describes the process of hand design. The fourth section presents the schematic and simulation results. The fifth section presents the layout and simulation results with extracted parasitics. The last section is the conclusion of this work.

Table 1: OpAmp specifications

Spec.	Value
A_{v0}	$> 80dB$
GBW	$\cong 2MHz$
PM	$> 55^o$
SR	$> 1V/\mu s$
Systematic Offset	$< 200\mu V$
Settling Time	$< 700ns$
THD	$< 1\%$ @ $1Vpp$
Input Ref. Noise	$< 300nV/\sqrt{Hz}$ @ $1kHz$
Input Ref. Noise	$< 25nV/\sqrt{Hz}$ @ $1MHz$
Power	$< 1mW$
Supply Voltage	$1.8V$
C_L	$20pF$

2 Parameters Extraction

In order to perform the hand design it is first needed to extract some transistor parameters. The following parameters were extracted: normalized Early voltage V_E, sheet specific current I_{SQ} and threshold voltage V_{T0}. The parameters are summarized in Table 2.

It was observed that the normalized Early votage V_E slightly varies for different conditions (channel length and width, gate, drain and source voltages). Thus, to obtain more accurate results, the conditions were set to be near the ones met by the transistors at the output branches, i.e., $L = 1.8\mu m$, $W = 30\mu m$, $V_G = V_{T0}$ and $V_S = V_{SS}$ (for NMOS) or V_{DD} (for PMOS). To extract the V_E, V_D is swept and the g_{md} is calculated at the chosen value $V_D = 0.9V$ through Equation 1, then V_E is calculated using the approximation given in Equation 2. The obtained values of V_E are: $19.19V/\mu m$ for the PMOS and $5.5V/\mu m$ for the NMOS.

$$g_{md} = \frac{\partial I_D}{\partial V_D} \tag{1}$$

$$g_{md} = \frac{I_D}{V_E L} \tag{2}$$

The threshold voltage V_{T0} and the sheet specific current I_{SQ} were extracted through the g_m/I_D method [1] [2]. The obtained values are: $V_{T0N} = 0.52V$, $V_{T0P} = -0.40V$, $I_{SQN} = 141nA/\square$ and $I_{SQP} = 19.6nA/\square$.

Table 2: Extracted transistor parameters

Parameter	NMOS	PMOS
I_{SQ}	$141nA$	$19.6nA$
V_{T0}	$0.52V$	$-0.40V$
V_E	$5.5V/\mu m$	$19.19/\mu m$

3 Hand Design

The design of this OpAmp is divided in three parts: amplifier, which effectively amplifies the input signals; bias, the bias circuit; and common mode feed back (CMFB), which sets the output common mode. We start by designing the amplifier circuit. The chosen topology of this circuit is presented in Figure 1.

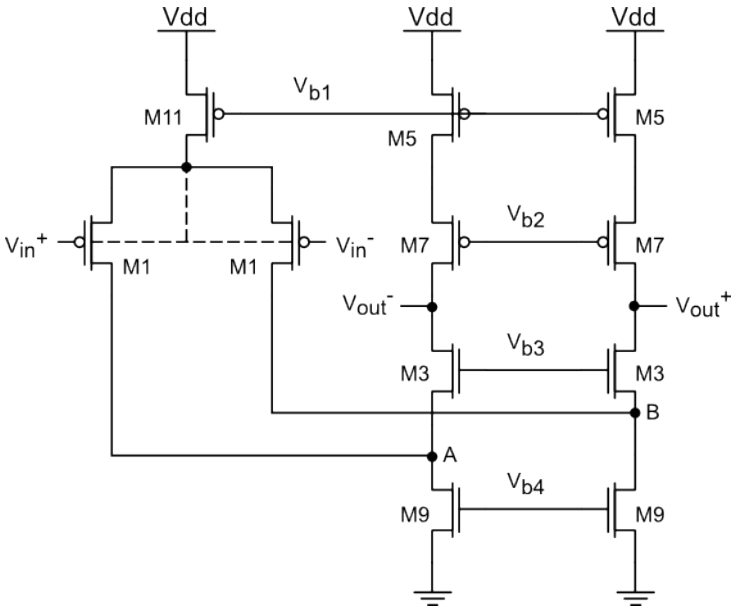

Figure 1: Amplifier circuit

We start by choosing a tail current I_T for the OpAmp. The current I_T flows through transistor M11 and the current that flows through transistor M9 is $I_T/2$. The minimum I_T is given by the minimum slew rate and the maximum I_T can be estimated from the maximum power specification. The minimum SR is $1V/\mu s$, so the minimum I_T, with a $20pF$ load capacitance C_L, is $40\mu A$. To estimate the maximum I_T, it was first considered that the entire OpAmp would consume $6I_T$ ($2I_T$ for the amplifier, $1I_T$ for the CMFB and $3I_T$ for bias). The maximum power is $1mW$, so the maximum I_T would be $92.6\mu A$. The chosen I_T was $50\mu A$, so that we have some margin from the minimum I_T and still have a high gain (smaller

the I_T, higher the gain).

Now we must define g_{m1} (gate transconductance of transistor M1). It is given by the gain bandwidth GBW, which is approximately $2MHz$. Through Equation 3, it is calculated $g_{m1} \cong 251.3\mu S$. It is considered that the GBW is define for one branch, not related to the differential output.

$$GBW = \frac{g_{m1}}{C_L} \tag{3}$$

Now we can calculate the inversion level at source i_{f1} of transistor M1 using Equantion 4. The calculated value is 31.25. With this value of i_{f1} and the value of g_{m1} it is possible to calculate, through Equation 5, the aspect ratio S1 of this transistor, which was found to be approximately 40.8. For a chosen channel length L was 2 times the minimum L, that is $L1 = 0.36\mu m$, we have $W1 = 14.69\mu m$. These equation are valid because transistors M1 are operating in saturation and it is considered $n_p = 1.15$.

$$g_{m1} = \frac{I_T}{2n_p\phi_t}\frac{2}{\sqrt{1+i_f}+1} \tag{4}$$

$$I_{D1} = \frac{I_T}{2} = I_{SQP}S_1 i_{f1} \tag{5}$$

Let us consider now the output branches. These branches are designed to support an excursion of the output signal equal to $1V$. For this purpose we must set the drain to source saturation voltage V_{DSsat} equal to $200mV$, because we have four transistors in series and $1.8V$ supply voltage. Actually it is set $V_{DSsat} = 200mV - \Delta V = 175mV$, for a safety margin. Using Equation 6 we can find the inversion level i_f of the transistors, which are $i_{f3,5,7,9} = 13.11$.

$$V_{DSsat} + \phi_t(\sqrt{1+i_f}+3) \tag{6}$$

Based on drain current ($= I_T/2$), i_f and I_{SQ}, we calculate the aspect ratio of these transistors. The aspect ratios are presented in Table 3. The W and L of the transistors will be chosen to obtain a gain greater than $80dB$. A small signal analyses is executed to determine the equation that defines the OpAmp's gain. The equation found is the Equation 7. It is important to notice that the effects of CMFB circuit and transistors M1 and M11 are neglected. Thus, the gain will be lower than the calculated.

$$A_{v0} = \frac{-g_{md7}g_{ms7}}{g_{md5}+g_{ms7}} - \frac{g_{md3}g_{ms3}}{g_{md9}+g_{ms3}} + g_{md3} + g_{md7} \tag{7}$$

These tranconductances can be calculated using the Equations 8 and 2.

$$g_{ms} = \frac{I_D}{\phi_t} \frac{2}{\sqrt{1+i_f}+1} \tag{8}$$

Knowing the aspect ratio of each transistors, their L was chosen to obtain a high gain in a reasonable chip area. The dimensions of the transistors can be found in Table 3. For these dimensions the calculated gain is $97dB$.

With the amplifier already designed, we must proceed with the design of the CMFB and bias circuit. The CMFB and bias schematics are shown in Figures 2 and 3, respectively.

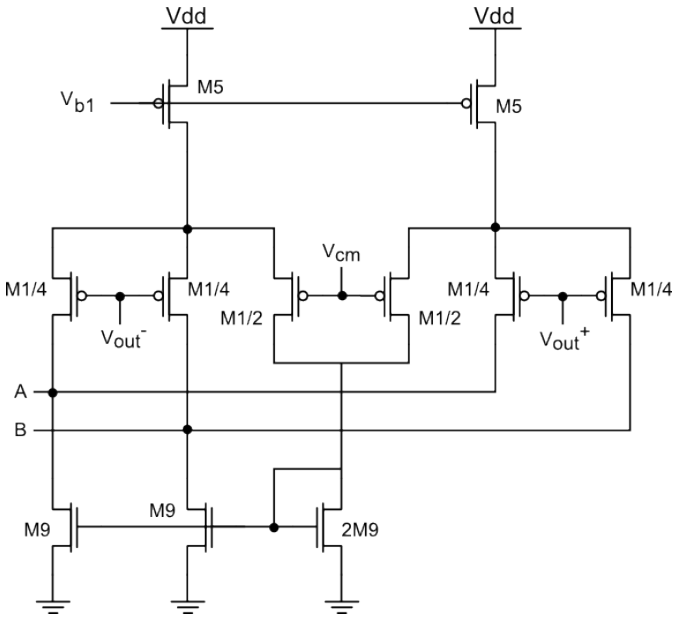

Figure 2: Commom mode feedback circuit

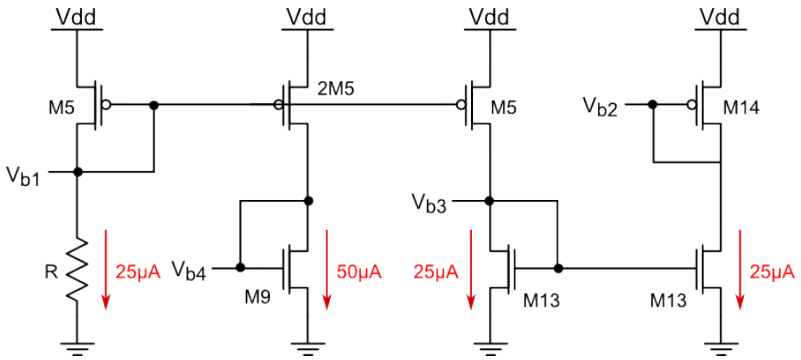

Figure 3: Bias circuit

Knowing the inversion level of the transistors we can define their dimensions. The dimensions of all the transistors and their inversion level are presented in Table 3. The resistance of R can be found through the UICM and Ohm's law, and it is equal to $52.7k\Omega$.

Table 3: Hand design results

Transistor	S	W (μm)	L (μm)	i_f
M1	40.81	14.69	0.36	31.25
M3	13.52	175.77	13	13.11
M5	97.27	175.08	1.8	13.11
M7	97.27	350.17	3.6	13.11
M9	27.04	135.21	5	13.11
M11	194.54	350.17	1.8	13.11
M13	1.70	22.08	13	52.15
M14	12.22	43.98	3.6	52.19

The maximum and minimum values of input signal common mode were calculated and are equal to 1.04V and 0.13V, respectively.

4 Schematic

The schematic was draw and the simulation results are presented here. The results are summarized in Table 4.

The current drawn from supply is $277.5\mu A$. Thus, the power comsuption is $499.5\mu W$.

Open loop gain for low frequencies A_{v0} is $80.13dB$ and phase margin PM, GBW is $2.248MHz$ and PM is 64.93^o. The plot of gain and phase is shown in Figure 4. This is refered to one output, not the differential output.

The total harmonic distortion (THD) with a differential output signal of $1Vpp$ is $3.8 \cdot 10^{-5}\%$. For this measurement it was used an unity gain configuration with resistors equal to $25M\Omega$, $V_{icm} = 600mV$ and $V_{ocm} = 900mV$. The frequency of the input/output signal in this simulation is $50Hz$. The output signal in this configuration is shown in Figure 5.

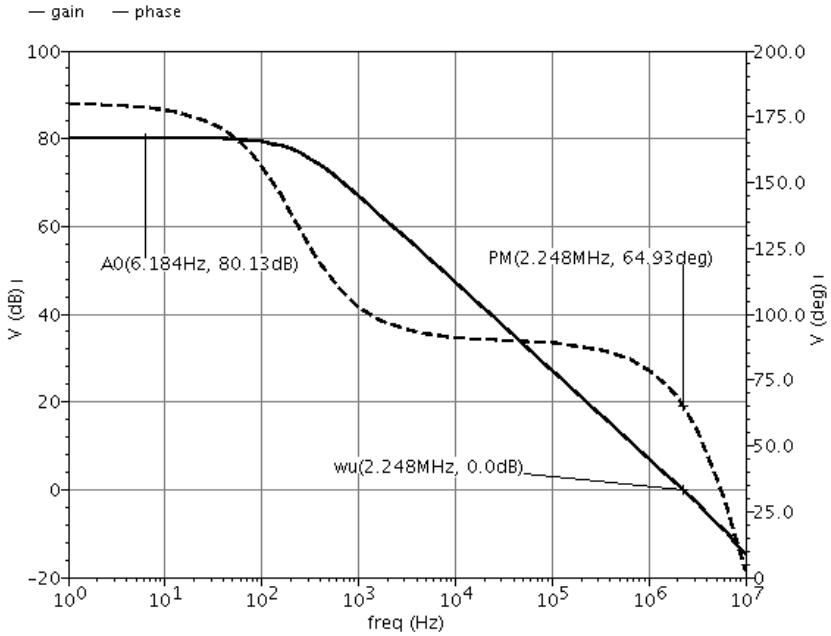

Figure 4: Bode diagram of gain and phase retrieved from schematic simulation

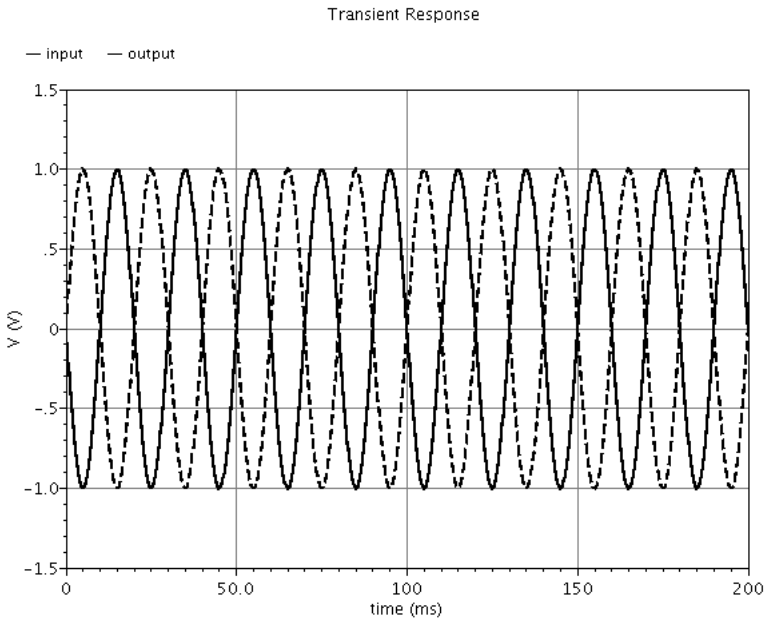

Figure 5: Differential output and input waveforms at 50Hz, schematic simulation

Now with an unity gain configuration with resistors equal to $1M\Omega$. Input signals are steps of $20mV$ and have fall/rise time equal to $1ns$. The measured settling time of output signal is $410ns$. The transient simulation result is presented in Figure 6.

Input refered noise measured at $1kH$ was $191nV/\sqrt{Hz}$ and at $1Mhz$ was $22.16nV/\sqrt{Hz}$, as shown in Figure 7.

The systematic offset is $0V$ because the schematic is symmetric. When the layout is implemented an offset, will appear due to the non symmetry of the interconnections.

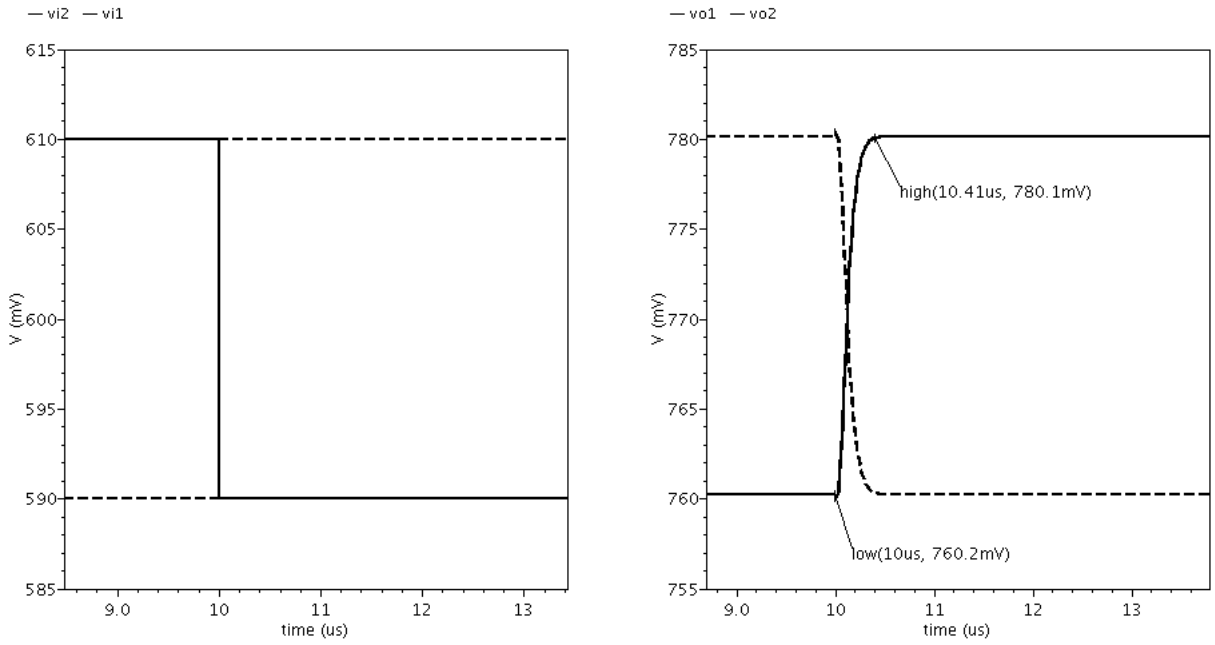

Figure 6: Settling time analysis of schematic

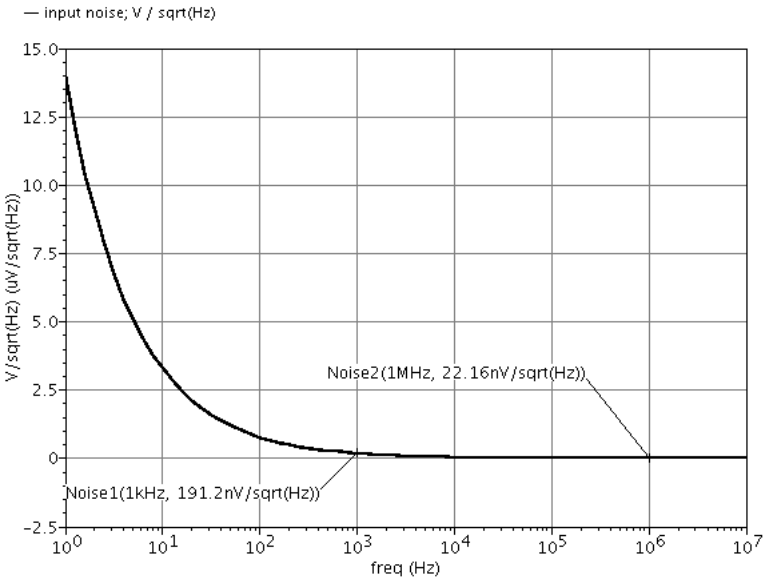

Figure 7: Input referred noise of schematic

Table 4: Schematic simulation results

Spec.	Value
A_{v0}	$80.13dB$
GBW	$2.248MHz$
PM	64.93^o
SR	$1.04V/\mu s$
Systematic Offset	$0V$
Settling Time	$410ns$
THD	$3.8 \cdot 10^{-5}\%$ @ $1Vpp$
Input Ref. Noise	$191nV/\sqrt{Hz}$ @ $1kHz$
Input Ref. Noise	$22.16nV/\sqrt{Hz}$ @ $1MHz$
Power	$0.5mW$

5 Layout

The layout for the OpAmp is shown in Figure 8. The dimensions of the layout are $193.41\mu m$ width and $202.35\mu m$ height, totalizing an area equal to $39137\mu m^2$. That is 1.74% of the chip area ($1.5mm$ x $1.5mm$).

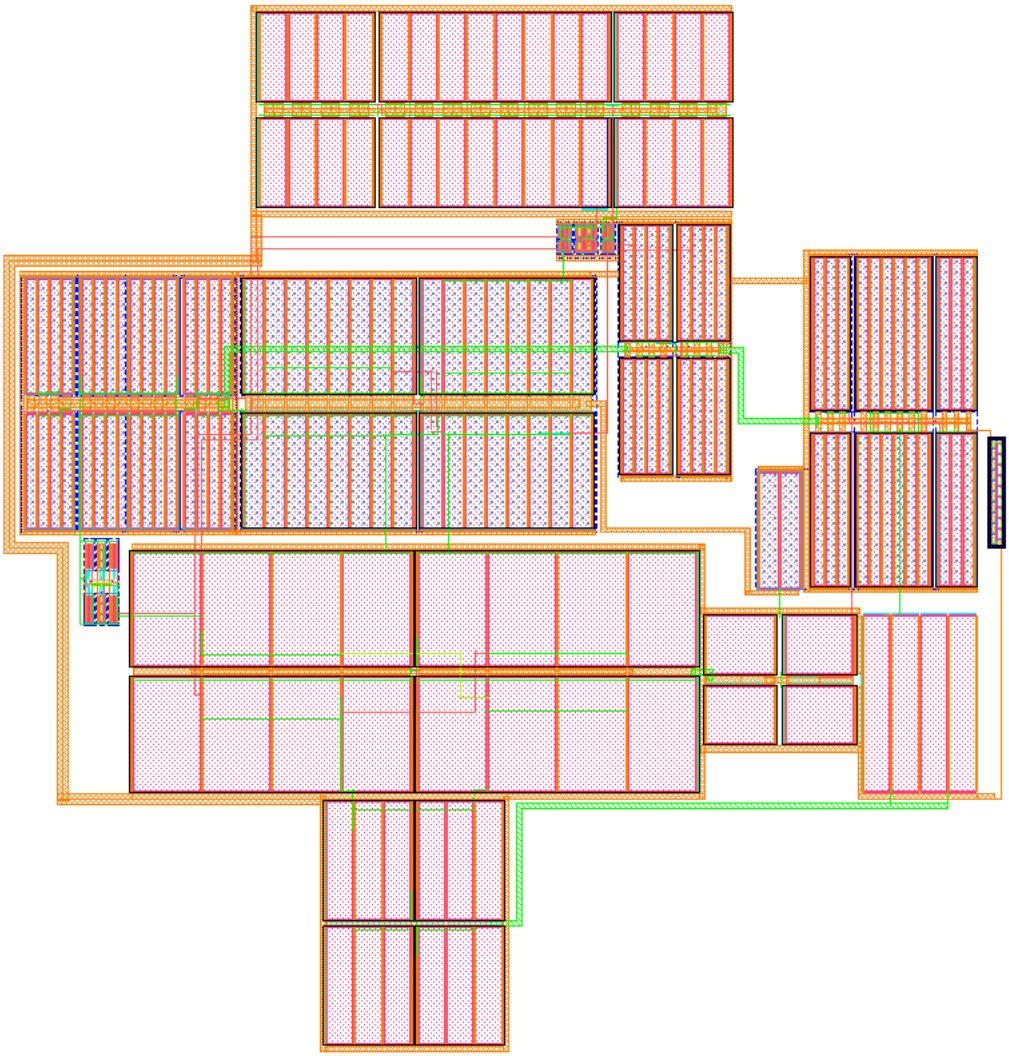

Figure 8: Layout

One of the layout considerations is the minimum wire width for the first metal level, the one that support less current. It was chosen to be $0.3\mu m$, so the maximum DC current is approximately $790\mu A$, that's greater than the total current. In critical sections, where the current is known to be higher (for example, supply interconnections), greater care were taken and wider wires were used.

Other consideration is the common-centroid geometries for transistors that must match, for example, the differential input pair and current mirrors.

The Design Rule Check (DRC) and Layout Versus Schematic (LVS) were successfully executed. Then the resistance and capacitante (RC) parasitcs were extracted via QRC and the final netlist was simulated. Figures 9 to 12 presents

the simulations results for the same configurations presented in last section. The simulation results are summarized in Table 5.

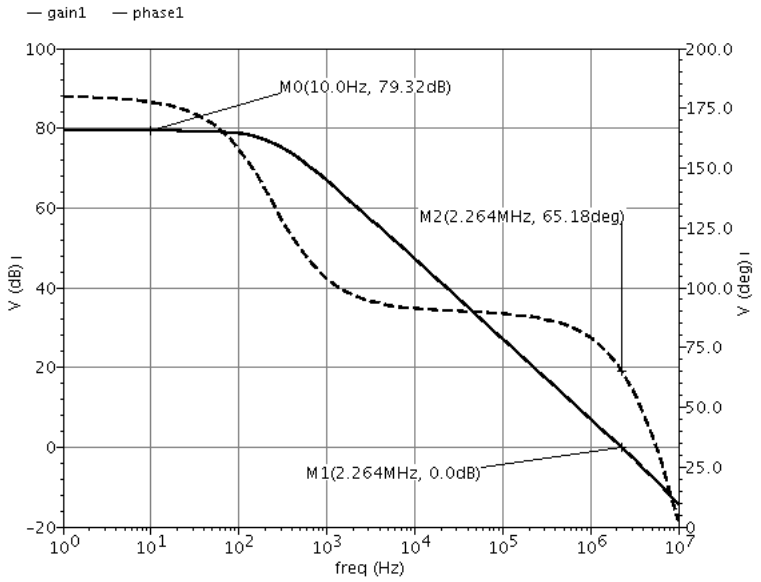

Figure 9: Bode diagram of gain and phase retrieved from layout simulation

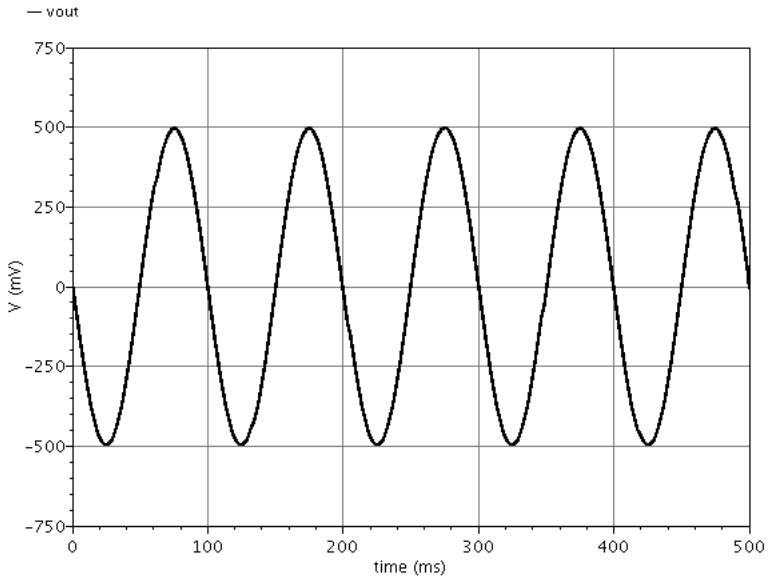

Figure 10: Differetial output waveform at 50Hz, layout simulation

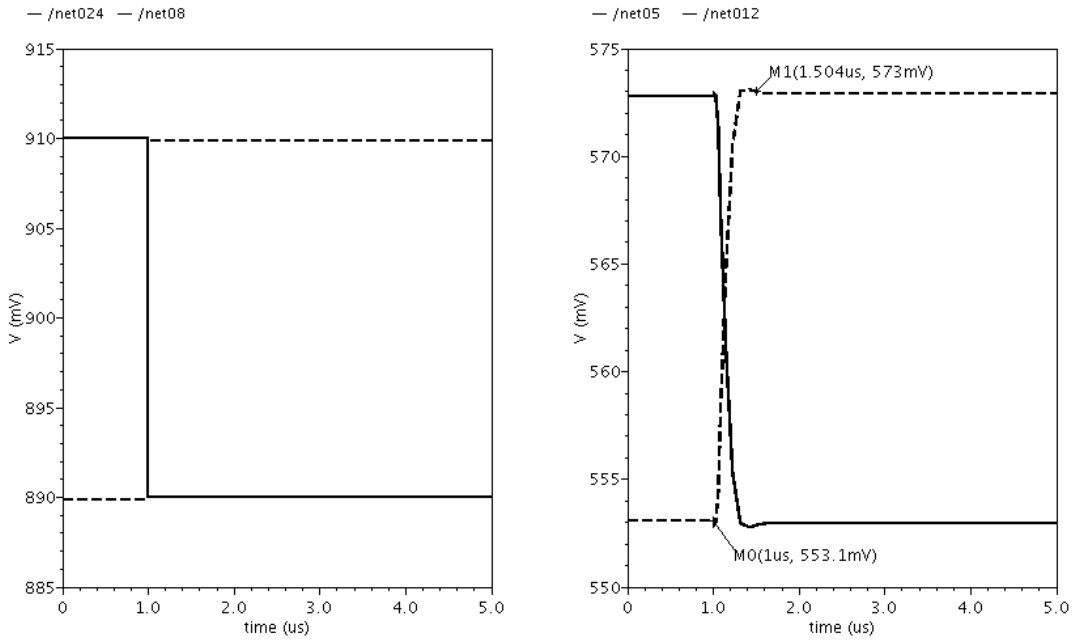

Figure 11: Settling time analysis of layout

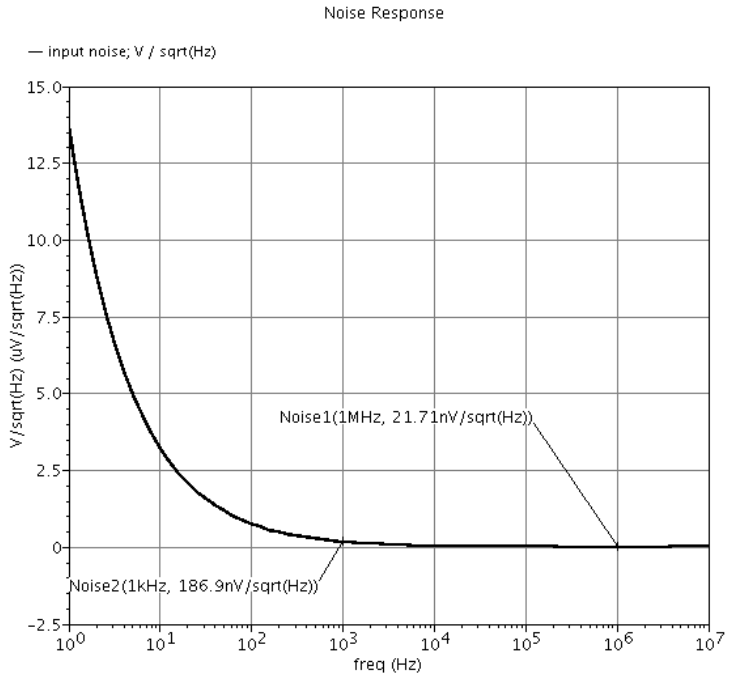

Figure 12: Input referred noise of layout

Table 5: Layout simulation results

Spec.	Value
A_{v0}	$79.32dB$
GBW	$2.264MHz$
PM	65.18^o
SR	$992mV/\mu s$
Systematic Offset	$128\mu V$
Settling Time	$504ns$
THD	$4 \cdot 10^{-3}\%$ @ $1Vpp$
Input Ref. Noise	$186.9nV/\sqrt{Hz}$ @ $1kHz$
Input Ref. Noise	$21.71nV/\sqrt{Hz}$ @ $1MHz$
Power	$0.5mW$

Besides that, a simulation was performed to garantee the funcionality of CMFB in the desired output signal range. For that, a voltage was applied to each output node and the voltage of nodes A and B are observed. Figure 13 presents the A and B node voltages versus the differential voltage V_o^+ - V_o^-. It can be noticed that the CMFB operates correctly until the differential output is around $1.2V$, so the circuit works correctly in its operation range ($1V$ differential output). In correct operation it was expected that the A and B voltages would maintain the same value, since common mode doesn't change, that is what is observed until 1.2V. After this value the voltages of A and B get far apart, so we can say that the circuit doesn't operates correctly after this point.

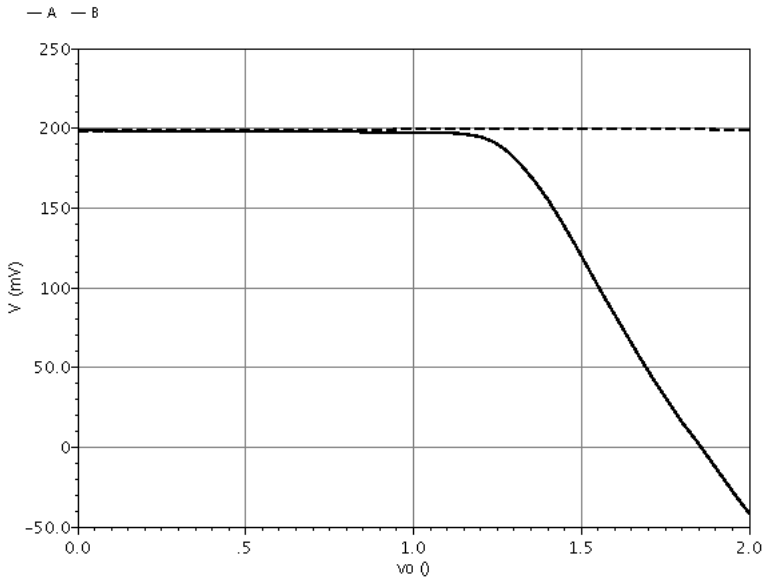

Figure 13: Test of CMFB operation

6 Conclusion

A fully-differential folded-cascode OpAmp was designed with $85.32dB$ differential gain, $2.2MHz$ GBW and $0.5mW$ power consumption, with IBM $0.18\mu m$ technology process. The OpAmp has a greater than 1V differential output signal excursion with $1.8V$ power supply.

References

[1] M. C. Schneider, C. Galup-Montoro. *CMOS Analog Design Using All-Region MOSFET Modeling*, 1st edition, Cambridge University Press, 2010, ISBN 978-0521110365.

[2] M. C. Schneider, C. Galup-Montoro, M. B. Machado and A. I. A. Cunha. *Interrelations between Threshold Voltage Definitions and Extraction Methods*, The Nanotechnology Conference and Trade Show, Boston, USA, Proceedings of Nanotech 2006, pp. 868- 871, May 2006.