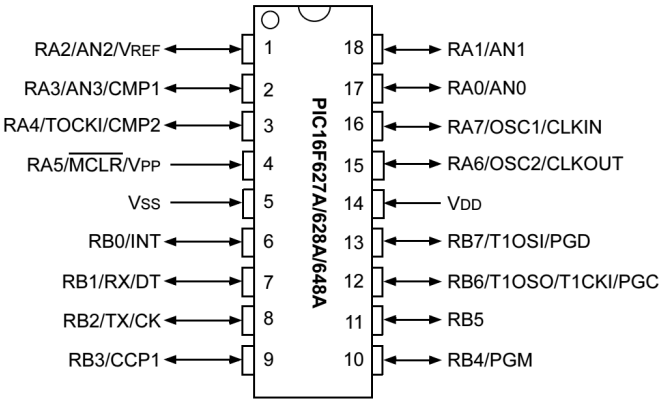
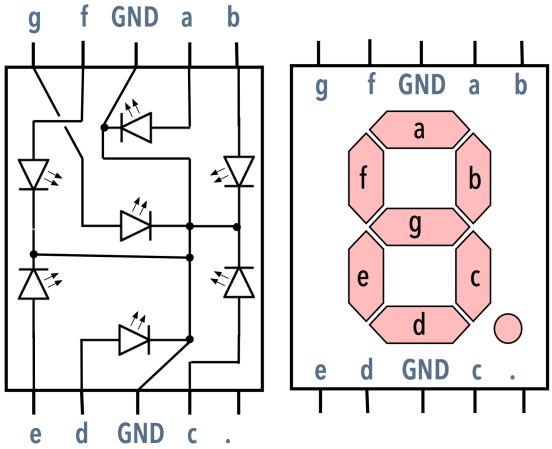
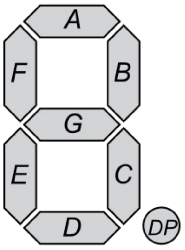
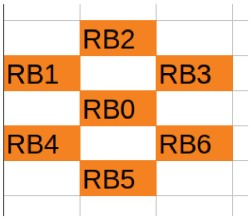


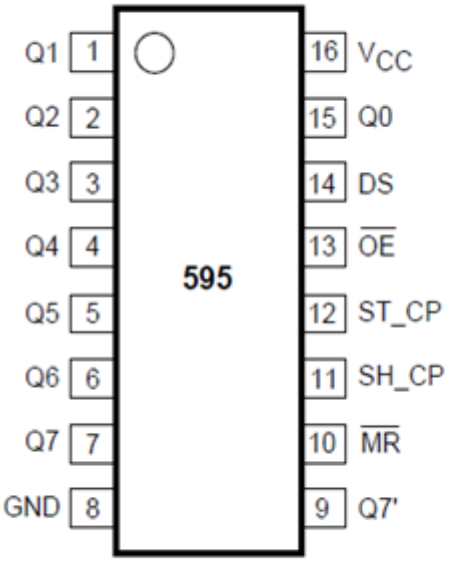






- Pino 1 do gravador → Vpp/MCLR
- Pino 2 do gravador → Vdd
- Pino 3 do gravador → Vss
- Pino 4 do gravador → PGD
- Pino 5 do gravador → PGC

```
    //dc_ebafg
 0: 0b11011110;
 1: 0b01001000;
 2: 0b10011101;
 3: 0b11001101;
 4: 0b01001011;
 5: 0b11000111;
 6: 0b11010111;
 7: 0b01001100;
 8: 0b11011111;
 9: 0b11001111;
10:0b10000100; //duas barras
Erro:0b10010111; //Erro
```



Pinos de saída: 15, 1, 2, 3, 4, 5, 6, 7

PIN	SYMBOL	DESCRIPTION
1	Q1	parallel data output
2	Q2	parallel data output
3	Q3	parallel data output
4	Q4	parallel data output
5	Q5	parallel data output
6	Q6	parallel data output
7	Q7	parallel data output
8	GND	ground (0 V)
9	Q7'	serial data output
10	$\overline{MR}$	master reset (active LOW)
11	SH_CP	shift register clock input
12	ST_CP	storage register clock input
13	$\overline{OE}$	output enable (active LOW)
14	DS	serial data input
15	Q0	parallel data output
16	V_{CC}	positive supply voltage