



Allwinner A23 User Manual

Dual-Core Mobile Application Processor

Revision 1.0

August 30, 2013

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Revision History

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Chapter 1

About This Document

The Allwinner A23 processor is a remarkably power efficient dual-core mobile application processor that is constructed on the basis of ARM Cortex™-A7 CPU and Mali400MP2 GPU architecture, and features all the optimizations and enhancements Allwinner has made for mobile application.

This user manual of A23 processor is intended to be used by board-level product designers and product software developers. This manual assumes that the reader has a background in computer engineering and/or software engineering and understands concepts of digital system design, microprocessor architecture, Input / Output (I/O) devices, industry standard communication and device interface protocols.

Chapter 2

Platform Introduction

This chapter provides a brief introduction of the dual-core A23 processor.

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2.1 Overview

The Allwinner A23 is a remarkably power-efficient dual-core mobile application processor that based on ARM Cortex™-A7 CPU together with Mali400MP2 GPU architecture. It also outperforms its competitors in terms of total system cost, and enables excellent user experience without compromising the battery life.

Main features of A23 include:

CPU architecture: A23 is based on dual-core Cortex™-A7 CPU architecture to deliver superior system performance as well as optimized battery life experience, in that Cortex™-A7 is the most power efficient CPU core ARM's ever developed.

Graphic: A23 adopts the extensively implemented and technically mature Mali400MP2 GPU to provide end users with optimal experience in web browsing, video playback and games; OpenGL ES 2.0 and OpenVG 1.1 standards are supported;

Video Engine: A23 supports high-definition 1080P video processing, and supports various mainstream video standards such as H.264, VP8, MPEG 1/2/4, JPEG/MJPEG, etc;

Display: A23 supports CPU/RGB/LVDS LCD interface up to 1280x800 resolution. Four-lane MIPI DSI (Display Serial Interface) is integrated as well, supporting MIPI DSI V1.01 and MIPI D-PHY V1.00;

Image: A23 supports a parallel CMOS sensor interface up to 5M resolution

Thanks to its advanced system design and outstanding software optimization, the A23 is capable of providing top-notch system performance with long-lasting battery life experience: in addition to its energy-efficient Cortex™-A7 CPU architecture, advanced fabrication process, video acceleration hardware, DVFS technology support and high system integration, A23 also features a unique Talking Standby Mode where the processor can be inactive during voice calls to provide end users with ultra-long battery life experience. Additionally, Allwinner A23 features high system integration with a wide range of integrated I/Os like 4-lane MIPI DSI, LVDS, USB OTG/HOST, SD/MMC, I2S/PCM, thus significantly reducing system components required in design to simplify product design and reduce total system costs.

2.2 System Features

2.2.1 ARM CPU Architecture

The dual-core A23 platform is based on ARM's Cortex™-A7 CPU architecture.

- ARMv7 ISA standard instruction set plus Thumb-2 and Jazeller RCT
- NEON with SIMD and VFPv4 support
- Support hardware virtualization
- Support LPAE
- Support 4GB address space
- 128KB L1 cache and shared 256KB L2 cache
- Support DVFS with independent power domain

2.2.2 Mali400MP2 GPU

- ARM Mali400MP2 GPU
- Support OpenGL ES 2.0 / OpenVG 1.1 standard

2.2.3 Memory Subsystem

This section includes:

- Boot ROM
- SDRAM
- NAND Flash
- SD/MMC interface

BOOT ROM

- Support system boot from Raw NAND, eMMC NAND, SPI Nor Flash, SD/TF card (SDMC0/2)
- Support system code download through USB OTG (USB0)

SDRAM

- Support 1GB address space
- Support 16-bit bus width
- Support DDR3 /DDR3L SDRAM

NAND FLASH

- Comply to ONFI 2.3 and Toggle 1.0
- Support 64-bit ECC per 512 bytes or 1024 bytes
- 8-bit Raw NAND flash controller sharing pin with eMMC
- Support 3.0V IO voltage
- Support up to 2 CE and 2 RB signals
- Support SLC/MLC/TLC NAND and EF-NAND

SD/MMC INTERFACE

- Comply to eMMC standard specification V4.41, SD physical layer specification V2.0, SDIO card specification V2.0
- Support 4 / 8-bit bus width
- Support HS/DS/SDR12/SDR25 bus mode
- Support three SD/MMC controllers
- Support SDIO interrupt detection
- Support build-in 128-byte FIFO for buffered read or write operations
- Support 3.0V IO voltage

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2.2.4 System Peripheral

This section includes:

- Timer
- High Speed Timer
- RTC
- GIC
- DMA
- CCU
- PWM

TIMER

- Support two timers: clock source can be switched over 24MHz and 32768Hz
- Support two 33-bit AVS counters
- Support one 64-bit system counter from 24MHz
- Support watchdog to generate reset signal or interrupts

HIGH SPEED TIMER

- Clock source is fixed to AHB, and the pre-scale ranges from 1 to 16
- Support 56-bit counter

RTC

- Support full clock features: second/minute/hour/day/month/year
- Support 32768Hz clock fanout

GIC

- Support 16 SGIs, 16 PPIs and 128 SPIs
- Support ARM architecture security extensions
- Support ARM architecture virtualization extensions
- Support single processor and multiprocessor environments

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DMA

- 8-channel DMA
- Support data width of 8/16/32 bits
- Support linear and IO address modes

CCU

- 9 PLLs
- 24MHz oscillator, a 32768Hz oscillator and an on-chip RC oscillator

PWM

- 2 PWM outputs
- Support cycle mode and pulse mode
- The pre-scale is from 1 to 64

2.2.5 Display Subsystem

This section includes:

- Display engine
- Video output

DISPLAY ENGINE

- Four movable layers, each layer size up to 8192x8192 pixels
- Ultra-Scaling engine
 - 4-tap scale filter in horizontal and vertical
 - Support source image size from 8x4 to 8192x8192 resolution and destination image size from 8x4 to 8192x8192 resolution
- Support multiple image input formats: mono 1/2/4/8 bpp, palette 1/2/4/8 bpp, 6/24/32 bpp color, YUV444/420/422/411
- Support alpha blending / color key / gamma
- Support output color correction: luminance / hue / saturation, etc
- Support Color Management Unit (CMU) and Dynamic Range Correction (DRC)
- Support real time write back function

VIDEO OUTPUT

- Support CPU / Sync RGB / LVDS LCD interface up to 1280x800 resolution
- Integrated 4-lane MIPI DSI interface up to 1280x800 resolution
 - Support MIPI DSI V1.01 and D-PHY V1.00
 - Support command mode and video mode (non-burst mode with sync pulses, non-burst mode with sync event and burst mode)
- Support RGB666 dither function

2.2.6 Video Engine

VIDEO DECODING

- Support video playback up to 1920x1080@60ps
- Support multi-format video playback, including MPEG1/2, MPEG4 SP/ASP GMC, H.263 including Sorenson Spark, H.264 BP/MP/HP, VP8, JPEG/MJPEG, etc

VIDEO ENCODING

- Support H.264 HP video encoding up to 1920x1080@60fps
- JPEG baseline: picture size up to 4080x4080
- Support Alpha blending
- Support thumb generation
- 4x2 scaling ratio: from 1/16 to 64 arbitrary non-integer ratio

2.2.7 Video Input

- Support parallel camera sensor
- 8-bit CCIR601/656 interface
- Support up to 5M pixel camera sensor
- Support dual outputs for display and encoding

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2.2.8 Audio Subsystem

ANALOG AUDIO CODEC

- Support stereo audio DAC
 - Up to 100dB SNR
 - 8KHz to 192KHz DAC sample rate
- Stereo audio ADC
 - Up to 94dB SNR
 - 8KHz ~ 48KHz ADC sample rate
- Support four analog audio inputs
 - Two microphone differential inputs for main mic and headphone mic
 - One differential phone input for modem
 - One stereo line-in input for FM
- Support two analog audio outputs
 - One stereo or differential capless headphone output
 - One differential earpiece output
- Support talking standby mode, where the application processor remains inactive during voice call application

2.2.9 External Peripherals

This section includes:

- USB 2.0 OTG
- USB HOST
- LRADC
- Digital Audio
- UART
- SPI
- Open-drain TWI
- RSB™

USB 2.0 OTG

- Support High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) in Host mode
- Support High-Speed (HS, 480-Mbps) and Full-Speed (FS, 12-Mbps) in Device mode
- Support up to 5 user-configurable endpoints for Bulk, Isochronous, Control and Interrupt

USB HOST

- EHCI/OHCI-compliant hosts
- USB2.0 PHY and HSIC

LRADC

- 6-bit resolution

DIGITAL AUDIO

- Support two I2S/PCM compliant digital audio interfaces for modem and BT
- I2S supports 2 channels output and 2 channels input
- PCM supports linear sample(8-bit or 16-bit), 8-bit u-law and A-law companded sample

UART

- Six UART controllers
- FIFO size up to 64 bytes
- Support speed up to 3MHz

SPI

- Two SPI controllers with one CS signal
- Master/Slave configurable

TWI

- Support four TWIs
- One dedicated TWI for CSI
- Support speed up to 400Kb/s

RSB

- Support speed up to 20MHz

2.2.10 Power Management

- Support DVFS for CPU frequency and voltage adjustment
- Support super standby mode for power efficiency
- Support talking standby mode for energy efficiency during voice call applications

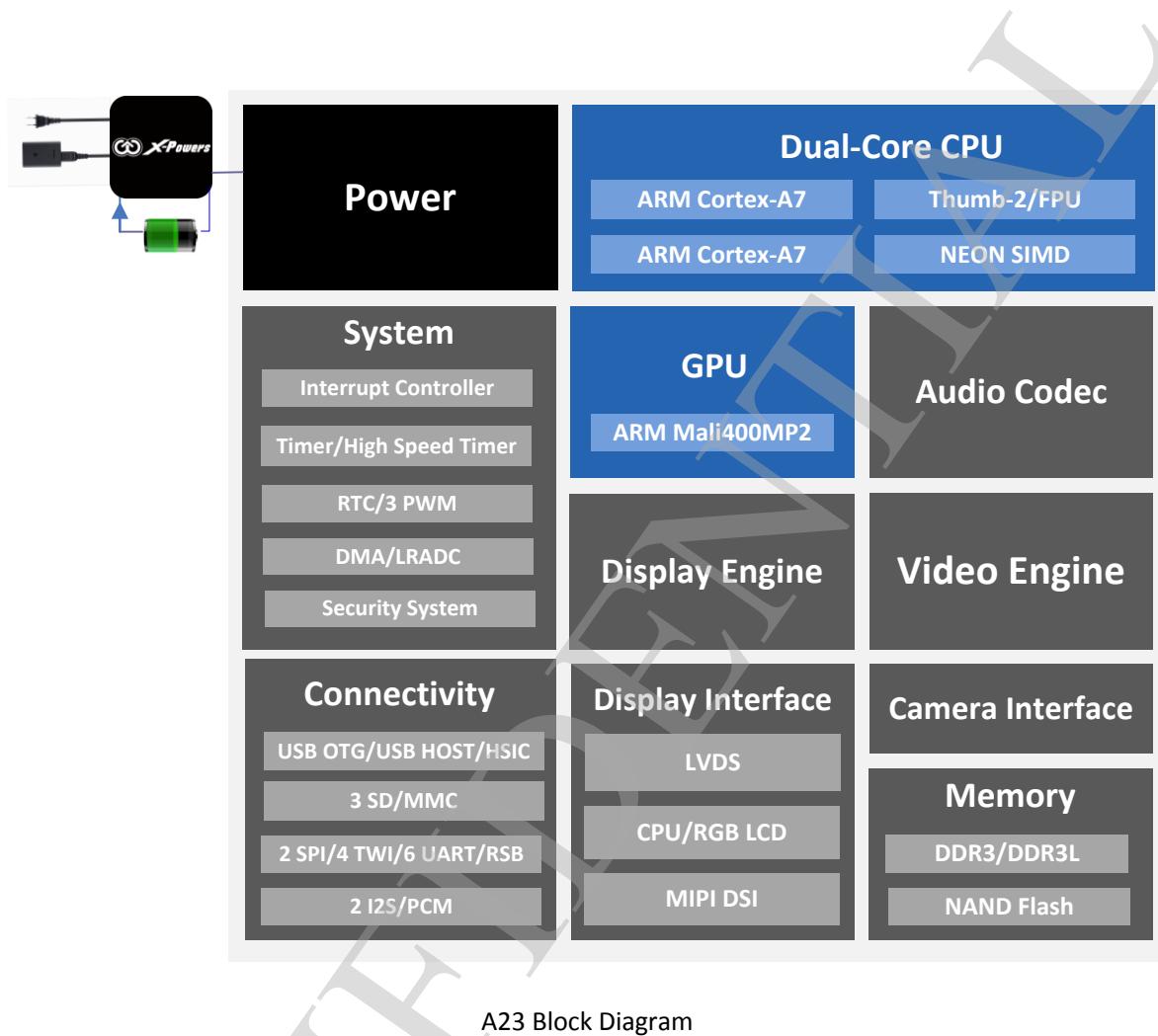
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2.2.11 Process and Package

- 40nm LP process
- FBGA 280 balls, 0.80mm ball pitch, 14 x 14 x 1.4-mm

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2.3 Block Diagram



Chapter 3

System

This chapter introduces the A23 system architecture from several perspectives, including memory mapping, boot system, clock control unit (CCU), CPU configuration, power/reset/clock management, timer, PWM, high-speed timer, DMA, GIC, RTC, system control, audio CODEC, LRADC, thermal sensor controller, port configuration, etc.

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3.1 Memory Map

Module	CPU0/1 Address	Size(Bytes)
SRAM A1	0x0000 0000---0x0000 3FFF	16K
SRAM A2	0x0004 4000---0x0005 3FFF 0x40100, 0x40200, 0x40300, 0x40400, 0x40500, 0x40600, 0x40700, 0x40800, 0x40900, 0x40a00, 0x40b00, 0x40c00, 0x40d00, 0x40e00	64K
VE SRAM	0x0000 4000---0x0000 FFFF	48K
SRAM Controller	0x01C0 0000---0x01C0 0FFF	4K
DMA	0x01C0 2000---0x01C0 2FFF	4K
NDFC	0x01C0 3000---0x01C0 3FFF	4K
LCD	0x01C0 C000---0x01C0 CFFF	4K
VE	0x01C0 E000---0x01C0 EFFF	4K
SD/MMC 0	0x01C0 F000---0x01C0 FFFF	4K
SD/MMC 1	0x01C1 0000---0x01C1 0FFF	4K
SD/MMC 2	0x01C1 1000---0x01C1 1FFF	4K
/	0x01C1 2000---0x01C1 2FFF	4K
SS	0x01C1 5000---0x01C1 5FFF	4K
/	0x01C1 7000---0x01C1 7FFF	/
/	0x01C1 8000---0x01C1 8FFF	/
USB OTG	0x01C1 9000---0x01C1 9FFF	4K
USB EHCI0/OHCI0	0x01C1 A000---0x01C1 AFFF	4K
/	0x01C1 C000---0x01C1 CFFF	4K
CCU	0x01C2 0000---0x01C2 03FF	1K
/	0x01C2 0400---0x01C2 07FF	1K
PIO	0x01C2 0800---0x01C2 0BFF	1K

TIMER	0x01C2 0C00---0x01C2 0FFF	1K
PWM	0x01C2 1400---0x01C2 17FF	1K
DAUDIO-0	0x01C2 2000---0x01C2 23FF	1K
DAUDIO-1	0x01C2 2400---0x01C2 27FF	1K
LRADC	0x01C2 2800---0x01C2 2BFF	1K
AD/DA	0x01C2 2C00---0x01C2 2FFF	1K
THERMAL SENSOR CONTROLLER	0x01C2 5000---0x01C2 53FF	1K
UART 0	0x01C2 8000---0x01C2 83FF	1K
UART 1	0x01C2 8400---0x01C2 87FF	1K
UART 2	0x01C2 8800---0x01C2 8BFF	1K
UART 3	0x01C2 8C00---0x01C2 8FFF	1K
UART 4	0x01C2 9000---0x01C2 93FF	1K
/	0x01C2 9400---0x01C2 97FF	1K
TWI 0	0x01C2 AC00---0x01C2 AFFF	1K
TWI 1	0x01C2 B000---0x01C2 B3FF	1K
TWI 2	0x01C2 B400---0x01C2 B7FF	1K
/	0x01C2 B800---0x01C2 BBFF	1K
GPU	0x01C4 0000---0x01C4 FFFF	64K
HSTMRR	0x01C6 0000---0x01C6 0FFF	4K
/	0x01C6 1000---0x01C6 1FFF	4K
DRAMCOM	0x01C6 2000---0x01C6 2FFF	4K
DRAMCTL	0x01C6 3000---0x01C6 3FFF	4K
DRAMPHY	0x01C6 5000---0x01C6 5FFF	4K
/	0x01C6 7000---0x01C6 7FFF	/
SPI0	0x01C6 8000---0x01C6 8FFF	4K
SPI1	0x01C6 9000---0x01C6 9FFF	4K
/	0x01C6 A000---0x01C6 AFFF	4K

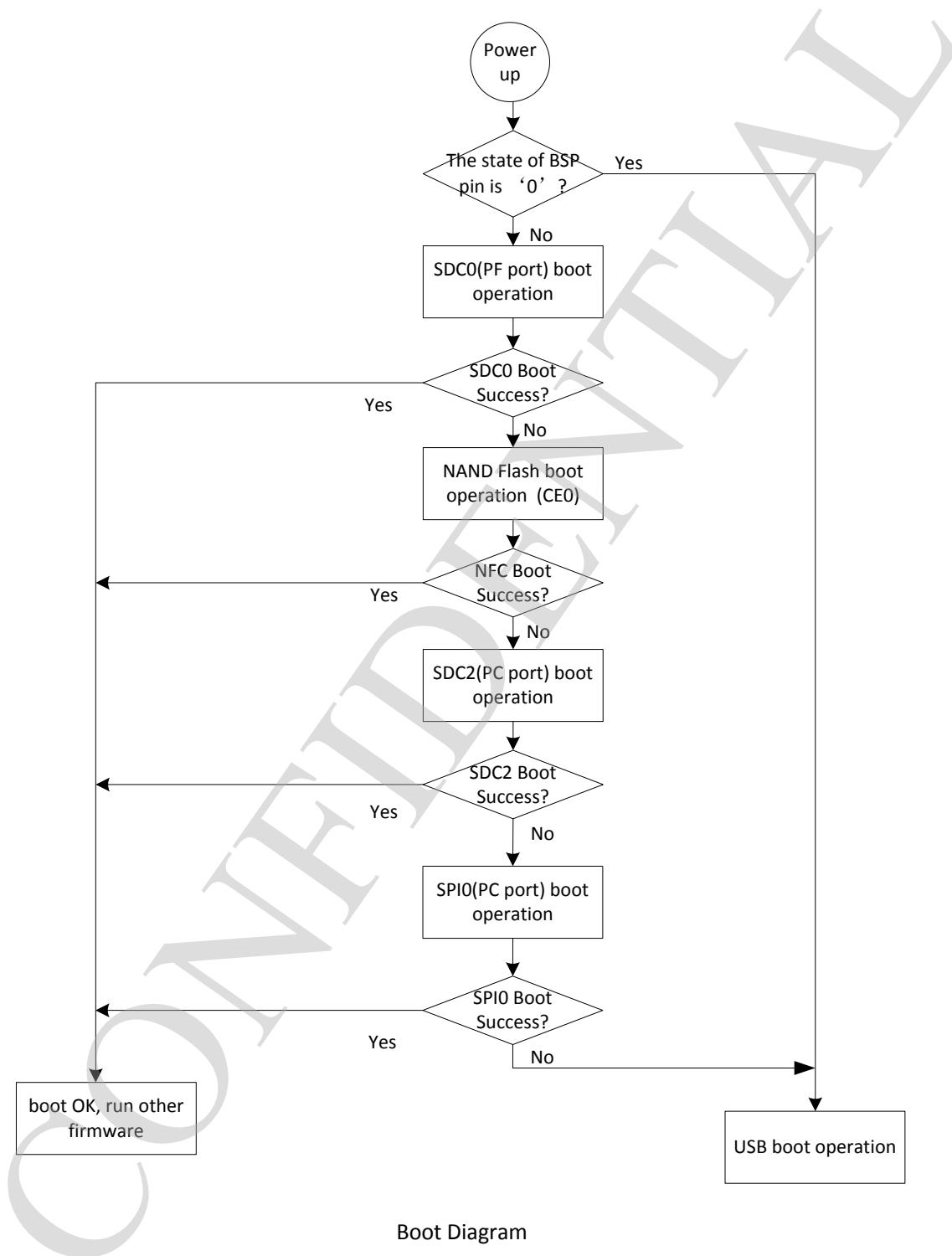
/	0x01C6 B000---0x01C6 BFFF	4K
SCU REGISTERS	0x01C8 0000	/
MIPI DSIO	0x01CA 0000---0x01CA 0FFF	4K
MIPI DSIO-PHY	0x01CA 1000---0x01CA 1FFF	4K
CSI	0x01CB 0000---0x01CB 0FFF	4K
DEFE	0x01E0 0000---0x01E1 FFFF	128K
DEBE	0x01E6 0000---0x01E6 FFFF	64K
DRC	0x01E7 0000---0x01E7 FFFF	64K
RTC	0x01F0 0000---0x01F0 03FF	1K
/	0x01F0 0400---0x01F0 07FF	1K
/	0x01F0 0800---0x01F0 0BFF	1K
/	0x01F0 0C00---0x01F0 0FFF	1K
/	0x01F0 1000---0x01F0 13FF	1K
/	0x01F0 1400---0x01F0 17FF	1K
/	0x01F0 1C00---0x01F0 1FFF	1K
/	0x01F0 2400---0x01F0 27FF	1K
/	0x01F0 2800---0x01F0 2BFF	1K
/	0x01F0 2C00---0x01F0 2FFF	1K
/	0x01F0 3400---0x01F0 37FF	1K
/	0x01F0 3800---0x01F0 3BFF	1K
/	0x3F50 0000---0x3F51 FFFF	128K
TSGEN RO	0x3F50 6000---0x3F50 6FFF	4K
TSGEN CTRL	0x3F50 7000---0x3F50 7FFF	4K
DDR	0x4000 0000---0xBFFF FFFF	2G
BROM	0xFFFF 0000—0xFFFF 7FFF	32K

3.2 Boot System

3.2.1 Overview

The dual-core A23 processor supports system boot from five devices: it can boot sequentially from NAND Flash, eMMC NAND, SPI Nor Flash, SD card (SDC 0/2) and USB, but if you want to boot the system directly from USB, the UBOOT_SEL pin pulled up by internal 50K resistor in normal state can be set to low level.

3.2.2 Boot Diagram



Boot Diagram

3.3 CCU

3.3.1 Overview

The Clock Control Unit (CCU) is made up of 9 PLLs and 1 MIPI in PLL macro, a main oscillator, an on-chip RC oscillator that must be in the range of 466.9KHz ~ 867.1KHz, and a 32768Hz low-power oscillator.

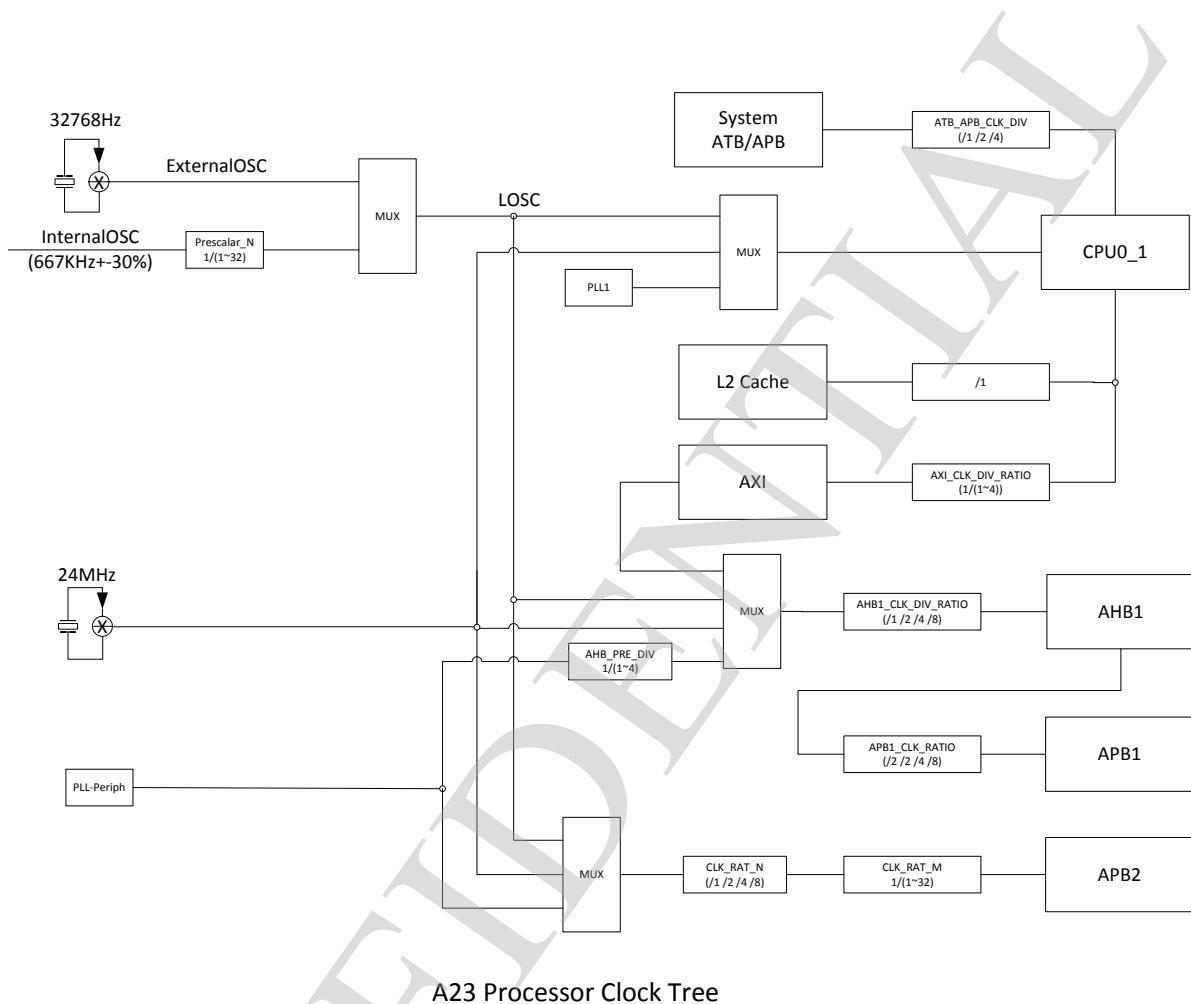
- CPU Clock
- AHB Clock
- APB Clock
- Special Clock

A23 integrates two crystal oscillators: a 24MHz crystal is mandatory and provides clock source for PLLs and main digital blocks; a 32768Hz oscillator is used only to provide a low power, accurate reference for RTC.

It features:

- 9 PLLs, a MIPI in PLL macro, a main oscillator, an on-chip RC oscillator and a 32768Hz low-power oscillator
- PLL_CPU is for the clock of CPU0/1
- Clock configuration for corresponding modules
- Software-controlled clock gating
- Software-controlled reset for corresponding module

3.3.2 Clock Tree Diagram



3.3.3 CCU Register List

Module Name	Base Address
CCU	0x01c20000

Register Name	Offset	Description
PLL_CPU_CFG_REG	0x0000	PLL Control Register(CPU0_1 PLL)
PLL_AUDIO_CFG_REG	0x0008	PLL Control Register (Audio PLL)
PLL_VIDEO_CFG_REG	0x0010	PLL Control Register (Video PLL)
PLL_VE_CFG_REG	0x0018	PLL Control Register (VE PLL)
PLL_DDR_CFG_REG	0x0020	PLL Control Register (DDR PLL)
PLL_PERIPH_CFG_REG	0x0028	PLL Control Register (Peripheral PLL)
PLL_GPU_CFG_REG	0x0038	PLL Control Register (GPU PLL)
MIPI_PLL_CFG_REG	0x0040	MIPI_PLL Control Register
PLL_HSIC_CFG_REG	0x0044	PLL Control Register(PLL HSIC)
PLL_DE_CFG_REG	0x0048	PLL Control Register(PLL DE)
CPU_AXI_CFG_REG	0x0050	CPU /AXI CLK Ratio Register
AHB1_APB1_CFG_REG	0x0054	AHB1/APB1 CLK Ratio Register
APB2_CLK_DIV_REG	0x0058	APB2 Clock Divider Register
AHB1_GATING_REG0	0x0060	AHB1 Module Clock Gating Register 0
AHB1_GATING_REG1	0x0064	AHB1 Module Clock Gating Register 1
APB1_GATING_REG	0x0068	APB1 Module Clock Gating Register
APB2_GATING_REG	0x006C	APB2 Module Clock Gating Register
NAND_SCLK_CFG_REG	0x0080	NAND Clock Register
SD0_CLK_REG	0x0088	SD0 Clock Register
SD1_CLK_REG	0x008C	SD1 Clock Register
SD2_CLK_REG	0x0090	SD2 Clock Register

SPI0_CLK_REG	0x00A0	SPI0 Clock Register
SPI1_CLK_REG	0x00A4	SPI1 Clock Register
/	0x00A8	/
/	0x00AC	/
DAUDIO0_CLK_REG	0x00B0	Digital Audio0 Clock Register
DAUDIO1_CLK_REG	0x00B4	Digital Audio1 Clock Register
USBPHY_CFG_REG	0x00CC	USBPHY Configuration Register
/	0x00E0	/
DRAM_CFG_REG	0x00F4	DRAM Configuration Register
DRAM_GATING_REG	0x0100	DRAM Clock Gating Register
BE_SCLK_CFG_REG	0x0104	Display Engine Back-End Clock Configuration Register
FE_CLK_REG	0x010C	Display Engine Front-End Clock Register
/	0x0114	/
LCD_CH0_CLK_REG	0x0118	LCD Channel0 Clock Register
LCD_CH1_CLK_REG	0x012C	LCD Channel1 Clock Register
/	0x0130	/
CSI_CLK_REG	0x0134	CSI Clock Register
VE_CLK_REG	0x013C	Video Engine Clock Register
AUDIO_CODEC_CLK_REG	0x0140	Audio Codec Clock Configuration Register
AVS_CLK_REG	0x0144	AVS Clock Register
MBUS_SCLK_CFG_REG	0x015C	/
MIPI_DSI_CLK_REG	0x0168	Mipi_Dsi Clock Register
DRC_SCLK_CFG_REG	0x0180	DRC Clock Configuration Register
GPU_CORE_CLK_REG	0x01A0	GPU Core Clock Configuration Register
GPU_MEM_CLK_REG	0x01A4	/
GPU_HYD_CLK_REG	0x01A8	/
ATS_CLK_REG	0x01B0	ATS Clock Configuration Register

PLL_LOCK_CFG_REG	0x0200	PLL(Except PLL_CPU) Lock Time Control Register
PLL_CPU_LOCK_CFG_REG	0x0204	PLL_CPU Lock Time Control Register
PLL_CPU_BIAS_REG	0x0220	PLL_CPU Bias Register
PLL_AUDIO_BIAS_REG	0x0224	PLL_Audio Bias Register
PLL_VIDEO_BIAS_REG	0x0228	PLL_Video Bias Register
PLL_VE_BIAS_REG	0x022C	PLL_VE Bias Register
PLL_DDR_BIAS_REG	0x0230	PLL_DDR Bias Register
PLL_PERIPH_BIAS_REG	0x0234	PLL_PERIPH Bias Register
PLL_GPU_BIAS_REG	0x023C	PLL_GPU Bias Register
MIPI_PLL_BIAS_REG	0x0240	MIPI_PLL Bias Register
PLL_HSIC_BIAS_REG	0x0244	PLL_HSIC Bias Register
PLL_DE_BIAS_REG	0x0248	PLL_DE Bias Register
PLL_CPU_TUN_REG	0x0250	PLL_CPU Tuning Register
PLL_DDR_TUN_REG	0x0260	PLL_DDR Tuning Register
MIPI_PLL_TUN_REG	0x0270	MIPI_PLL Tuning Register
PLL_CPU_PAT_CFG_REG	0x0280	PLL_CPU-PATTERN Control Register
PLL_AUDIO_PAT_CFG_REG	0x0284	PLL_AUDIO-PATTERN Control Register
PLL_VIDEO_PAT_CFG_REG	0x0288	PLL_VIDEO-PATTERN Control Register
PLL_VE_PAT_CFG_REG	0x028C	PLL_VE-PATTERN Control Register
PLL_DDR_PAT_CFG_REG	0x0290	PLL_DDR-PATTERN Control Register
PLL_GPU_PAT_CFG_REG	0x029C	PLL_GPU-PATTERN Control Register
MIPI_PLL_PAT_CFG_REG	0x02A0	MIPI_PLL PATTERN Control Register
PLL_HSIC_PAT_CFG_REG	0x02A4	PLL_HSIC PATTERN Control Register
PLL_DE_PAT_CFG_REG	0x02A8	PLL_DE-PATTERN Control Register
AHB1_RST_REG0	0x02C0	AHB1 Module Software Reset Register0
AHB1_RST_REG1	0x02C4	AHB1 Module Software Reset Register1
AHB1_RST_REG2	0x02C8	AHB1 Module Software Reset Register2

APB1_RST_REG	0x02D0	APB1 Module Software Reset Register
APB2_RST_REG	0x02D8	APB2 Module Software Reset Register

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3.3.4 CCU Register Description

PLL-CPU0_1 REGISTER (DEFAULT: 0X00001000)

Offset: 0x00			Register Name: PLL_CPU_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>PLL_ENABLE.</p> <p>0: Disable, 1: Enable.</p> <p>The PLL output= (24MHz*N*K)/(M*P).</p> <p>The PLL output is for the CPU0_1 CLK.</p> <p>Note: the PLL output clock must be in the range of 200MHz~2.6GHz, Its default is 408MHz.</p>
30:29	/	/	/
28	R	0x0	<p>LOCK</p> <p>0: unlocked</p> <p>1: locked (It indicates that the PLL has been stable.)</p>
27:25	/	/	/
24	R/W	0x0	<p>CPU_SIGMA_DELTA_EN.</p> <p>0: disable.</p> <p>1: enable.</p>
23:18	/	/	/
17:16	R/W	0x0	<p>PLL_OUT_EXT_DIVP</p> <p>PLL Output external divider P</p> <p>00: /1</p> <p>01: /2</p> <p>10: /4</p> <p>11: /</p>

15:13	/	/	/
12:8	R/W	0x10	<p>PLL_FACTOR_N</p> <p>PLL Factor N.</p> <p>Factor=0, N=1;</p> <p>Factor=1, N=2;</p> <p>Factor=2, N=3;</p> <p>.....</p> <p>Factor=31,N=32</p>
7:6	/	/	/
5:4	R/W	0x0	<p>PLL_FACTOR_K.</p> <p>PLL Factor K.(K=Factor + 1)</p> <p>The range is from 1 to 4.</p>
3:2	/	/	/
1:0	R/W	0x0	<p>PLL_FACTOR_M.</p> <p>PLL Factor M. (M=Factor + 1)</p> <p>The range is from 1 to 4.</p>

PLL-AUDIO REGISTER (DEFAULT:0X00035514)

Offset: 0x08			Register Name: PLL_AUDIO_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>PLL_ENABLE.</p> <p>0: Disable, 1: Enable.</p> <p>The PLL is for Audio.</p> <p>The PLL Output = $24\text{MHz} * N / (P * M)$.</p> <p>Note: In the Clock Control Module, The PLL_AUDIO(8X) Output = $24\text{MHz} * N * 2 / M$.</p> <p>the PLL output clock must be in the range of 20MHz~200MHz,</p> <p>Its default is 24.571MHz.</p>

30:29	/	/	/
28	R	0x0	<p>LOCK.</p> <p>0: unlocked</p> <p>1: locked (It indicates that the PLL has been stable.)</p>
27:25	/	/	/
24	R/W	0x0	<p>PLL_SDM_EN.</p> <p>0: Disable.</p> <p>1: Enable, In this case, the PLL_FACTOR_N only low 4 bits are valid (N: The range is from 1 to 16).</p>
23:20	/	/	/
19:16	R/W	0x3	<p>PLL_POSTDIV_P.</p> <p>Post-div factor (P= Factor+1)</p> <p>The range is from 1 to 16.</p>
15	/	/	/
14:8	R/W	0x55	<p>PLL_FACTOR_N.</p> <p>PLL Factor N.</p> <p>Factor=0, N=1;</p> <p>Factor=1, N=2;</p> <p>.....</p> <p>Factor=127, N=128;</p>
7:5	/	/	/
4:0	R/W	0x14	<p>PLL_PREDIV_M.</p> <p>Pre-div factor(M = Factor+1).</p> <p>The range is from 1 to 32</p>

PLL-VIDEO REGISTER (DEFAULT:0X03006207)

Offset: 0x10		Register Name: PLL_VIDEO_CFG_REG	
Bit	Read/ Write	Default /Hex	Description

31	R/W	0x0	<p>PLL_ENABLE.</p> <p>0: Disable, 1: Enable.</p> <p>In the integer mode,</p> <p>The PLL output = $(24\text{MHz} \times N)/M$.</p> <p>In the fractional mode, the PLL output is select by bit 25.</p> <p>Note: In the Clock Control Module, PLL(1X) output=PLL while PLL(2X) output=PLL * 2.</p> <p>the PLL output clock must be in the range of 30MHz~600MHz,</p> <p>Its default is 297MHz.</p>
30	R/W	0x0	<p>PLL_MODE.</p> <p>0: Manual Mode.</p> <p>1: Auto Mode (Controlled by DE).</p>
29	/	/	/
28	R	0x0	<p>LOCK.</p> <p>0: unlocked.</p> <p>1: locked (It indicates that the PLL has been stable.)</p>
27:26	/	/	/
25	R/W	0x1	<p>FRAC_CLK_OUT.</p> <p>PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL=1.</p> <p>0: pllout=270MHz;</p> <p>1: pllout=297MHz.</p>
24	R/W	0x1	<p>PLL_MODE_SEL.</p> <p>0: Fractional mode.</p> <p>1: Integer mode.</p> <p>Note: When in Fractional mode, the pre-divider M should be set to 0.</p>
23:21	/	/	/
20	R/W	0x0	<p>PLL_SDM_EN.</p> <p>0: Disable, 1: Enable.</p>

19:15	/	/	/
14:8	R/W	0x62	<p>PLL_FACTOR_N.</p> <p>PLL Factor N.</p> <p>Factor=0, N=1;</p> <p>Factor=1, N=2;</p> <p>Factor=2, N=3;</p> <p>.....</p> <p>Factor=127,N=128</p>
7:4	/	/	/
3:0	R/W	0x7	<p>PLL_PREDIV_M.</p> <p>PLL pre-divider(M = Factor+1).</p> <p>The range is from 1 to 16.</p>

PLL-VE REGISTER (DEFAULT:03006207)

Offset: 0x18			Register Name: PLL_VE_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>PLL_ENABLE.</p> <p>0: Disable, 1: Enable.</p> <p>In the integer mode, The PLL output = (24MHz*N)/M.</p> <p>In the fractional mode, the PLL output is select by bit 25.</p> <p>Note: The PLL output clock must be in the range of 30MHz~600MHz, Its default is 297MHz.</p>
30:29	/	/	/
28	R	0x0	<p>LOCK</p> <p>0: unlocked</p> <p>1: locked (It indicates that the PLL has been stable.)</p>
27:26	/	/	/
25	R/W	0x1	FRAC_CLK_OUT.

			PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL =1. 0: pllout=270MHz; 1: pllout=297MHz.
24	R/W	1	PLL_MODE_SEL. 0: Fractional mode. 1: Integer mode. Note: When in Fractional mode, the pre-divider M should be set to 0.
23:21	/	/	/
20	R/W	0x0	PLL_SDM_EN. 0: Disable, 1: Enable.
19:15	/	/	/
14:8	R/W	0x62	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3 Factor=31,N=32 ... Factor=127,N=128
7:4	/	/	/. /.
3:0	R/W	0x7	PLL_PREDIV_M. PLL pre-divider (M = Factor+1). The range is from 1 to 16.

PLL-DDR REGISTER (DEFAULT:0X00001000)

Offset: 0x20		Register Name: PLL_DDR_CFG_REG	
Bit	Read/	Default	Description

	Write	/Hex	
31	R/W	0x0	<p>PLL_ENABLE.</p> <p>0: Disable, 1: Enable.</p> <p>Set bit20 to validate the PLL after this bit is set to 1.</p> <p>the PLL_DDR output for SDRAM = (24MHz*N*K)/M.</p> <p>Note: the PLL output clock must be in the range of 200MHz~2.6GHz, Its default is 408MHz.</p>
30:29	/	/	/
28	R	0x0	<p>LOCK</p> <p>0: unlocked</p> <p>1: locked (It indicates that the PLL has been stable.)</p>
27:25	/	/	/
24	R/W	0x0	<p>SDRAM_SIGMA_DELTA_EN.</p> <p>0: Disable.</p> <p>1: Enable.</p>
23:21	/	/	/
20	R/W	0x0	<p>SDRPLL_UPD.</p> <p>SDRPLL Configuration Update.</p> <p>Note: when PLL has changed, this bit should be set to 1 to validate PLL, otherwise the change is invalid. It will be auto cleared after the PLL is valid.</p> <p>0: No effect.</p> <p>1: To validate PLL.</p>
19:13	/	/	/
12:8	R/W	0x10	<p>PLL_FACTOR_N.</p> <p>PLL Factor N.</p> <p>Factor=0, N=1;</p> <p>Factor=1, N=2;</p> <p>Factor=2, N=3;</p>

		 Factor=31,N=32
7:6	/	/	/
5:4	R/W	0x0	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x0	PLL_FACTOR_M. PLL Factor M.(M = Factor + 1) The range is from 1 to 4.

PLL-PERIPHERAL REGISTER (DEFAULT:0X00041811)

Offset: 0x28			Register Name: PLL_PERIPH_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	PLL_ENABLE. 0: Disable, 1: Enable. The PLL Output = 24MHz*N*K/2. Note: The PLL Output should be fixed to 600MHz, it is not recommended to vary this value arbitrarily. In the Clock Control Module, PLL(2X) output= PLL*2 = 24MHz*N*K. The PLL output clock must be in the range of 200MHz~1.8GHz, Its default is 600MHz.
30:29	/	/	/
28	R	0x0	LOCK. 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27:26	/	/	/
25	R/W	0x0	PLL_BYPASS_EN.

			PLL Output Bypass Enable. 0: Disable, 1: Enable. If the bypass is enabled, the PLL output is 24MHz.
24	R/W	0x0	PLL_CLK_OUT_EN. PLL clock output enable.(Just for the SATA Phy) 0: Disable, 1: Enable.
23:19	/	/	/
18	R/W	0x1	PLL_24M_OUT_EN. PLL 24MHz output enable. 0: Disable, 1: Enable. When 25MHz crystal used, this PLL can output 24MHz.
17:16	R/W	0x0	PLL_24M_POST_DIV. PLL 24M output clock post divider (when 25MHz crystal used). 1/2/3/4.
15:13	/	/	/
12:8	R/W	0x18	PLL_FACTOR_N. PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3; Factor=31,N=32
7:6	/	/	/
5:4	R/W	0x1	PLL_FACTOR_K. PLL Factor K.(K=Factor + 1) The range is from 1 to 4.
3:2	/	/	/
1:0	R/W	0x1	/

PLL-GPU REGISTER (DEFAULT:0X03006207)

Offset: 0x38			Register Name: PLL_GPU_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>PLL_GPU_ENABLE.</p> <p>0: Disable, 1: Enable.</p> <p>In the integer mode, The PLL_GPU output= $(24\text{MHz} \times N) / M$.</p> <p>In the fractional mode, the PLL_GPU output is select by bit 25.</p> <p>Note: The PLL output clock must be in the range of 30MHz~600MHz, Its default is 297MHz.</p>
30:29	/	/	/
28	R	0x0	<p>LOCK</p> <p>0: unlocked</p> <p>1: locked (It indicates that the PLL has been stable.)</p>
27:26	/	/	/
25	R/W	0x1	<p>FRAC_CLK_OUT.</p> <p>PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL =1.</p> <p>0: pllout=270MHz;</p> <p>1: pllout=297MHz.</p>
24	R/W	0x1	<p>PLL_MODE_SEL.</p> <p>0: Fractional mode.</p> <p>1: Integer mode.</p> <p>Note: When in Fractional mode, the pre-divider M should be set to 0.</p>
23:21	/	/	/
20	R/W	0x0	<p>PLL_SDM_EN.</p> <p>0: Disable, 1: Enable.</p>
19:15	/	/	/

14:8	R/W	0x62	PLL_FACTOR_N PLL Factor N. Factor=0, N=1; Factor=1, N=2; Factor=2, N=3 Factor=127,N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL pre-divider (M = Factor+1). The range is from 1 to 16.

MIPI_PLL CONTROL REGISTER (DEFAULT:0X000000502)

Offset: 0x40			Register Name: MIPI_PLL_Cfg_Reg0
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	MIPI_PLL_ENABLE. 0: Disable, 1: Enable. The PLL output= (PLL_SRC*N*K)/M when VFB_SEL=0 (MIPI mode); When VFB_SEL=1, the PLL output is depend on these bits: sint_frac,sdiv2,s6p25_7p5 ,pll_feedback_div.
30:29	/	/	/
28	R	0x0	LOCK. 0: unlocked 1: locked (It indicates that the PLL has been stable.)
27	R/W	0x0	SINT_FRAC. When VFB_SEL=1, PLL mode control, otherwise no meaning. 0: Integer mode 1: Fractional mode

26	R/W	0x0	SDIV2. PLL clock output when VFB_SEL=1; no meaning when VFB_SEL =0 0: PLL output 1: PLL output X2.
25	R/W	0x0	S6P25_7P5. PLL Output is selected by this bit when VFB_SEL=1 and SINT_FRAC=1, otherwise no meaning. 0: pllout=pllinput*6.25 1: pllout=pllinput*7.5.
24	/	/	/
23	R/W	0	LDO1_EN. On-chip LDO1 Enable.
22	R/W	0	LDO2_EN. On-chip LDO2 Enable.
21	R/W	0	PLL_SRC. PLL Source Select. 0: VIDEO PLL 1: /.
20	R/W	0x0	PLL_SDM_EN. 0: Disable, 1: Enable.
19:18	/	/	/
17	R/W	0x0	PLL_FEEDBACK_DIV. PLL feed-back divider control. PLL clock output when VFB_SEL=1; no meaning when VFB_SEL =0 0:divided by 5 1:divided by 7
16	R/W	0x0	VFB_SEL. 0: MIPI mode(N, K, M valid) 1:/

15:12	/	/	/
11:8	R/W	0x5	<p>PLL_FACTOR_N</p> <p>PLL Factor N.</p> <p>Factor=0, N=1;</p> <p>Factor=1, N=2;</p> <p>.....</p> <p>Factor=15, N=16</p>
7:6	/	/	/
5:4	R/W	0x0	<p>PLL_FACTOR_K.</p> <p>PLL Factor K.(K=Factor + 1)</p> <p>The range is from 1 to 4.</p>
3:0	R/W	0x2	<p>PLL_PRE_DIV_M.</p> <p>PLL Pre-divider Factor (M = Factor+1).</p> <p>The range is from 1 to 16.</p>

PLL REGISTER HSIC PLL(DEFAULT:0X03001300)

Offset: 0x44			Register Name: PLL9_HSIC_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>PLL9_ENABLE.</p> <p>0: Disable, 1: Enable.</p> <p>In the integer mode, The PLL9 output= (24MHz*N)/M.</p> <p>In the fractional mode, the PLL9 output is select by bit 25.</p> <p>Note: The PLL output clock must be in the range of 30MHz~600MHz, Its default is 480MHz.</p>
30:29	/	/	/
28	R	0x0	<p>LOCK</p> <p>0: unlocked</p> <p>1: locked (It indicates that the PLL has been stable.)</p>

27:26	/	/	/
25	R/W	0x1	<p>FRAC_CLK_OUT.</p> <p>PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL =1.</p> <p>0: pllout=270MHz;</p> <p>1: pllout=297MHz.</p>
24	R/W	0x1	<p>PLL_MODE_SEL.</p> <p>0: Fractional mode.</p> <p>1: Integer mode.</p> <p>Note: When in Fractional mode, the pre-divider M should be set to 0.</p>
23:21	/	/	/
20	R/W	0x0	<p>PLL_SDM_EN.</p> <p>0: Disable, 1: Enable.</p>
19:15	/	/	/
14:8	R/W	0x13	<p>PLL_FACTOR_N</p> <p>PLL Factor N.</p> <p>Factor=0, N=1;</p> <p>Factor=1, N=2;</p> <p>Factor=2, N=3</p> <p>.....</p> <p>Factor=0x7F, N=128</p>
7:4	/	/	/
3:0	R/W	0x0	<p>PLL_PRE_DIV_M.</p> <p>PLL pre-divider (M = Factor+1).</p> <p>The range is from 1 to 16.</p>

PLL-DE REGISTER(DEFAULT:0X03006207)

Offset: 0x48		Register Name: PLL_DE_CFG_REG	
Bit	Read/	Default	Description

	Write	/Hex	
31	R/W	0x0	<p>PLL_ENABLE.</p> <p>0: Disable, 1: Enable.</p> <p>In the integer mode, The PLL output= $(24\text{MHz} \times N)/M$.</p> <p>In the fractional mode, the PLL output is select by bit 25.</p> <p>Note: The PLL output clock must be in the range of 30MHz~600MHz, Its default is 297MHz.</p>
30:29	/	/	/
28	R	0x0	<p>LOCK</p> <p>0: unlocked</p> <p>1: locked (It indicates that the PLL has been stable.)</p>
27:26	/	/	/
25	R/W	0x1	<p>FRAC_CLK_OUT.</p> <p>PLL clock output when PLL_MODE_SEL=0(PLL_PREDIV_M factor must be set to 0); no meaning when PLL_MODE_SEL =1.</p> <p>0: plfout=270MHz;</p> <p>1: plfout=297MHz.</p>
24	R/W	0x1	<p>PLL_MODE_SEL.</p> <p>0: Fractional mode.</p> <p>1: Integer mode.</p> <p>Note: When in Fractional mode, the pre-divider M should be set to 0.</p>
23:21	/	/	/
20	R/W	0x0	<p>PLL_SDM_EN.</p> <p>0: Disable, 1: Enable.</p>
19:15	/	/	/
14:8	R/W	0x62	<p>PLL_FACTOR_N</p> <p>PLL Factor N.</p> <p>Factor=0, N=1;</p> <p>Factor=1, N=2;</p>

			Factor=2, N=3 Factor=0x7F,N=128
7:4	/	/	/
3:0	R/W	0x7	PLL_PRE_DIV_M. PLL pre-divider (M = Factor+1). The range is from 1 to 16.

CPU /AXI CLOCK RATIO REGISTER (DEFAULT: 0X00010000)

Offset: 0x50			Register Name: CPU_AXI_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31:18	/	/	/
17:16	R/W	0x1	CPU_CLK_SRC_SEL. CPU0/1 Clock Source Select. 00: LOSC 01: OSC24M 10: PLL_CPU 11: PLL_CPU If the clock source is changed, at most to wait for 8 present running clock cycles.
15:10	/	/	/
9:8	R/W	0x0	CPU_APB_CLK_DIV. 00: /1 01: /2 1x: /4 Note: System APB clock source is CPU clock source.
7:3	/	/	/
2:0	R/W	0x0	AXI_CLK_DIV_RATIO.

			<p>AXI Clock divide ratio.</p> <p>AXI Clock source is CPU clock source.</p> <p>000: /1</p> <p>001: /2</p> <p>010: /3</p> <p>011: /4</p> <p>1xx: /4</p>
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AHB1/APB1 CLOCK RATIO REGISTER (DEFAULT: 0X00001010)

Offset: 0x54			Register Name: AHB1_APB1_CFG_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 4	/	/	/
13:1 2	R/W	0x1	<p>AHB1_CLK_SRC_SEL.</p> <p>00: LOSC</p> <p>01: OSC24M</p> <p>10: AXI</p> <p>11: PLL_PERIPH/ AHB1_PRE_DIV.</p>
11:1 0	/	/	/
9:8	R/W	0x0	<p>APB1_CLK_RATIO.</p> <p>APB1 Clock divide ratio. APB1 clock source is AHB1 clock.</p> <p>00: /2</p> <p>01: /2</p> <p>10: /4</p> <p>11: /8</p>
7:6	R/W	0x0	<p>AHB1_PRE_DIV</p> <p>AHB1 clock pre-divide ratio</p>

			00: /1 01: /2 10: /3 11: /4
5:4	R/W	0x1	AHB1_CLK_DIV_RATIO. AHB1 Clock divide ratio. 00: /1 01: /2 10: /4 11: /8
3:0	/	/	/

APB2 CLOCK DIVIDE RATIO REGISTER (DEFAULT: 0X01000000)

Offset: 0x58			Register Name: APB2_CLK_DIV_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 6	/	/	/
25:2 4	R/W	0x1	APB2_CLK_SRC_SEL. APB2 Clock Source Select 00: LOSC 01: OSC24M 10: PLL_PERIPH 11: PLL_PERIPH This clock is used for some special module apbclk(UART、TWI). Because these modules need special clock rate even if the apb1clk changed.
23:1 8	/	/	/
17:1	R/W	0x0	CLK_RAT_N

6			Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n . The divider is 1/2/4/8.
15:5	/	/	/
4:0	R/W	0x0	CLK_RAT_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 32.

AHB1 MODULE CLOCK GATING REGISTER 0(DEFAULT: 0X00000000)

Offset: 0x60			Register Name: AHB1_GATING_REG0
Bit	Read/Writ e	Default/H ex	Description
31:3 0	/	/	/
29	R/W	0x0	Gating AHB Clock for USB OHCI(0: mask, 1: pass).
27:2 8	/	/	/
26	R/W	0x0	Gating AHB Clock for USB EHCI (0: mask, 1: pass).
25	/	/	/
24	R/W	0x0	USB_OTG_AHB_GATING. Gating AHB Clock for USB-OTG(0: mask, 1: pass).
23:2 2	/	/	/
21	R/W	0x0	SPI1_AHB_GATING. Gating AHB Clock for SPI1(0: mask, 1: pass).
20	R/W	0x0	SPI0_AHB_GATING. Gating AHB Clock for SPI0(0: mask, 1: pass).
19	R/W	0x0	HSTMR_AHB_GATING. Gating AHB Clock for High Speed Timer (0: mask, 1: pass).

18:1 5	/	/	/
14	R/W	0x0	SDRAM_AHB_GATING. Gating AHB Clock for SDRAM(0: mask, 1: pass).
13	R/W	0x0	NAND_AHB_GATING. Gating AHB Clock for NAND(0: mask, 1: pass).
12:1 1	/	/	/
10	R/W	0x0	SD2_AHB_GATING. Gating AHB Clock for SD/MMC2(0: mask, 1: pass).
9	R/W	0x0	SD1_AHB_GATING. Gating AHB Clock for SD/MMC1(0: mask, 1: pass).
8	R/W	0x0	SD0_AHB_GATING. Gating AHB Clock for SD/MMC0(0: mask, 1: pass).
7	/	/	/
6	R/W	0x0	DMA_AHB_GATING. Gating AHB Clock for DMA(0: mask, 1: pass).
5:2	/	/	/
1	R/W	0x0	MIPIDSI_AHB_GATING. Gating AHB Clock for MIPI DSI(0: mask, 1: pass).
0	/	/	/

AHB1 MODULE CLOCK GATING REGISTER 1(DEFAULT: 0X00000000)

Offset: 0x64			Register Name: AHB1_GATING_REG1
Bit	Read/Writ e	Default/H ex	Description
31:2 6	/	/	/
25	R/W	0x0	DRC_AHB_GATING.

			Gating AHB Clock for DRC (0: mask, 1: pass).
24:2 3	/	/	/
22	R/W	0x0	SPINLOCK_AHB_GATING. Gating AHB Clock for SPINLOCK (0: mask, 1: pass).
21	R/W	0x0	/
20	R/W	0x0	GPU_AHB_GATING. Gating AHB Clock for GPU (0: mask, 1: pass).
19:1 5	/	/	/
14	R/W	0x0	FE_AHB_GATING. Gating AHB Clock for DE-FE (0: mask, 1: pass).
13			
12	R/W	0x0	BE_AHB_GATING. Gating AHB Clock for DE-BE (0: mask, 1: pass).
11:9	/	/	/
8	R/W	0x0	CSI_AHB_GATING. Gating AHB Clock for CSI (0: mask, 1: pass).
7:5	/	/	/
4	R/W	0x0	LCD_AHB_GATING. Gating AHB Clock for LCD (0: mask, 1: pass).
3:1	/	/	/
0	R/W	0x0	VE_AHB_GATING. Gating AHB Clock for VE (0: mask, 1: pass).

APB1 MODULE CLOCK GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x68		Register Name: APB1_GATING_REG	
Bit	Read/Writ e	Default/H ex	Description

31:1 4	/	/	/.
13	R/W	0x0	DAUDIO1_APB_GATING. Gating APB Clock for DAUDIO 1 (0: mask, 1: pass).
12	R/W	0x0	DAUDIO0_APB_GATING. Gating APB Clock for DAUDIO 0 (0: mask, 1: pass).
11:6	/	/	/
5	R/W	0x0	PIO_APB_GATING. Gating APB Clock for PIO (0: mask, 1: pass).
4:1	/	/	/
0	R/W	0x0	ADDA_D_APB_GATING. Gating APB Clock for ADDA_D(0: mask, 1: pass).

APB2 MODULE CLOCK GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x6C			Register Name: APB2_GATING_REG
Bit	Read/ Write	Default /Hex	Description
31:21	/	/	/.
20	R/W	0x0	UART4_APB_GATING. Gating APB Clock for UART4(0: mask, 1: pass).
19	R/W	0x0	UART3_APB_GATING. Gating APB Clock for UART3(0: mask, 1: pass).
18	R/W	0x0	UART2_APB_GATING. Gating APB Clock for UART2(0: mask, 1: pass).
17	R/W	0x0	UART1_APB_GATING. Gating APB Clock for UART1(0: mask, 1: pass).
16	R/W	0x0	UART0_APB_GATING. Gating APB Clock for UART0(0: mask, 1: pass).
15:3	/	/	/

2	R/W	0x0	TWI2_APB_GATING. Gating APB Clock for TWI2(0: mask, 1: pass).
1	R/W	0x0	TWI1_APB_GATING. Gating APB Clock for TWI1(0: mask, 1: pass).
0	R/W	0x0	TWI0_APB_GATING. Gating APB Clock for TWI0(0: mask, 1: pass).

NAND CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x80			Register Name: NAND_SCLK_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n . The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M

			Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.
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Note: In practical applications, the module clock frequency is always switched off.

SD/MMC 0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x88			Register Name: SDO_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH 10: / 11: /.
23	/	/	/
22:20	R/W	0x0	SAMPLE_CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n . The divider is 1/2/4/8.

15:11	/	/	/
10:8	R/W	0x0	<p>OUTPUT_CLK_PHASE_CTR.</p> <p>Output Clock Phase Control.</p> <p>The output clock phase delay is based on the number of source clock that is from 0 to 7.</p>
7:4	/	/	/
3:0	R/W	0x0	<p>CLK_DIV_RATIO_M.</p> <p>Clock divide ratio (m)</p> <p>The pre-divided clock is divided by (m+1). The divider is from 1 to 16.</p>

SD/MMC 1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x8C			Register Name: SD1_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>SCLK_GATING.</p> <p>Gating Special Clock(Max Clock = 200MHz)</p> <p>0: Clock is OFF</p> <p>1: Clock is ON</p> <p>This special clock = Clock Source/Divider N/Divider M.</p>
30:26	/	/	/
25:24	R/W	0x0	<p>CLK_SRC_SEL.</p> <p>Clock Source Select</p> <p>00: OSC24M</p> <p>01: PLL_PERIPH</p> <p>10: /</p> <p>11: /.</p>
23	/	/	/
22:20	R/W	0x0	<p>CLK_PHASE_CTR.</p> <p>Sample Clock Phase Control.</p>

			The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n . The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

SD/MMC 2 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x90			Register Name: SD2_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M

			01: PLL_PERIPH 10: / 11: /.
23	/	/	/
22:20	R/W	0x0	CLK_PHASE_CTR. Sample Clock Phase Control. The sample clock phase delay is based on the number of source clock that is from 0 to 7.
19:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n . The divider is 1/2/4/8.
15:11	/	/	/
10:8	R/W	0x0	OUTPUT_CLK_PHASE_CTR. Output Clock Phase Control. The output clock phase delay is based on the number of source clock that is from 0 to 7.
7:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

SPI0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xA0			Register Name: SPI0_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF

			1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 00: OSC24M 01: PLL_PERIPH 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n . The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

SPI1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xA4			Register Name: SPI1_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider N/Divider M.
30:26	/	/	/
25:24	R/W	0x0	CLK_SRC_SEL.

			Clock Source Select 00: OSC24M 01: PLL_PERIPH 10: / 11: /.
23:18	/	/	/
17:16	R/W	0x0	CLK_DIV_RATIO_N. Clock pre-divide ratio (n) The select clock source is pre-divided by 2^n . The divider is 1/2/4/8.
15:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

DAUDIO 0 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xB0			Register Name: DAUDIO0_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock(Max Clock = 200MHz) 0: Clock is OFF 1: Clock is ON
30:18	/	/	/
17:16	R/W	0x0	CLK_SRC_SEL. 00: PLL_AUDIO (8X) 01: PLL_AUDIO(8X)/2 10: PLL_AUDIO(8X)/4 11: PLL_AUDIO(1X)
15:0	/	/	/.

DAUDIO 1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0xB4			Register Name: DAUDIO1_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>SCLK_GATING.</p> <p>Gating Special Clock(Max Clock = 200MHz)</p> <p>0: Clock is OFF</p> <p>1: Clock is ON</p>
30:18	/	/	/
17:16	R/W	0x0	<p>CLK_SRC_SEL.</p> <p>00: PLL_AUDIO (8X)</p> <p>01: PLL_AUDIO(8X)/2</p> <p>10: PLL_AUDIO(8X)/4</p> <p>11: PLL_AUDIO(1X)</p>
15:0	/	/	/.

USBPHY CONFIGURATION REGISTER(DEFAULT: 0X00000000)

Offset: 0xCC			Register Name: USBPHY_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31:17	/	/	/
16	R/W	0x0	<p>SCLK_GATING_OHCI.</p> <p>Gating Special Clock for OHCI</p> <p>0: Clock is OFF</p> <p>1: Clock is ON</p>
15:12	/	/	/
11	R/W	0	<p>SCLK_GATING_12M</p> <p>Gating Special 12M Clock for HSIC</p>

			0: Clock is OFF 1: Clock is ON The special 12M clock = OSC24M/2.
10	R/W	0	SCLK_GATING_HSIC Gating Special Clock for HSIC 0: Clock is OFF 1: Clock is ON The special clock is from PLL_HSIC
9	R/W	0x0	SCLK_GATING_USBPHY1. Gating Special Clock for USB PHY1(EHCI0,OHCI0) 0: Clock is OFF 1: Clock is ON
8	R/W	0x0	SCLK_GATING_USBPHY0. Gating Special Clock for USB PHY0(USB OTG) 0: Clock is OFF 1: Clock is ON
7:3	/	/	/
2	R/W	0	USBHSIC_RST USB HSIC Reset Control 0: Assert 1: De-assert
1	R/W	0x0	USBPHY1_RST. USB PHY1 Reset Control 0: Assert 1: De-assert
0	R/W	0x0	USBPHY0_RST. USB PHY0 Reset Control 0: Assert

			1: De-assert
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DRAM CFG REGISTER (DEFAULT: 0X00000000)

Offset: 0xF4			Register Name: DRAM_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SDRAM_CTR_RST. Sdram Controller Reset. 0: assert, 1: de-assert.
30:17	/	/	/
16	R/W	0x0	SDRCLK_UPD. SDRCLK Configuration 0 update. 0:Invalid 1:Valid. Note: Set this bit will validate Configuration 0. It will be auto cleared after the Configuration 0 is valid. The SDRCLK Source is from PLL_DDR.
15:0	/	/	/

DRAM CLK GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x100			Register Name: DRAM_GATING_REG
Bit	Read/ Write	Default /Hex	Description
31:29	/	/	/
28	R/W	0x0	DE_MP_DCLK_GATING. Gating DRAM Clock for DE_MP(0: mask, 1: pass).
27	/	/	/
26	R/W	0x0	BE_DCLK_GATING. Gating DRAM Clock for DE_BE(0: mask, 1: pass).

25	/	/	/
24	R/W	0x0	FE_DCLK_GATING. Gating DRAM Clock for DE_FE (0: mask, 1: pass).
23:17	/	/	/.
16	R/W	0x0	DRC_DCLK_GATING. Gating DRAM Clock for IEP DRC (0: mask, 1: pass).
15:2	/	/	/
1	R/W	0x0	CSI_DCLK_GATING. Gating DRAM Clock for CSI(0: mask, 1: pass).
0	R/W	0x0	VE_DCLK_GATING. Gating DRAM Clock for VE(0: mask, 1: pass).

DEBE CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x104			Register Name: BE_SCLK_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO 001: / 010: PLL_PERIPH(2X) 011: PLL_GPU 100: /

			101:PLL_DE 110/111:Reserved.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

DEFE CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x10C			Register Name: FE_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO 001: / 010: PLL_PERIPH(2X) 011: PLL_GPU 100: / 101: PLL_DE 110/111: Reserved.
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m)

			The pre-divided clock is divided by (m+1). The divider is from 1 to 16.
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LCD CH0 CLOCK (DEFAULT: 0X00000000)

Offset: 0x118			Register Name: LCD_CH0_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>SCLK_GATING. Gating Special Clock</p> <p>0: Clock is OFF 1: Clock is ON</p> <p>This special clock = Clock Source/ Divider M</p>
30:27	/	/	/
26:24	R/W	0x0	<p>CLK_SRC_SEL. Clock Source Select</p> <p>000: PLL_VIDEO(1X) 001: / 010: PLL_VIDEO(2X) 011: / 100: MIPI_PLL 101~111: /</p>
23:0	/	/	/

LCD CH1 CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x12C			Register Name: LCD_CH1_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>SCLK_GATING. Gating Special Clock</p> <p>0: Clock is OFF</p>

			1: Clock is ON This special clock = Clock Source/ Divider M.
30:26	/	/	/
25:24	R/W	0x0	SCLK_SEL. Special Clock Source Select 00: PLL_VIDEO(1X) 01: / 10: PLL_VIDEO(2X) 11: /
23:4	/	/	/
3:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

CSI CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x134			Register Name: CSI_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	CSI_SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Special Clock Source/CSI_SCLK_DIV_M.
30:27	/	/	/
26:24	R/W	0x0	SCLK_SRC_SEL. Special Clock Source Select 000: PLL_VIDEO(1X) 001: / 010: /

			011: PLL_DE 100: MIPI_PLL 101: PLL_VE 110~111: /
23:20	/	/	/
19:16	R/W	0x0	CSI_SCLK_DIV_M. CSI Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.
15	R/W	0x0	CSI_MCLK_GATING. Gating Master Clock 0: Clock is OFF 1: Clock is ON This clock =Master Clock Source/ CSI_MCLK_DIV_M.
14:11	/	/	/
10:8	R/W	0x0	MCLK_SRC_SEL. Master Clock Source Select 000: PLL_VIDEO(1X) 001: / 010: / 011: / 100: / 101: OSC24M 110~111: /
7:4	/	/	/
3:0	R/W	0x0	CSI_MCLK_DIV_M. CSI Master Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

VE CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x13C			Register Name: VE_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>SCLK_GATING.</p> <p>Gating the Special clock for VE(0: mask, 1: pass).</p> <p>Its clock source is the PLL_VE output.</p> <p>This special clock = Clock Source/Divider N.</p>
30:19	/	/	/.
18:16	R/W	0x0	<p>CLK_DIV_RATIO_N.</p> <p>Clock pre-divide ratio (N)</p> <p>The select clock source is pre-divided by n+1. The divider is from 1 to 8.</p>
15:0	/	/	/

ADDA_D CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x140			Register Name: ADDA_D_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>SCLK_GATING.</p> <p>Gating Special Clock</p> <p>0: Clock is OFF</p> <p>1: Clock is ON</p> <p>This special clock = PLL-Audio output.</p>
30:0	/	/	/

AVS CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x144			Register Name: AVS_CLK_REG
Bit	Read/ Write	Default /Hex	Description

31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = OSC24M.
30:0	/	/	/

MBUS CLOCK CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x15C			Register Name: MBUS_SCLK_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	MBUS_SCLK_GATING. Gating Clock for MBUS 0: Clock is OFF, 1: Clock is ON; MBUS_CLOCK = Clock Source/Divider N/Divider M
30:26	/	/	/
25:24	R/W	0x0	MBUS_SCLK_SRC Clock Source Select 00: OSC24M 01: PLL_PERIPH(2X) 10: PLL_DDR 11: Reserved
23:3	/	/	/
2:0	R/W	0x0	MBUS_SCLK_RATIO_M Clock Divide Ratio (M) The divided clock is divided by (M+1). The divider is from 1 to 8. The divide ratio must be changed smoothly. Note: If the clock has been changed ,it must wait for at least 16 cycles.

MIPI_DSI CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x168			Register Name: MIPI_DSI_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>DSI_SCLK_GATING.</p> <p>Gating DSI Special Clock</p> <p>0: Clock is OFF</p> <p>1: Clock is ON</p> <p>DSI Special clock(test clock) = Clock Source/DSI_SCLK_DIV_M.</p>
30:26	/	/	/
25:24	R/W	0x0	<p>DSI_SCLK_SRC_SEL.</p> <p>DSI Special Clock Source Select</p> <p>00: PLL_VIDEO(1X)</p> <p>01: /</p> <p>10: PLL_VIDEO(2X)</p> <p>11: /</p>
23:20	/	/	/
19:16	R/W	0x0	<p>DSI_SCLK_DIV_M.</p> <p>DSI Special Clock divide ratio (m)</p> <p>The pre-divided clock is divided by (m+1). The divider is from 1 to 16.</p>
15	R/W	0x0	<p>DSI_DPHY_GATING.</p> <p>Gating DSI DPHY Clock</p> <p>0: Clock is OFF</p> <p>1: Clock is ON</p> <p>This DSI DPHY clock =Clock Source/ DPHY_CLK_DIV_M.</p>
14:10	/	/	/
9:8	R/W	0x0	<p>DSI_DPHY_SRC_SEL.</p> <p>DSI DPHY Clock Source Select.</p>

			00: PLL_VIDEO(1X) 01: / 10: PLL_PERIPH 11: /
7:4	/	/	/.
3:0	R/W	0x0	DPHY_CLK_DIV_M. DSI DPHY Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 16.

IEP-DRC CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x180			Register Name: DRC_SCLK_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SCLK_GATING. Gating Special Clock 0: Clock is OFF 1: Clock is ON This special clock = Clock Source/Divider M.
30:27	/	/	/
26:24	R/W	0x0	CLK_SRC_SEL. Clock Source Select 000: PLL_VIDEO(1X) 001: / 010: PLL_PERIPH(2X) 011: PLL_GPU 100:/ 101:PLL_DE 110/111:Reserved.
23:4	/	/	/

3:0	R/W	0x0	<p>CLK_DIV_RATIO_M.</p> <p>Clock divide ratio (m)</p> <p>The pre-divided clock is divided by (m+1). The divider is from 1 to 16.</p>
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GPU CLOCK REGISTER (DEFAULT: 0X00000000)

Offset: 0x1A0			Register Name: GPU_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	<p>SCLK_GATING.</p> <p>Gating the Special clock for GPU(0: mask, 1: pass).</p> <p>This special clock = Clock Source(PLL-GPU)/Divider N.</p>
30:3	/	/	/.
2:0	R/W	0x0	<p>CLK_DIV_RATIO_N.</p> <p>Clock pre-divide ratio (N)</p> <p>The select clock source is pre-divided by n+1. The divider is from 1 to 8.</p>

ATS CLOCK REGISTER (DEFAULT: 0X80000000)

Offset: 0x1B0			Register Name: ATS_CLK_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x1	<p>SCLK_GATING.</p> <p>Gating Special Clock(Max Clock = 200MHz)</p> <p>0: Clock is OFF</p> <p>1: Clock is ON</p> <p>This special clock = Clock Source /Divider M.</p>
30:26	/	/	/
25:24	R/W	0x0	<p>CLK_SRC_SEL.</p> <p>Clock Source Select</p>

			00: OSC24M 01: PLL_PERIPH 10: / 11: /.
23:3	/	/	/
2:0	R/W	0x0	CLK_DIV_RATIO_M. Clock divide ratio (m) The pre-divided clock is divided by (m+1). The divider is from 1 to 8.

PLL LOCK TIME REGISTER (DEFAULT:0X000000FF)

Offset: 0x200			Register Name: PLL_LOCK_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31:16	/	/	/
15:0	R/W	0x00FF	PLL_LOCK_TIME PLL Lock Time (Unit: us). Note: When any PLL (except PLL-CPU) is enabled or changed, the corresponding PLL lock bit will be set after the PLL Lock Time.

PLL_CPU LOCK TIME REGISTER (DEFAULT:0X000000FF)

Offset: 0x204			Register Name: PLLCPU_LOCK_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31:16	/	/	/
15:0	R/W	0x00FF	PLLCPU_LOCK_TIME PLLCPU Lock Time (Unit: us). Note: When PLLCPU is enabled or changed, the PLLCPU lock bit will be set after the PLLCPU Lock Time.

PLL_CPU_BIAS REGISTER (DEFAULT:0X08100200)

Offset: 0x220			Register Name: PLLCPU_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	VCO_RST. VCO reset in.
30:29	/	/	/
28	R/W	0x0	EXG_MODE. Exchange mode. Note: CPU PLL source will select PLL_PERIPH instead of PLL_CPU
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL. PLL VCO bias control[3:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control[4:0].
15:11	/	/	/
10:8	R/W	0x2	PLL_LOCK_CTRL. PLL lock time control[2:0].
7:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACT_CTRL. PLL damping factor control[3:0].

PLL_AUDIO_BIAS REGISTER (DEFAULT:0X10100000)

Offset: 0x224			Register Name: PLLAUDIO_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS. PLL VCO Bias Current[4:0]

23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR. PLL Bias Current[4:0]
15:0	/	/	/

PLL_VIDEO_BIAS REGISTER (DEFAULT:0X10100000)

Offset: 0x228			Register Name: PLLVIDEO_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

PLL_VE BIAS REGISTER (DEFAULT:10100000)

Offset: 0x22C			Register Name: PLLVE_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].

15:3	/	/	/
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

PLL_DDR BIAS REGISTER (DEFAULT:0X81104000)

Offset: 0x230			Register Name: PLLDDR_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31:28	R/W	0x8	PLL_VCO_BIAS. PLL VCO bias[3:0]
27:26	/	/	/
25	R/W	0x0	PLL_VCO_GAIN_CTRL_EN. PLL VCO gain control enable. 0: disable, 1: enable.
24	R/W	0x1	PLL_BANDW_CTRL. PLL band width control. 0: narrow, 1: wide.
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control.
15	/	/	/
14:12	R/W	0x4	PLL_VCO_GAIN_CTRL. PLL VCO gain control bit[2:0].
11:4	/	/	/
3:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[3:0].

PLL_PERH BIAS REGISTER (DEFAULT:0X10100010)

Offset: 0x234			Register Name: PLLPERH_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31:29	/	/	/
28:24	R/W	0x10	PLL_VCO_BIAS. PLL VCO bias[4:0]
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control.
15:5	/	/	/
4	R/W	0x1	PLL_BANDW_CTRL. PLL band width control. 0: narrow, 1: wide.
3:2	/	/	/
1:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[1:0].

PLL_GPU BIAS REGISTER (DEFAULT:0X10100000)

Offset: 0x23C			Register Name: PLLGPU_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31:29	/	/	/.
28:24	R/W	0X10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/.
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/.

2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].
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MIPI_PLL_BIAS REGISTER (DEFAULT: 0XA8100400)

Offset: 0x240			Register Name: MIPI_PLL_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x1	VCO_RST. VCO reset in.
30:28	R/W	0x2	PLLVDD_LDO_OUT_CTRL. PLLVDD LDO output control. 000:1.10v 001:1.15v 010:1.20v 011:1.25v 100: 1.30v 101:1.35v 110:1.40v 111:1.45v
27:24	R/W	0x8	PLL_VCO_BIAS_CTRL. PLL VCO bias control [3:0].
23:21	/	/	/
20:16	R/W	0x10	PLL_BIAS_CUR_CTRL. PLL Bias Current Control[4:0].
15:11	/	/	/
10:8	R/W	0x4	PLL_LOCK_CTRL. PLL lock time control[2:0].
7:1	/	/	/
0	R/W	0x0	PLL_DAMP_FACT_CTRL.

			PLL damping factor control.
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PLL HSIC BIAS REGISTER (DEFAULT:10100000)

Offset: 0x244			Register Name: PLL_HSIC_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31:29	/	/	/.
28:24	R/W	0X10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/.
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/.
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

PLL_DE BIAS REGISTER (DEFAULT:10100000)

Offset: 0x248			Register Name: PLLDE_BIAS_REG
Bit	Read/ Write	Default /Hex	Description
31:29	/	/	/.
28:24	R/W	0X10	PLL_VCO_BIAS_CTRL. PLL VCO Bias Control[4:0].
23:21	/	/	/.
20:16	R/W	0x10	PLL_BIAS_CTRL. PLL Bias Control[4:0].
15:3	/	/	/.
2:0	R/W	0x0	PLL_DAMP_FACTOR_CTRL. PLL damping factor control[2:0].

PLL_CPU TUNING REGISTER (DEFAULT:0X0A101000)

Offset: 0x250			Register Name: PLL-CPU_TUN_REG
Bit	Read/ Write	Default /Hex	Description
31:28	/	/	/
27	R/W	0x1	PLL_BAND_WID_CTRL. PLL band width control. 0: narrow, 1: wide.
26	R/W	0x0	VCO_GAIN_CTRL_EN. VCO Gain Control Enable. 0: disable, 1: enable.
25:23	R/W	0x4	VCO_GAIN_CTRL. VCO gain control bits[2:0].
22:16	R/W	0x10	PLL_INIT_FREQ_CTRL. PLL initial frequency control[6:0].
15	R/W	0x0	C_OD. c-reg-od for verify
14:8	R/W	0x10	C_B_IN. c-b-in[6:0] for verify
7	R/W	0x0	C_OD1. c-reg-od1 for verify
6:0	R	0x0	C_B_OUT. c-b-out[6:0] for verify

PLL-DDR-TUNING REGISTER (DEFAULT: 0X14880000)

Offset: 0x260			Register Name: PLLDDR_TUN_REG
Bit	Read/ Write	Default /Hex	Description

31:29	/	/	/
28	R/W	0x1	VREG1_OUT_EN. vreg1 out enable. 0: disable, 1: enable.
27	/	/	/
26:24	R/W	0x4	PLL_LTME_CTRL. PLL lock time control[2:0].
23	R/W	0x1	VCO_RST. VCO reset in.
22:16	R/W	0x08	PLL_INIT_FREQ_CTRL. PLL initial frequency control[6:0].
15	R/W	0x0	OD1. Reg-od1 for verify.
14:8	R/W	0x0	B_IN. b-in[6:0] for verify
7	R/W	0x0	OD. reg-od for verify
6:0	R/W	0x0	B_OUT. b-out[6:0] for verify.

MIPI_PLL TUNING REGISTER (DEFAULT: 0X8A002000)

Offset: 0x270			Register Name: MIPI_PLL_TUN_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x1	PLL_INPUT_POWER_SEL. 0:2.5V 1:3.3V
30	/	/	/

29:28	R/W	0x0	VREG_OUT_EN. for verify
27	R/W	0x1	PLL_BAND_WID_CTRL. PLL band width control. 0: narrow, 1: wide.
26	R/W	0x0	VCO_GAIN_CTRL_EN. VCO Gain Control Enable. 0: disable, 1: enable.
25:23	R/W	0x4	VCO_GAIN_CTRL. VCO gain control bits[2:0].
22	/	/	/
21:16	R/W	0x0	CNT_INT. For Verify[5:0].
15	R/W	0x0	C_OD. c-reg-od for verify
14	/	/	/
13:8	R/W	0x20	C_B_IN. c-b-in[5:0] for verify
7	R/W	0x0	C_OD1. c-reg-od1 for verify
6	/	/	/
5:0	R		C_B_OUT. c-b-out[5:0] for verify

PLL-CPU-PATTERN CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x280			Register Name: PLLCPU_PAT_CFG_REG
Bit	Read/ Write	Default /Hex	Description

31	R/W	0x0	SIG_DELTA_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

PLL-AUDIO- PATTERN CONTROL REGISTER(DEFAULT:0X00000000)

Offset: 0x284			Register Name: PLLAUDIO_PAT_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SIG_DELTA_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0

			01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32Khz 10: 32.5KHz 11: 33Khz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

PLL-VIDEO- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x288			Register Name: PLLVIDEO_PAT_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.

19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

PLL-VE- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x28C			Register Name: PLLVE_PAT_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz

			10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

PLL-DDR- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x290			Register Name: PLLDDR_PAT_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SIG_DELTA_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

PLL-GPU- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x29C			Register Name: PLLGPU_PAT_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32Khz 10: 32.5KHz 11: 33Khz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

MIPI_PLL- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x2A0			Register Name: MIPI_PLL_PAT_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN.

			Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

PLL_HSIC- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x2A4			Register Name: PLL_HSIC_PAT_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1

			10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/
18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

PLL-DE- PATTERN CONTROL REGISTER (DEFAULT:0X00000000)

Offset: 0x2A8			Register Name: PLLDE_PAT_CFG_REG
Bit	Read/ Write	Default /Hex	Description
31	R/W	0x0	SIG_DELT_PAT_EN. Sigma-delta pattern enable.
30:29	R/W	0x0	SPR_FREQ_MODE. Spread Frequency Mode. 00: DC=0 01: DC=1 10: Triangular 11: awmode
28:20	R/W	0x0	WAVE_STEP. Wave step.
19	/	/	/

18:17	R/W	0x0	FREQ. Frequency. 00: 31.5KHz 01: 32KHz 10: 32.5KHz 11: 33KHz
16:0	R/W	0x0	WAVE_BOT. Wave Bottom.

AHB1 MODULE SOFTWARE RESET REGISTER 0(DEFAULT: 0X00000000)

Offset: 0x2C0			Register Name: AHB1_RST_REG0
Bit	Read/ Write	Default /Hex	Description
31:30	/	/	/
29	R/W	0x0	USBOHCI_RST. USB OHCI Reset Control 0: Assert 1: De-assert
27	/	/	/
26	R/W	0x0	USBEHCI_RST. USB EHCI Reset Control 0: Assert 1: De-assert
25	/	/	/
24	R/W	0x0	USBOTG_RST. USB OTG Reset Control 0: Assert 1: De-assert
23:22			

21	R/W	0x0	SPI1_RST. SPI1 reset. 0: assert, 1: de-assert.
20	R/W	0x0	SPI0_RST. SPI0 reset. 0: assert, 1: de-assert.
19	R/W	0x0	HSTMR_RST. HSTMR reset. 0: assert, 1: de-assert.
18:15	/	/	/
14	R/W	0x0	SDRAM_RST. SDRAM AHB reset. 0: assert, 1: de-assert.
13	R/W	0x0	NAND_RST. NAND reset. 0: assert, 1: de-assert.
12:11	/	/	/
10	R/W	0x0	SD2_RST. SD/MMC2 reset. 0: assert, 1: de-assert.
9	R/W	0x0	SD1_RST. SD/MMC1 reset. 0: assert, 1: de-assert.
8	R/W	0x0	SD0_RST. SD/MMC0 reset. 0: assert, 1: de-assert.
7	/	/	/
6	R/W	0x0	DMA_RST.

			DMA reset. 0: assert, 1: de-assert.
5:2	/	/	/
1	R/W	0x0	MIPIDSI_RST. MIPI DSI reset. 0: assert, 1: de-assert.
0	/	/	/

AHB1 MODULE SOFTWARE RESET REGISTER 1(DEFAULT: 0X00000000)

Offset: 0x2C4			Register Name: AHB1_RST_REG1
Bit	Read/ Write	Default /Hex	Description
31:26	/	/	/
25	R/W	0x0	DRC_RST. DRC reset. 0: assert, 1: de-assert.
24:23	/	/	/
22	R/W	0x0	SPINLOCK_RST. SPINLOCK reset. 0: assert, 1: de-assert.
21	R/W	0x0	/
20	R/W	0x0	GPU_RST. GPU reset. 0: assert, 1: de-assert.
19:15	/	/	/
14	R/W	0x0	FE_RST. DE-FE reset. 0: assert, 1: de-assert.

13	/	/	/
12	R/W	0x0	BE_RST. DE-BE reset. 0: assert, 1: de-assert.
11:9	/	/	/
8	R/W	0x0	CSI_RST. CSI reset. 0: assert, 1: de-assert.
7:5	/	/	
4	R/W	0x0	LCD_RST. LCD reset. 0: assert, 1: de-assert.
3:1	/	/	/
0	R/W	0x0	VE_RST. VE reset. 0: assert, 1: de-assert.

AHB1 MODULE SOFTWARE RESET REGISTER2(DEFAULT:0X00000000)

Offset: 0x2C8			Register Name: AHB1_RST_REG2
Bit	Read/ Write	Default /Hex	Description
31:1	/	/	/
0	R/W	0x0	LVDS_RST. LVDS reset. 0: assert, 1: de-assert.

APB1 MODULE SOFTWARE RESET REGISTER(DEFAULT: 0X00000000)

Offset: 0x2D0	Register Name: APB1_RST_REG
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Bit	Read/ Write	Default /Hex	Description
31:14	/	/	/.
13	R/W	0x0	DAUDIO1_RST. DAUDIO 1 reset. 0: assert, 1: de-assert.
12	R/W	0x0	DAUDIO0_RST. DAUDIO 0 reset. 0: assert, 1: de-assert.
11:1	/	/	/
0	R/W	0x0	ADDA_D_RST. ADDA_D reset. 0: assert, 1: de-assert.

APB2 MODULE SOFTWARE RESET REGISTER(DEFAULT: 0X00000000)

Offset: 0x2D8			Register Name: APB2_RST_REG
Bit	Read/ Write	Default /Hex	Description
31:21	/	/	/.
20	R/W	0x0	UART4_RST. UART4 reset. 0: assert, 1: de-assert.
19	R/W	0x0	UART3_RST. UART3 reset. 0: assert, 1: de-assert.
18	R/W	0x0	UART2_RST. UART2 reset. 0: assert, 1: de-assert.
17	R/W	0x0	UART1_RST.

			UART1 reset. 0: assert, 1: de-assert.
16	R/W	0x0	UART0_RST. UART0 reset. 0: assert, 1: de-assert.
15:3	/	/	/
2	R/W	0x0	TWI2_RST. TWI2 reset. 0: assert, 1: de-assert.
1	R/W	0x0	TWI1_RST. TWI1 reset. 0: assert, 1: de-assert.
0	R/W	0x0	TWI0_RST. TWI0 reset. 0: assert, 1: de-assert.

3.4 CPU

3.4.1 Overview

The CPU configuration module features:

- Support software reset control for each CPU core
- Support CPU configuration for each CPU core
- Support a 64-bit common counter

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3.4.2 CPUCFG Register List

Module Name	Base Address
CPUCFG	0x01F01C00

Register Name	Offset	Description
/	0x0000	/
/	0x000C	/
/	0x0010	/
/	0x0014	/
/	0x0018	/
/	0x001C	/
/	0x0020	/
/	0x0024	/
/	0x0028	/
/	0x002C	/
CPU0_RST_CTRL	0x0040	CPU0 Reset Control
CPU0_CTRL_REG	0x0044	CPU0 Control Register
CPU0_STATUS_REG	0x0048	CPU0 Status Register
CPU1_RST_CTRL	0x0080	CPU1 Reset Control
CPU1_CTRL_REG	0x0084	CPU1 Control Register
CPU1_STATUS_REG	0x0088	CPU1 Status Register
CPU_SYS_RST_REG	0x0140	CPU System Reset Register
GENER_CTRL_REG	0x0184	General Control Register
EVENT_IN	0x0190	Event Input Register
SUP_STAN_FLAG_REG	0x01A0	Super Standby Flag Register
PRIVATE_REG0	0x01A4	Private Register0

PRIVATE_REG1	0x01A8	Private Register1
CNT64_CTRL_REG	0x0280	64-Bit Counter Control Register
CNT64_LOW_REG	0x0284	64-Bit Counter Low Register
CNT64_HIGH_REG	0x0288	64-Bit Counter High Register

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3.4.3 CPUCFG Register Description

CPU0 RESET CONTROL(DEFAULT: 0X00000003)

Offset: 0x40			Register Name: CPU0_RST_CTRL
Bit	Read/Writ e	Default/H ex	Description
31: 2	/	/	/.
1	R/W	0x1	<p>CPU0_CORE_RST.</p> <p>These are the primary reset signals which initialize the processor logic in the processor power domains, not including the debug, breakpoint and watchpoint logic.</p> <p>0: assert 1: de-assert.</p>
0	R/W	0x1	<p>CPU0_RESET.</p> <p>CPU0 Reset Assert.</p> <p>These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain.</p> <p>0: assert 1: de-assert.</p>

CPU0 CONTROL REGISTER(DEFAULT :0X00000000)

Offset: 0x44			Register Name: CPU0_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	<p>CPU0_CP15_WRITE_DISABLE.</p> <p>Disable write access to certain CP15 registers.</p>

			0: enable 1: disable
--	--	--	-------------------------

CPU0 STATUS REGISTER(DEFAULT : 0X00000000)

Offset: 0x48			Register Name: CPU0_STATUS
Bit	Read/Writ e	Default/H ex	Description
31: 3	/	/	/.
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode: 0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

CPU1 RESET CONTROL(DEFAULT: 0X00000001)

Offset: 0x80			Register Name: CPU1_RST_CTRL
Bit	Read/Writ e	Default/H ex	Description
31: 2	/	/	/.
1	R/W	0x0	CPU1_CORE_RST. These are the primary reset signals which initialize the processor logic in the processor power domains, not including

			the debug, breakpoint and watchpoint logic. 0: assert 1: de-assert.
0	R/W	0x1	CPU1_RESET. CPU1 Reset Assert. These power-on reset signals initialize all the processor logic, including CPU Debug, and breakpoint and watch point logic in the processor power domains. They do not reset debug logic in the debug power domain. 0: assert 1: de-assert.

CPU1 CONTROL REGISTER(DEFAULT :0X00000000)

Offset: 0x84			Register Name: CPU1_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	CPU1_CP15_WRITE_DISABLE. Disable write access to certain CP15 registers. 0: enable 1: disable

CPU1 STATUS REGISTER(DEFAULT : 0X00000000)

Offset: 0x88			Register Name: CPU1_STATUS
Bit	Read/Writ e	Default/H ex	Description
31: 3	/	/	/.
2	R	0x0	STANDBYWFI. Indicates if the processor is in WFI standby mode:

			0: Processor not in WFI standby mode. 1: Processor in WFI standby mode
1	R	0x0	STANDBYWFE. Indicates if the processor is in the WFE standby mode: 0: Processor not in WFE standby mode 1: Processor in WFE standby mode
0	R	0x0	SMP_AMP 0: AMP mode 1: SMP mode

CPU SYSTEM RESET CONTROL REGISTER(DEFAULT :0X00000001)

Offset: 0x140			Register Name: CPU_SYS_RST_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x1	CPU System Reset Control. 0: assert 1: de-assert.

GENERAL CONTROL REGISTER(DEFAULT :0X00000020)

Offset: 0x184			Register Name: GENER_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31: 9	/	/	/.
8	R/W	0x0	CFGSDISABLE. Disables write access to some secure GIC registers.
7	/	/	/

6	R/W	0x0	ACINACTM. Snoop interface is inactive and no longer accepting requests.
5	R/W	0x1	L2_RST. L2 Reset.(SCU global reset) 0: Apply reset to shared L2 memory system controller. 1: Do not apply reset to shared L2 memory system controller.
4	R/W	0x0	L2_RST_DISABLE. Disable automatic L2 cache invalidate at reset: 0: L2 cache is reset by hardware. 1: L2 cache is not reset by hardware.
3:2	/	/	/
1:0	R/W	0x0	L1_RST_DISABLE. L1 Reset Disable[1:0]. 0: L1 cache is reset by hardware. 1: L1 cache is not reset by hardware.

EVENT INPUT REGISTER(DEFAULT : 0X00000000)

Offset: 0x190			Register Name: EVENT_IN
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/.
0	R/W	0x0	EVENT_IN. Event input that can wake-up CPU0/1/2/3 from WFE standby mode.

SUPER STANDBY FLAG REGISTER (DEFAULT: 0X00000000)

Offset: 0x1A0			Register Name: SUP_STAN_FLAG_REG
Bit	Read/Writ e	Default/H ex	Description

31:1 6	R/W	0x0	SUP_STANBY_FLAG. Key Field. Any value can be written and read back in the key field, but if the values are not appropriate, the lower 16 bits will not change in this register. Only follow the appropriate process, the super standby flag can be written in the lower 16 bits. Refer to Description and Diagram.
15:0	R/W	0x0	SUP_STANBY_FLAG_DATA. Refer to Description and Diagram

Note: When system is turned on, the value in the Super Standby Flag Register low 16 bits should be 0x0. If software programmer wants to write correct super standby flag ID in low 16 bits, the high 16 bits should be written 0x16AA at first. Then, software programmer must write 0xAA16XXXX in the Super Standby Flag Register, the 'XXXX' means the correct super standby flag ID. Referring to the Diagram section (Diagram 1.1) in detail.

PRIVATE REGISTERO (DEFAULT: 0X00000000)

Offset: 0x1A4			Register Name: PRIVATE_REG0
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	

PRIVATE REGISTER1 (DEFAULT: 0X00000000)

Offset: 0x1A8			Register Name: PRIVATE_REG1
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	

64-BIT COUNTER CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x280			Register Name: CNT64_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description

31: 3	/	/	/.
2	R/W	0x0	CNT64_CLK_SRC_SEL. 64-bit Counter Clock Source Select. 0: OSC24M 1: /
1	R/W	0x0	CNT64_RL_EN. 64-bit Counter Read Latch Enable. 0: no effect, 1: to latch the 64-bit Counter to the Low/Hi registers and it will change to zero after the registers are latched.
0	R/W	0x0	CNT64_CLR_EN. 64-bit Counter Clear Enable. 0: no effect, 1: to clear the 64-bit Counter Low/Hi registers and it will change to zero after the registers are cleared. Note: It is not recommended to clear this counter arbitrarily.

Note: This 64-bit counter will start to count as soon as the System Power On finished.

64-BIT COUNTER LOW REGISTER (DEFAULT: 0X00000000)

Offset: 0x284			Register Name: CNT64_LOW_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	CNT64_LO. 64-bit Counter [31:0].

64-BIT COUNTER HIGH REGISTER (DEFAULT: 0X00000000)

Offset: 0x288			Register Name: CNT64_HIGH_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	CNT64_HI.

			64-bit Counter [63:32].
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3.5 Power, Reset & Clock Management

3.5.1 Overview

The PRCM module features:

- Support clock configuration
- Support module reset
- Support GPU power clamp control
- Support system core power clamp control
- Support one clock output channel

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3.5.2 PRCM Register List

Module Name	Base Address
PRCM	0x01F01400

Register Name	Offset	Description
/	0x0000	/
APB0_CLK_DIV_REG	0x000C	Apb0 Clock Divide Ratio
APB0_GATING_REG	0x0028	Apb0 Clock Gating Register
PLL_CTRL_REG0	0x0040	PLL Control Register0
PLL_CTRL_REG1	0x0044	PLL Control Register1
APB0_MODULE_RST_REG	0x00B0	Apb0 Module Software Reset Register
CPU_PWROFF_GATING	0x0100	CPU Power Off Gating Register
VDD_SYS_PWROFF_GATING	0x0110	VDD_SYS Power Off Gating Register
GPU_PWROFF_GATING	0x0118	GPU Power Off Gating Register
VDD_SYS_PWR_RST	0x0120	VDD_SYS Power Domain Reset Register.
AUDIO_CFG	0x01C0	Audio Codec Configuration
HMIC_EN	0x01C4	Headphone Mic Detect Digital Part Enable
HMIC_CTL	0x01C8	HMIC Detect Control
HMIC_DATA	0x01CC	HMIC Pending&Data

3.5.3 PRCM Register Description

APB0 CLOCK DIVIDE RATIO (DEFAULT: 0X00000000)

Offset: 0x0C			Register Name: APB0_CLK_DIV_REG
Bit	Read/ Write	Default/H ex	Description
31:2	/	/	/
1:0	R/W	0x0	<p>APB0_CLK_RATIO.</p> <p>APB0 Clock divide ratio. APB0 clock source is AHBO clock.</p> <p>00: /1</p> <p>01: /2</p> <p>10: /3</p> <p>11: /4</p> <p>Note: This clock is used for some special module apbclk (R_UART/R_TWI/R_RSB)</p>

APB0 MODULE CLK GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x28			Register Name: APB0_GATING_REG
Bit	Read/ Write	Default/H ex	Description
31:7	/	/	/
6	R/W	0x0	<p>R_TWI_GATING</p> <p>Gating APB Clock for R_TWI.</p>
5	/	/	/
4	R/W	0x0	<p>R_UART_GATING.</p> <p>Gating APB Clock for R_UART(0: mask, 1: pass).</p>
3	R/W	0x0	<p>R_RSB_GATING.</p> <p>Gating APB Clock for R_RSB(0: mask, 1: pass).</p>
2	R/W	0x0	R_TIMERO_1_GATING.

			Gating APB Clock for R_TIMER0_1 (0: mask, 1: pass).
1	/	/	/
0	R/W	0x0	R_PIO_GATING Gating APB Clock for R_PIO(0: mask, 1: pass)

PLL CONTROL REGISTER (DEFAULT: 0X00101013)

Offset: 0x40			Register Name: PLL_CTRL_REG0
Bit	Read/W rite	Default/H ex	Description
31:25	/	/	/
24	R/W	0	TEST_CLK_SEL. Test clock select. 0: 24MHz. 1: external clock.
23:22	/	/	/
21:20	R/W	0x1	OSC24M_CLK_SEL. 24MHz clock source select.
19:14	/	/	/
13:12	R/W	0x1	INTERNALPLL_INPUT_SEL. Internal PLL input select.
11:6	/	/	/
5:4	R/W	1	USB_24M_CLK_SEL. USB 24MHz clock source select.
3:2	/	/	/
1	R/W	0x1	OSC24M_GAIN_ENHANCE.
0	R/W	0x1	PLL_BIAS_EN. PLL Bias Enable. 0: disable,

			1: enable.
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PLL CONTROL REGISTER1 (DEFAULT: 00070007)

Offset: 0x44			Register Name: PLL_CTRL_REG1																		
Bit	Read/Writ e	Default/H ex	Description																		
31:2 4	R/W	0x0	<p>KEY_FIELD. Key Field for LDO Enable bit. If the key field value is 0xA7, the bit[23:0] can be modified.</p>																		
23:1 9	/	/	/																		
18:1 6	R/W	0x7	<p>PLLVDD_LDO_OUT_CTRL. PLLVDD LDO (both LDO and LDO1) output control.</p> <table> <tr> <td>PLL_IN_PWR_SEL= 0</td> <td>PLL_IN_PWR_SEL= 1</td> </tr> <tr> <td>000: 1.16v</td> <td>000: 1.00v</td> </tr> <tr> <td>001: 1.19v</td> <td>001: 1.02v</td> </tr> <tr> <td>010: 1.22v</td> <td>010: 1.04v</td> </tr> <tr> <td>011: 1.25v</td> <td>011: 1.06v</td> </tr> <tr> <td>100: 1.28v</td> <td>100: 1.08v</td> </tr> <tr> <td>101: 1.31v</td> <td>101: 1.10v</td> </tr> <tr> <td>110: 1.34v</td> <td>110: 1.12v</td> </tr> <tr> <td>111: 1.37v</td> <td>111: 1.14v</td> </tr> </table> <p>Note: Before enable PLL, PLVVDD LDO should be set to 1.37v</p>	PLL_IN_PWR_SEL= 0	PLL_IN_PWR_SEL= 1	000: 1.16v	000: 1.00v	001: 1.19v	001: 1.02v	010: 1.22v	010: 1.04v	011: 1.25v	011: 1.06v	100: 1.28v	100: 1.08v	101: 1.31v	101: 1.10v	110: 1.34v	110: 1.12v	111: 1.37v	111: 1.14v
PLL_IN_PWR_SEL= 0	PLL_IN_PWR_SEL= 1																				
000: 1.16v	000: 1.00v																				
001: 1.19v	001: 1.02v																				
010: 1.22v	010: 1.04v																				
011: 1.25v	011: 1.06v																				
100: 1.28v	100: 1.08v																				
101: 1.31v	101: 1.10v																				
110: 1.34v	110: 1.12v																				
111: 1.37v	111: 1.14v																				
15	R/W	0x0	<p>PLL_IN_PWR_SEL. PLL Input Power Select. 0: 2.5v, 1: 3.0v</p>																		
14:4	/	/	/																		
3	R/W	0	CLKTEST_EN. For verify (Back door clock PLLTEST enable).																		

2	R/W	1	CRYSTAL_EN. External crystal enable.
1	R/W	1	LDO1_EN. 0: disable; 1: enable. Note: All PLL Analog Power enable (power source from VCC-PLL).
0	R/W	1	LDO_EN. 0: disable; 1: enable. Note: All PLL Digital Power enable (power source from VCC-PLL).

APB0 MODULE SOFTWARE RESET (DEFAULT: 0X00000000)

Offset: 0xB0			Register Name: APB0_MODULE_RST_REG
Bit	Read/Writ e	Default/H ex	Description
31: 7	/	/	/
6	R/W	0x0	R_TWI_RST. R_TWI Reset Control 0: Assert 1: De-assert
5	/	/	/
4	R/W	0x0	R_UART_RST. R_UART Reset Control 0: Assert 1: De-assert
3	R/W	0x0	R_RSB_RST. R_P2WI Reset Control

			0: Assert 1: De-assert
2	R/W	0x0	R_TIMERO_1_RST. R_TIMERO_1 Reset Control 0: Assert 1: De-assert
1:0	/	/	/

CPU POWER OFF GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x100			Register Name:CPU_PWROFF_GATING
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	PWROFF_GATING Gating the corresponding modules when CPU0 power off. 0: Invalid 1: Valid Note: This bit should be set to 1 before CPU0 power off while it should be set to 0 after the CPU0 power on.

VDD_SYS POWER OFF GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x110			Register Name: VDD_SYS_PWROFF_GATING
Bit	Read/Writ e	Default/H ex	Description
31: 4	/	/	/
3	R/W	0x0	VDD_CPLUS_GATING
2	R/W	0x0	AVCC_A_GATING Gating the corresponding modules to the AVCC_A Power

			<p>Domain when VDD_SYS power off.</p> <p>0: Invalid</p> <p>1: Valid</p> <p>Note: This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.</p>
1	R/W	0x0	<p>DRAM_CH1_PAD_HOLD.</p> <p>Hold the pad of DRAM channel 1</p> <p>0:Not hold</p> <p>1:Hold DRAM Pad.</p> <p>Note: This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.</p>
0	R/W	0x0	<p>DRAM_CH0_PAD_HOLD.</p> <p>Hold the pad of DRAM channel 0</p> <p>0:Not hold</p> <p>1:Hold DRAM Pad.</p> <p>Note: This bit should be set to 1 before VDD_SYS power off while it should be set to 0 after the VDD_SYS power on.</p>

GPU POWER OFF GATING REGISTER (DEFAULT: 0X00000000)

Offset: 0x118			Register Name: GPU_PWROFF_GATING
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	<p>PWROFF_GATING</p> <p>Gating the corresponding modules when GPU power off.</p> <p>0: Invalid</p> <p>1: Valid</p> <p>Note: This bit should be set to 1 before GPU power off while it should be set to 0 after the GPU power on.</p>

VDD_SYS POWER DOMAIN RESET REGISTER (DEFAULT: 0X00000001)

Offset: 0x120			Register Name: VDD_SYS_PWR_RST
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x1	<p>MODULE_RST</p> <p>VDD_SYS Power Domain Modules should be reset before VDD_SYS power on.</p> <p>0: Assert</p> <p>1: De-assert</p>

ADDA_PR CONFIGURATION REGISTER (DEFAULT: 0X10000000)

Offset: 0x1C0			Register Name: ADDA_PR_CFG_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28	R/W	0x1	<p>ADDA_PR_RST.</p> <p>ADDA_PR Reset.</p> <p>0: Assert</p> <p>1: De-assert</p>
27:2 5	/	/	/
24	R/W	0x0	<p>ADDA_PR_RW.</p> <p>ADDA_PR Read or Write.</p> <p>0: read</p> <p>1: write</p>
23:2 1	/	/	/

20:1 6	R/W	0x0	ADDA_PR _ADDR. ADDA_PR Address[4:0].
15:8	R/W	0x0	ADDA_PR _WDAT. ADDA_PR Write Data [7:0].
7:0	R/W	0x0	ADDA_PR _RDAT. ADDA_PR Read Data[7:0].

HMIC DIGITAL ENABLE REGISTER (DEFAULT: 0X00000001)

Offset: 0x1C4			Register Name: HMIC_EN
Bit	Read/Write	Default	Description
31:1	R/W	0x0	/
0	R/W	0x1	HMIC_DIG_EN Headphone mic detect digital part enable 0: disable 1:enable

HMIC CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x1C8			Register Name: HMIC_CTL
Bit	Read/Write	Default	Description
31:28	R/W	0x0	HMIC_M debounce when Key down or key up
27:24	R/W	0x0	HMIC_N debounce when earphone plug in or pull out
23	R/W	0x0	HMIC_DATA_IRQ_MODE Hmic Data Irq Mode Select 0: Hmic data irq once after key down 1: Hmic data irq from key down, util key up
22:21	R/W	0x0	HMIC_TH1_HYSTESIS Hmic Hysteresis Threshold1

			00: no Hysteresis 01: Pull Out when Data <= (Hmic_th2-1) 10: Pull Out when Data <= (Hmic_th2-2) 11: Pull Out when Data <= (Hmic_th2-3)
20	R/W	0x0	HMIC_PULLOUT_IRQ Hmic Earphone Pull out Irq Enable 00: disable 11: enable
19	R/W	0x0	HMIC_PLUGIN_IRQ Hmic Earphone Plug in Irq Enable 00: disable 11: enable
18	R/W	0x0	HMIC_KEYUP_IRQ Hmic Key Up Irq Enable 00: disable 11: enable
17	R/W	0x0	HMIC_KEYDOWN_IRQ Hmic Key Down Irq Enable 00: disable 11: enable
16	R/W	0x0	HMIC_DATA_IRQ_EN Hmic Data Irq Enable 00: disable 11: enable
15:14	R/W	0x0	HMIC_SAMPLE_SELECT Down Sample Setting Select 00: Down by 1, 128Hz 01: Down by 2, 64Hz 10: Down by 4, 32Hz 11: Down by 8, 16Hz
13	R/W	0x0	HMIC_TH2_HYSTERESIS Hmic Hysteresis Threshold2 0: no Hysteresis

			1: Key Up when Data <= (Hmic_th2-1)
12:8	R/W	0x0	HMIC_TH2 Hmic_th2 for detecting Key down or Key up.
7:6	R/W	0x0	HMIC_SF Hmic Smooth Filter setting 00: by pass 01: $(x_1+x_2)/2$ 10: $(x_1+x_2+x_3+x_4)/4$ 11: $(x_1+x_2+x_3+x_4+x_5+x_6+x_7+x_8)/8$
5	R/W	0x0	KEYUP_CLEAR Key Up Irq Pending bit auto clear when Key Down Irq 0: don't clear 1: auto clear
4:0	R/W	0x0	HMIC_TH1 Hmic_th1[4:0], detecting eraphone plug in or pull out.

HMIC DATA REGISTER (DEFAULT: 0X00000000)

Offset: 0x1CC			Register Name: HMIC_DATA
Bit	Read/Write	Default	Description
31:21	/	/	/
20	R/W	0x0	HMIC_PULLOUT_PENDING Hmic Earphone Pull out Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Pull out Irq Pending Interrupt
19	R/W	0x0	HMIC_PLUGIN_PENDING Hmic Earphone Plug in Irq pending bit, write 1 to clear 0: No Pending Interrupt 1: Plug in Irq Pending Interrupt
18	R/W	0x0	HMIC_KEYUP_PENDING

			Hmic Key Up IRQ pending bit, write 1 to clear 0: No Pending Interrupt 1: Key up IRQ Pending Interrupt
17	R/W	0x0	HMIC_KEYDOWN_PENDING Hmic Key Down IRQ pending bit, write 1 to clear 0: No Pending Interrupt 1: Key down IRQ Pending Interrupt
16	R/W	0x0	HMIC_DATA_PENDING Hmic Data IRQ pending bit, write 1 to clear 0: No Pending Interrupt 1: Data IRQ Pending Interrupt
15:5	/	/	/
4:0	R	0x0	HMIC_DATA HMIC ADC Data

3.6 Timer

3.6.1 Overview

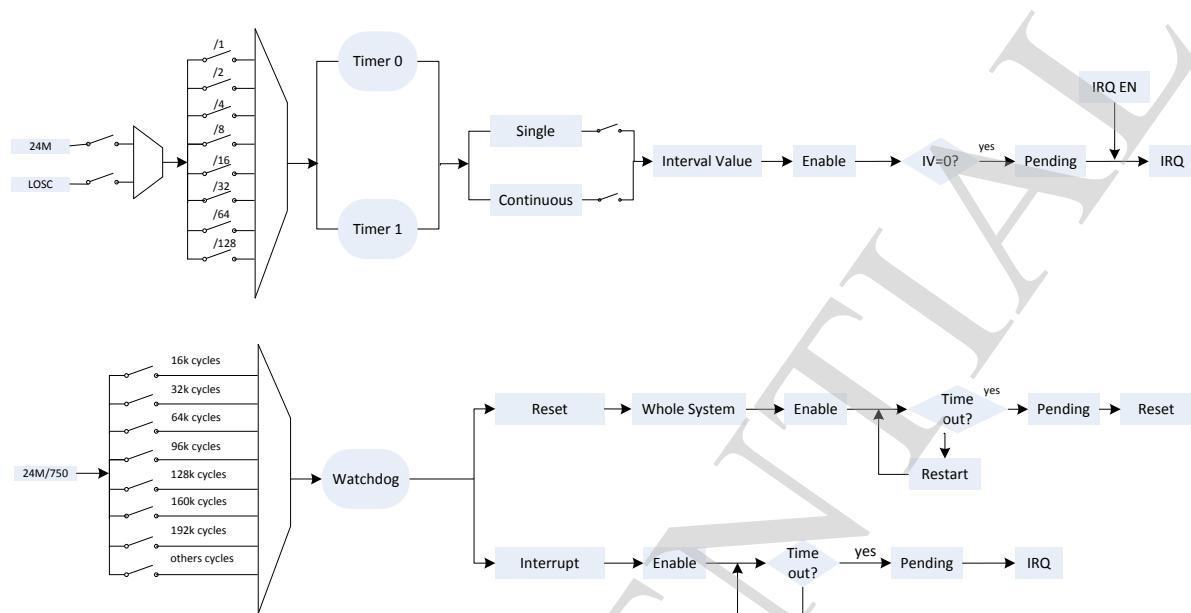
The A23 provides two timers, a watch dog and two AVS counters.

Timer 0/1 can take their inputs from internal RC oscillator, external 32768Hz crystal or OSC24M. They provide the operating system's scheduler interrupt. It is designed to offer maximum accuracy and efficient management, even for systems with long or short response time. They provide 24-bit programmable overflow counter and work in auto-reload mode or no-reload mode. When the current value in *Current Value Register* is counting down to zero, the timer will generate interrupt if set interrupt enable bit.

The watchdog is used to resume the controller operation when it had been disturbed by malfunctions such as noise and system errors. It features a down counter that allows a watch dog period of up to 16 seconds (512000 cycles). It can generate a general reset or interrupt request.

AVS counter is used to synchronize video and audio in the player.

3.6.2 Block Diagram



3.6.3 Timer Register List

Module Name	Base Address
Timer	0x01C20C00

Register Name	Offset	Description
TMR_IRQ_EN_REG	0x0	Timer IRQ Enable Register
TMR_IRQ_STA_REG	0x4	Timer Status Register
TMRO_CTRL_REG	0x10	Timer 0 Control
TMRO_INTV_VALUE_REG	0x14	Timer 0 Interval Value Register
TMRO_CUR_VALUE_REG	0x18	Timer 0 Current Value Register
TMR1_CTRL_REG	0x20	Timer 1 Control Register
TMR1_INTV_VALUE_REG	0x24	Timer 1 Interval Value Register
TMR1_CUR_VALUE_REG	0x28	Timer 1 Current Value Register
AVS_CNT_CTL_REG	0x80	AVS Control Register
AVS_CNT0_REG	0x84	AVS Counter 0 Register
AVS_CNT1_REG	0x88	AVS Counter 1 Register
AVS_CNT_DIV_REG	0x8C	AVS Divisor
WDOG0_IRQ_EN_REG	0xA0	Watchdog 0 IRQ Enable Register
WDOG0_IRQ_STA_REG	0xA4	Watchdog 0 Status Register
WDOG0_CTRL_REG	0xB0	Watchdog 0 Control Register
WDOG0_CFG_REG	0xB4	Watchdog 0 Configuration Register
WDOG0_MODE_REG	0xB8	Watchdog 0 Mode Register

3.6.4 Timer Programmable Register

TIMER IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x0			Register Name: TMR_IRQ_EN_REG
Bit	Read/Writ e	Default/H ex	Description
31:2	/	/	/
1	R/W	0x0	<p>TMR1_IRQ_EN.</p> <p>Timer 1 Interrupt Enable.</p> <p>0: No effect;</p> <p>1: Timer 1 Interval Value reached interrupt enable.</p>
0	R/W	0x0	<p>TMR0_IRQ_EN.</p> <p>Timer 0 Interrupt Enable.</p> <p>0: No effect;</p> <p>1: Timer 0 Interval Value reached interrupt enable.</p>

TIMER IRQ STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x4			Register Name: TMR_IRQ_STA_REG
Bit	Read/Writ e	Default/H ex	Description
31:2	/	/	/
1	R/W	0x0	<p>TMR1_IRQ_PEND.</p> <p>Timer 1 IRQ Pending. Set 1 to the bit will clear it.</p> <p>0: No effect;</p> <p>1: Pending, timer 1 interval value is reached.</p>
0	R/W	0x0	<p>TMR0_IRQ_PEND.</p> <p>Timer 0 IRQ Pending. Set 1 to the bit will clear it.</p> <p>0: No effect;</p>

			1: Pending, timer 0 interval value is reached.
--	--	--	--

TIMER 0 CONTROL REGISTER (DEFAULT: 0X00000004)

Offset:0x10			Register Name: TMRO_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31:8	/	/	/
7	R/W	0x0	<p>TMRO_MODE.</p> <p>Timer 0 mode.</p> <p>0: Continuous mode. When interval value reached, the timer will not disable automatically.</p> <p>1: Single mode. When interval value reached, the timer will disable automatically.</p>
6:4	R/W	0x0	<p>TMRO_CLK_PRES.</p> <p>Select the pre-scale of timer 0 clock source.</p> <p>000: /1</p> <p>001: /2</p> <p>010: /4</p> <p>011: /8</p> <p>100: /16</p> <p>101: /32</p> <p>110: /64</p> <p>111: /128</p>
3:2	R/W	0x1	<p>TMRO_CLK_SRC.</p> <p>Timer 0 Clock Source. 'N' is the value of Internal OSC Clock Prescalar register.</p> <p>00: InternalOSC / N</p> <p>01: OSC24M.</p> <p>10: /</p> <p>11: /</p>

1	R/W	0x0	<p>TMRO_RELOAD.</p> <p>Timer 0 Reload.</p> <p>0: No effect, 1: Reload timer 0 Interval value.</p> <p>After the bit is set, it can not be written again before it's cleared automatically.</p>
0	R/W	0x0	<p>TMRO_EN.</p> <p>Timer 0 Enable.</p> <p>0: Stop/Pause, 1: Start.</p> <p>If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0.</p> <p>If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1.</p> <p>In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.</p>

TIMER 0 INTERVAL VALUE REGISTER

Offset:0x14			Register Name: TMRO_INTV_VALUE_REG
Bit	Read/Writ e	Default/H ex	Description
31:0	R/W	0x0	<p>TMRO_INTV_VALUE.</p> <p>Timer 0 Interval Value.</p>

Note: the value setting should consider the system clock and the timer clock source.

TIMER 0 CURRENT VALUE REGISTER

Offset:0x18			Register Name: TMRO_CUR_VALUE_REG
Bit	Read/Writ e	Default/H ex	Description

31:0	R/W	0x0	TMRO_CUR_VALUE. Timer 0 Current Value.
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Note: Timer 0 current value is a 32-bit down-counter (from interval value to 0).

TIMER 1 CONTROL REGISTER (DEFAULT: 0X00000004)

Offset:0x20			Register Name: TMR1_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31:8	/	/	/
7	R/W	0x0	<p>TMR1_MODE. Timer 1 mode.</p> <p>0: Continuous mode. When interval value reached, the timer will not disable automatically.</p> <p>1: Single mode. When interval value reached, the timer will disable automatically.</p>
6:4	R/W	0x0	<p>TMR1_CLK_PRES. Select the pre-scale of timer 1 clock source.</p> <p>000: /1 001: /2 010: /4 011: /8 100: /16 101: /32 110: /64 111: /128</p>
3:2	R/W	0x1	<p>TMR1_CLK_SRC. Timer 1 Clock Source. 'N' is the value of Internal OSC Clock Prescalar register.</p> <p>00: InternalOSC / N 01: OSC24M.</p>

			10: / 11: /.
1	R/W	0x0	<p>TMR1_RELOAD.</p> <p>Timer 1 Reload.</p> <p>0: No effect, 1: Reload timer 1 Interval value.</p> <p>After the bit is set, it can not be written again before it's cleared automatically.</p>
0	R/W	0x0	<p>TMR1_EN.</p> <p>Timer 1 Enable.</p> <p>0: Stop/Pause, 1: Start.</p> <p>If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0.</p> <p>If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1.</p> <p>In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.</p>

TIMER 1 INTERVAL VALUE REGISTER

Offset:0x24			Register Name: TMR1_INTV_VALUE_REG
Bit	Read/Writ e	Default/H ex	Description
31:0	R/W	0x0	<p>TMR1_INTV_VALUE.</p> <p>Timer 1 Interval Value.</p>

Note: the value setting should consider the system clock and the timer clock source.

TIMER 1 CURRENT VALUE REGISTER

Offset:0x28	Register Name: TMR1_CUR_VALUE_REG
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Bit	Read/Writ e	Default/H ex	Description
31:0	R/W	0x0	TMR1_CUR_VALUE. Timer 1 Current Value.

Note: Timer 1 current value is a 32-bit down-counter (from interval value to 0).

AVS COUNTER CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x80			Register Name: AVS_CNT_CTL_REG
Bit	Read /Write	Default	Description
31:10	/	/	/
9	R/W	0x0	AVS_CNT1_PS. Audio/Video Sync Counter 1 Pause Control 0: Not pause 1: Pause Counter 1
8	R/W	0x0	AVS_CNT0_PS. Audio/Video Sync Counter 0 Pause Control 0: Not pause 1: Pause Counter 0
7:2	/	/	/
1	R/W	0x0	AVS_CNT1_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable 1: Enable
0	R/W	0x0	AVS_CNT0_EN. Audio/Video Sync Counter 1 Enable/ Disable. The counter source is OSC24M. 0: Disable

			1: Enable
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AVS COUNTER 0 REGISTER (DEFAULT: 0X00000000)

Offset:0x84			Register Name: AVS_CNT0_REG
Bit	Read /Write	Default	Description
31:0	R/W	0x0	<p>AVS_CNT0.</p> <p>Counter 0 for Audio/ Video Sync Application</p> <p>The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT0_PS to '1'. When it is paused, the counter won't increase.</p>

AVS COUNTER 1 REGISTER (DEFAULT: 0X00000000)

Offset:0x88			Register Name: AVS_CNT1_REG
Bit	Read /Write	Default	Description
31:0	R/W	0x0	<p>AVS_CNT1.</p> <p>Counter 1 for Audio/ Video Sync Application</p> <p>The high 32 bits of the internal 33-bits counter register. The initial value of the internal 33-bits counter register can be set by software. The LSB bit of the 33-bits counter register should be zero when the initial value is updated. It will count from the initial value. The initial value can be updated at any time. It can also be paused by setting AVS_CNT1_PS to '1'. When it is paused, the counter won't increase.</p>

AVS COUNTER DIVISOR REGISTER (DEFAULT: 0X05DB05DB)

Offset:0x8C	Register Name: AVS_CNT_DIV_REG
-------------	--------------------------------

Bit	Read /Write	Default	Description
31:28	/	/	/
27:16	R/W	0x5DB	<p>AVS_CNT1_D.</p> <p>Divisor N for AVS Counter 1</p> <p>AVS CN1 CLK=24MHz/Divisor_N1.</p> <p>Divisor N1 = Bit [27:16] + 1.</p> <p>The number N is from 1 to 0x7ff. The zero value is reserved.</p> <p>The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (\geq N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again.</p> <p>Note: It can be configured by software at any time.</p>
15:12	/	/	/
11:0	R/W	0x5DB	<p>AVS_CNT0_D.</p> <p>Divisor N for AVS Counter 0</p> <p>AVS CNO CLK=24MHz/Divisor_NO.</p> <p>Divisor NO = Bit [11:0] + 1</p> <p>The number N is from 1 to 0x7ff. The zero value is reserved.</p> <p>The internal 33-bits counter engine will maintain another 12-bits counter. The 12-bits counter is used for counting the cycle number of one 24Mhz clock. When the 12-bits counter reaches (\geq N) the divisor value, the internal 33-bits counter register will increase 1 and the 12-bits counter will reset to zero and restart again.</p> <p>Note: It can be configured by software at any time.</p>

WATCHDOG 0 IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0xA0		Register Name: WDOG0_IRQ_EN_REG	
Bit	Read/Writ	Default/H	Description

	e	ex	
31:1	/	/	/
0	R/W	0x0	<p>WDOG0_IRQ_EN.</p> <p>Watchdog 0 Interrupt Enable.</p> <p>0: No effect, 1: Watchdog 0 interrupt enable.</p>

WATCHDOG 0 STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0xA4			Register Name: WDOG0_IRQ_STA_REG
Bit	Read/Writ e	Default/H ex	Description
31:1	/	/	/
0	R/W	0x0	<p>WDOG0_IRQ_PEND.</p> <p>Watchdog 0 IRQ Pending. Set 1 to the bit will clear it.</p> <p>0: No effect, 1: Pending, Watchdog 0 interval value is reached.</p>

WATCHDOG 0 CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0xB0			Register Name: WDOG0_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:1	R/W	0x0	/
0	R/W	0x0	<p>WDOG0_RSTART.</p> <p>Watchdog 0 Restart.</p> <p>0: No effect, 1: Restart the Watchdog 0.</p>

WATCHDOG 0 CONFIGURATION REGISTER (DEFAULT: 0X00000000)

Offset:0xB4			Register Name: WDOG0_CFG_REG
Bit	Read/Writ	Default/H	Description

	e	ex	
31:2	/	/	/
1:0	R/W	0x1	<p>WDOG0_CONFIG.</p> <p>00: /</p> <p>01: to whole system</p> <p>10: only interrupt</p> <p>11: /</p>

WATCHDOG 0 MODE REGISTER (DEFAULT: 0X00000000)

Offset:0xB8			Register Name: WDOG0_MODE_REG
Bit	Read/Writ e	Default/H ex	Description
31:8	/	/	/
7:4	R/W	0x0	<p>WDOG0_INTV_VALUE.</p> <p>Watchdog 0 Interval Value.</p> <p>Watchdog 0 clock source is <i>OSC24M / 750</i>. If the clock source is turned off, Watchdog 0 will not work.</p> <p>0000: 16000 cycles (0.5s)</p> <p>0001: 32000 cycles (1s)</p> <p>0010: 64000 cycles (2s)</p> <p>0011: 96000 cycles (3s)</p> <p>0100: 128000 cycles (4s)</p> <p>0101: 160000 cycles (5s)</p> <p>0110: 192000 cycles (6s)</p> <p>0111: 256000 cycles (8s)</p> <p>1000: 320000 cycles (10s)</p> <p>1001: 384000 cycles (12s)</p> <p>1010: 448000 cycles (14s)</p> <p>1011: 512000 cycles (16s)</p>

			others: /
3:1	/	/	/
0	R/W	0x0	WDOG0_EN. Watchdog 0 Enable. 0: No effect; 1: Enable the Watchdog 0.

3.7 PWM

3.7.1 Overview

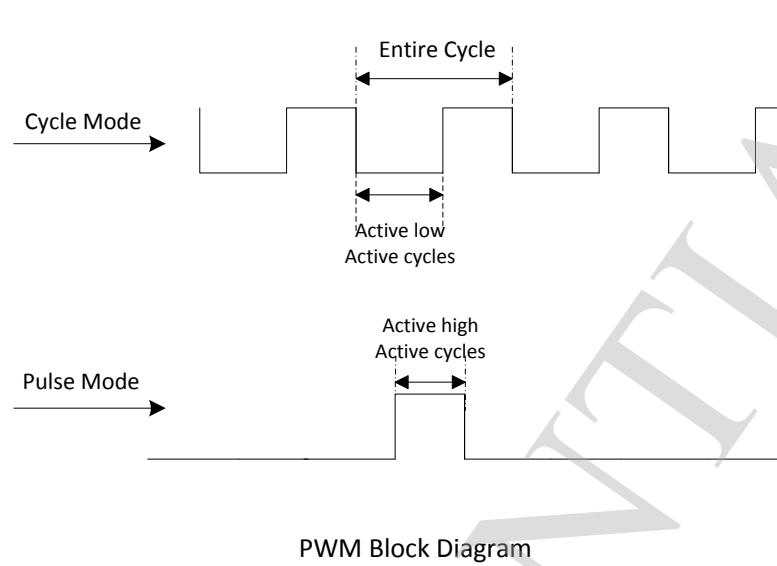
The A23 comes with three PWMs.

The output of the PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up-counter. If the counter reaches the value stored in the channel period register, it resets. At the beginning of a count period cycle, the PWMOUT is set to active state and count from 0x0000.

The PWM divider divides the clock(24MHz) by 1~4096 according to the pre-scalar bits in the PWM control register.

In PWM cycle mode, the output will be a square waveform, the frequency is set to the period register. In PWM pulse mode, the output will be a positive pulse or a negative pulse.

3.7.2 Block Diagram



PWM Block Diagram

3.7.3 PWM Register List

Module Name	Base Address
PWM	0x01C21400

Register Name	Offset	Description
PWM_CTRL_REG	0x0	PWM Control Register
PWM_CH0_PERIOD	0x4	PWM Channel 0 Period Register
PWM_CH1_PERIOD	0x8	PWM Channel 1 Period Register

3.7.4 PWM Register Description

PWM CONTROL REGISTER (DEFAULT: 0X00000000)

Offset: 0x0			Register Name: PWM_CTRL_REG
Bit	Read/ Write	Default /Hex	Description
31:30	/	/	/.
29	RO	0x0	<p>PWM1_RDY.</p> <p>PWM1 period register ready.</p> <p>0: PWM1 period register is ready to write, 1: PWM1 period register is busy.</p>
28	RO	0x0	<p>PWM0_RDY.</p> <p>PWM0 period register ready.</p> <p>0: PWM0 period register is ready to write, 1: PWM0 period register is busy.</p>
27:25	/	/	/
24	R/W	0x0	<p>PWM1_BYPASS.</p> <p>PWM CH1 bypass enable.</p> <p>If the bit is set to 1, PWM1's output is OSC24MHz.</p> <p>0: disable 1: enable</p>
23	R/W	0x0	<p>PWM_CH1_PULSE_OUT_START.</p> <p>PWM Channel 1 pulse output start.</p> <p>0: no effect, 1: output 1 pulse.</p> <p>The pulse width should be according to the period 1 register[15:0],and the pulse state should be according to the active state.</p>

			After the pulse is finished, the bit will be cleared automatically.
22	R/W	0x0	PWM_CH1_MODE. PWM Channel 1 mode. 0: cycle mode, 1: pulse mode.
21	R/W	0x0	PWM_CH1_CLK_GATING Gating the Special Clock for PWM1(0: mask, 1: pass).
20	R/W	0x0	PWM_CH1_ACT_STATE. PWM Channel 1 Active State. 0: Low Level, 1: High Level.
19	R/W	0x0	PWM_CH1_EN. PWM Channel 1 Enable. 0: Disable, 1: Enable.
18:15	R/W	0x0	PWM_CH1_PRESCAL. PWM Channel 1 Prescalar. These bits should be setting before the PWM Channel 1 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k

			1100: /72k 1101: / 1110: / 1111: /1
14:10	/	/	/
9	R/W	0x0	PWM0_BYPASS. PWM CH0 bypass enable. If the bit is set to 1, PWM0's output is OSC24MHz. 0: disable, 1: enable.
8	R/W	0x0	PWM_CH0_PUL_START. PWM Channel 0 pulse output start. 0: no effect, 1: output 1 pulse. The pulse width should be according to the period 0 register[15:0],and the pulse state should be according to the active state. After the pulse is finished, the bit will be cleared automatically.
7	R/W	0x0	PWM_CHANNEL0_MODE. 0: cycle mode, 1: pulse mode.
6	R/W	0x0	SCLK_CH0_GATING. Gating the Special Clock for PWM0(0: mask, 1: pass).
5	R/W	0x0	PWM_CH0_ACT_STA. PWM Channel 0 Active State. 0: Low Level, 1: High Level.
4	R/W	0x0	PWM_CH0_EN. PWM Channel 0 Enable. 0: Disable, 1: Enable.
3:0	R/W	0x0	PWM_CH0_PRESCAL.

		PWM Channel 0 Prescalar. These bits should be setting before the PWM Channel 0 clock gate on. 0000: /120 0001: /180 0010: /240 0011: /360 0100: /480 0101: / 0110: / 0111: / 1000: /12k 1001: /24k 1010: /36k 1011: /48k 1100: /72k 1101: / 1110: / 1111: /1
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PWM CHANNEL 0 PERIOD REGISTER

Offset: 0x4			Register Name: PWM_CHO_PERIOD
Bit	Read/ Write	Default /Hex	Description
31:16	R/W	x	<p>PWM_CHO_ENTIRE_CYS</p> <p>Number of the entire cycles in the PWM clock.</p> <p>0 = 1 cycle</p> <p>1 = 2 cycles</p> <p>.....</p>

			<p>$N = N+1$ cycles</p> <p>If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK(PWM CLK = 24MHz/pre-scale).</p>
15:0	R/W	x	<p>PWM_CH0_ENTIRE_ACT_CYS</p> <p>Number of the active cycles in the PWM clock.</p> <p>0 = 0 cycle</p> <p>1 = 1 cycles</p> <p>.....</p> <p>$N = N$ cycles</p>

Note: the active cycles should be no larger than the period cycles.

PWM CHANNEL 1 PERIOD REGISTER

Offset: 0x8			Register Name: PWM_CH1_PERIOD
Bit	Read/ Write	Default /Hex	Description
31:16	R/W	x	<p>PWM_CH1_ENTIRE_CYS</p> <p>Number of the entire cycles in the PWM clock.</p> <p>0 = 1 cycle</p> <p>1 = 2 cycles</p> <p>.....</p> <p>$N = N+1$</p> <p>If the register need to be modified dynamically, the PCLK should be faster than the PWM CLK(PWM CLK = 24MHz/pre-scale).</p>
15:0	R/W	x	<p>PWM_CH1_ENTIRE_CYS</p> <p>Number of the active cycles in the PWM clock.</p> <p>0 = 0 cycle</p> <p>1 = 1 cycles</p> <p>.....</p>

			N = N cycles
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CONFIDENTIAL

3.8 High Speed Timer

3.8.1 Overview

High Speed Timer clock source is fixed to AHBCLK, which is much higher than OSC24M. Compared with other timers, High Speed Timer clock source is synchronized with AHB clock, and when the relevant bit in the control register is set to 1, timer goes into the test mode, which is used to System Simulation. When the current value in both LO and HI Current Value Register are counting down to zero, the timer will generate interrupt if set interrupt enable bit.

3.8.2 High Speed Timer Register List

Module Name	Base Address
High Speed Timer	0x01C60000

Register Name	Offset	Description
HS_TMR IRQ_EN_REG	0x0	HS Timer IRQ Enable Register
HS_TMR IRQ_STAS_REG	0x4	HS Timer Status Register
HS_TMR0_CTRL_REG	0x10	HS Timer Control Register
HS_TMR0_INTV_LO_REG	0x14	HS Timer Interval Value Low Register
HS_TMR0_INTV_HI_REG	0x18	HS Timer Interval Value High Register
HS_TMR0_CURNT_LO_REG	0x1C	HS Timer Current Value Low Register
HS_TMR0_CURNT_HI_REG	0x20	HS Timer Current Value High Register

3.8.3 High Speed Timer Register Description

HS TIMER IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x0			Register Name: HS_TMR_IRQ_EN_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	HS_TMR_INT_EN. High Speed Timer Interrupt Enable. 0: No effect; 1: High Speed Timer Interval Value reached interrupt enable.

HS TIMER IRQ STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x4			Register Name: HS_TMR_IRQ_STAS_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	HS_TMR_IRQ_PEND. High Speed Timer IRQ Pending. Set 1 to the bit will clear it. 0: No effect; 1: Pending, High speed timer interval value is reached.

HS TIMER CONTROL REGISTER (DEFAULT: 0X00000000)

Offset:0x10			Register Name: HS_TMR0_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description

	e	ex	
31	R/W	0x0	<p>HS_TMR_TEST.</p> <p>High speed timer test mode. In test mode, the low register should be set to 0x1, the high register will down counter. The counter needs to be reloaded.</p> <p>0: normal mode; 1: test mode.</p>
30: 8	/	/	/
7	R/W	0x0	<p>HS_TMR_MODE.</p> <p>High Speed Timer mode.</p> <p>0: Continuous mode. When interval value reached, the timer will not disable automatically. 1: Single mode. When interval value reached, the timer will disable automatically.</p>
6:4	R/W	0x0	<p>HS_TMR_CLK</p> <p>Select the pre-scale of the high speed timer clock sources.</p> <p>000: /1 001: /2 010: /4 011: /8 100: /16 101: / 110: / 111: /</p>
3:2	/	/	/
1	R/W	0x0	<p>HS_TMR_RELOAD.</p> <p>High Speed Timer Reload.</p> <p>0: No effect, 1: Reload High Speed Timer Interval Value.</p>
0	R/W	0x0	HS_TMR_EN.

			<p>High Speed Timer Enable.</p> <p>0: Stop/Pause, 1: Start.</p> <p>If the timer is started, it will reload the interval value to internal register, and the current counter will count from interval value to 0.</p> <p>If the current counter does not reach the zero, the timer enable bit is set to "0", the current value counter will pause. At least wait for 2 cycles, the start bit can be set to 1.</p> <p>In timer pause state, the interval value register can be modified. If the timer is started again, and the Software hope the current value register to down-count from the new interval value, the reload bit and the enable bit should be set to 1 at the same time.</p>
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HS TIMER INTERVAL VALUE LO REGISTER

Offset:0x14			Register Name: HS_TMR_INTV_LO_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	x	<p>HS_TMR_INTV_VALUE_LO.</p> <p>High Speed Timer Interval Value [31:0].</p>

HS TIMER INTERVAL VALUE HI REGISTER

Offset:0x18			Register Name: HS_TMR_INTV_HI_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:0	R/W	x	<p>HS_TMR_INTV_VALUE_HI.</p> <p>High Speed Timer Interval Value [55:32].</p>

Note: the interval value register is a 56-bit register. When read or write the interval value, the Lo register should be read or write first. And the Hi register should be written after the Lo register.

HS TIMER CURRENT VALUE LO REGISTER

Offset:0x1C			Register Name: HS_TMR_CURNT_LO_REG
Bit	Read/Writ e	Default/H ex	Description
31:0	R/W	x	HS_TMR_CUR_VALUE_LO. High Speed Timer Current Value [31:0].

HS TIMER CURRENT VALUE HI REGISTER

Offset:0x20			Register Name: HS_TMR_CURNT_HI_REG
Bit	Read/Writ e	Default/H ex	Description
31:24	/	/	/
23:0	R/W	x	HS_TMR_CUR_VALUE_HI. High Speed Timer Current Value [55:32].

Note:

HS timer current value is a 56-bit down-counter (from interval value to 0).

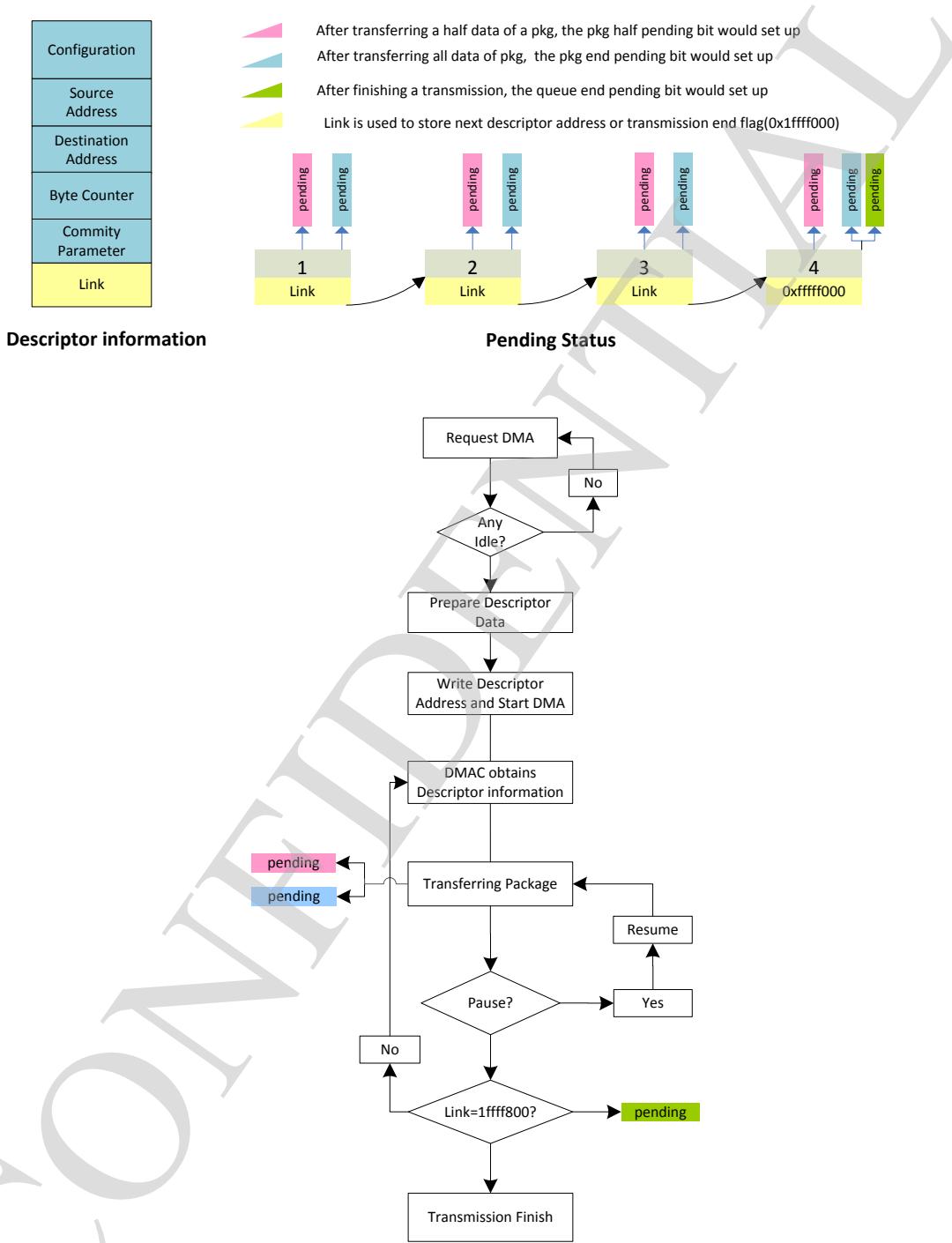
The current value register is a 56-bit register. When read or write the current value, the Lo register should be read or write first.

3.9 DMA

3.9.1 Overview

The A23 supports 8-channel DMA. Each DMA channel can generate interrupts, and each referenced DMA channel can generate interrupts according to different pending status, and the configuration information of every DMA channel will be stored in the DDR or SRAM. After a DMA transfer starts, the address information in the DDR or SRAM will be described in *DMA Channel Descriptor Address Register*.

3.9.2 Block Diagram



3.9.3 DRQ Type and Port Corresponding Relation

Source DRQ Type		Destination DRQ Type	
port0	SRAM	port0	SRAM
port1	SDRAM	port1	SDRAM
port2	/	port2	/
port3	DAUDIO_0-RX	port3	DAUDIO_0-TX
port4	DAUDIO_1-RX	port4	DAUDIO_1-TX
port5	NAND	port5	NAND
port6	UART0-RX	port6	UART0-TX
port7	UART1-RX	port7	UART1-TX
port8	UART2-RX	port8	UART2-TX
port9	UART3-RX	port9	UART3-TX
port10	UART4-RX	port10	UART4-TX
port11	/	port11	/
port12	/	port12	TCON_0
port13	/	port13	/
port14	/	port14	/
port15	AUDIO CODEC	port15	AUDIO CODEC
port16	/	port16	/
port17	OTG_EP1	port17	OTG_EP1
port18	OTG_EP2	port18	OTG_EP2
port19	OTG_EP3	port19	OTG_EP3
port20	OTG_EP4	port20	OTG_EP4
port21	OTG_EP5	port21	OTG_EP5
port22	/	port22	/
port23	SPI_0-RX	port23	SPI_0-TX

port24	SPI_1-RX	port24	SPI_1-TX
port25	/	port25	/
port26	/	port26	/
port27	/	port27	/
port28	/	port28	/
port29	/	port29	/
Port30	/	Port30	/

3.9.4 DMA Description

In this section, the DMA descriptor registers will be introduced in detail.

When starting a DMA transmission, the module data are transferred as packages, which have the link data information. And, by reading the DMA Status Register, the status of a DMA channel could be known. Reading back the descriptor address register, the value is the link data in the transferring package. If only the value is equal to 0xfffff800, then it can be regarded as NULL, which means the package is the last package in this DMA transmission. Otherwise, the value means the start address of the next package. And, the Descriptor Address Register can be changed during a package transferring.

When transferring the half of a package, the relevant pending bit will be set up automatically, and if the corresponding interrupt is enabled, DMA generates an interrupt to the system. The similar thing would occur when transferring a package completely. Meanwhile, if DMA have transferred the last package in the data, the relevant pending bit would be set up, and generates an interrupt if the corresponding interrupt is enabled. The flow-process diagram is showed in Block Diagram section.

During a DMA transmission, the configuration could be obtained via the Configuration Register. And, behind the address of the configuration register in DDR or SRAM, there are some registers including other information of a DMA transmission. The structure chart is showed in Block Diagram section. Also, other information of a transferring data can be obtained by reading the Current Source Address Register, Current Destination Address Register and Byte Counter Left Register. The configuration must be word-aligning.

The transferring data would be paused when setting up the relevant Pause Register, if coming up emergency. And the pausing data could be presumable when set 0 to the same bit in Pause Register.

3.9.5 DMA Register List

Module Name	Base Address
DMA	0x01C02000

Register Name	Offset	Description
DMA_IRQ_EN_REG	0x0	DMA IRQ Enable Register
DMA_IRQ_PEND_REG	0x10	DMA IRQ Pending Register
DMA_STA_REG	0x30	DMA Status Register
DMA_EN_REG	0x100+N*0x40	DMA Channel Enable Register (N=0~7)
DMA_PAU_REG	0x100+N*0x40+0x4	DMA Channel Pause Register (N=0~7)
DMA_DESC_ADDR_REG	0x100+N*0x40+0x8	DMA Channel Start Address Register (N=0~7)
DMA_CFG_REG	0x100+N*0x40+0xC	DMA Channel Configuration Register (N=0~7)
DMA_CUR_SRC_REG	0x100+N*0x40+0x10	DMA Channel Current Source Register (N=0~7)
DMA_CUR_DEST_REG	0x100+N*0x40+0x14	DMA Channel Current Destination Register (N=0~7)
DMA_BCNT_LEFT_REG	0x100+N*0x40+0x18	DMA Channel Byte Counter Left Register (N=0~7)
DMA_PARA_REG	0x100+N*0x40+0x1C	DMA Channel Parameter Register (N=0~7)

3.9.6 DMA Register Description

DMA IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x0			Register Name: DMA_IRQ_EN_REG
Bit	Read/Writ e	Default/H ex	Description
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_EN DMA 7 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
29	R/W	0x0	DMA7_PKG_IRQ_EN DMA 7 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
28	R/W	0x0	DMA7_HLAF_IRQ_EN DMA 7 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_EN DMA 6 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
25	R/W	0x0	DMA6_PKG_IRQ_EN DMA 6 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
24	R/W	0x0	DMA6_HLAF_IRQ_EN DMA 6 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_EN

			DMA 5 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
21	R/W	0x0	DMA5_PKG_IRQ_EN DMA 5 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
20	R/W	0x0	DMA5_HLAF_IRQ_EN DMA 5 Half package Transfer Interrupt Enable. 0: Disable, 1: Enable.
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_EN DMA 4 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
17	R/W	0x0	DMA4_PKG_IRQ_EN DMA 4 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
16	R/W	0x0	DMA4_HLAF_IRQ_EN DMA 4 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_EN DMA 3 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
13	R/W	0x0	DMA3_PKG_IRQ_EN DMA 3 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
12	R/W	0x0	DMA3_HLAF_IRQ_EN DMA 3 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.

11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_EN DMA 2 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
9	R/W	0x0	DMA2_PKG_IRQ_EN DMA 2 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
8	R/W	0x0	DMA2_HLAF_IRQ_EN DMA 2 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_EN DMA 1 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
5	R/W	0x0	DMA1_PKG_IRQ_EN DMA 1 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
4	R/W	0x0	DMA1_HLAF_IRQ_EN DMA 1 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable.
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_EN DMA 0 Queue End Transfer Interrupt Enable. 0: Disable, 1: Enable.
1	R/W	0x0	DMA0_PKG_IRQ_EN DMA 0 Package End Transfer Interrupt Enable. 0: Disable, 1: Enable.
0	R/W	0x0	DMA0_HLAF_IRQ_EN

			DMA 0 Half Package Transfer Interrupt Enable. 0: Disable, 1: Enable
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DMA IRQ PENDING STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x10			Register Name: DMA_IRQ_PEND_REG
Bit	Read/Writ e	Default/H ex	Description
31	/	/	/
30	R/W	0x0	DMA7_QUEUE_IRQ_PEND. DMA 7 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
29	R/W	0x0	DMA7_PKG_IRQ_PEND DMA 7 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
28	R/W	0x0	DMA7_HLAF_IRQ_PEND. DMA 7 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
27	/	/	/
26	R/W	0x0	DMA6_QUEUE_IRQ_PEND. DMA 6 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
25	R/W	0x0	DMA6_PKG_IRQ_PEND DMA 6 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
24	R/W	0x0	DMA6_HLAF_IRQ_PEND. DMA 6 Half Package Transfer Interrupt Pending. Set 1 to the

			bit will clear it. 0: No effect, 1: Pending.
23	/	/	/
22	R/W	0x0	DMA5_QUEUE_IRQ_PEND. DMA 5 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
21	R/W	0x0	DMA5_PKG_IRQ_PEND DMA 5 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
20	R/W	0x0	DMA5_HLAF_IRQ_PEND. DMA 5 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
19	/	/	/
18	R/W	0x0	DMA4_QUEUE_IRQ_PEND. DMA 4 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
17	R/W	0x0	DMA4_PKG_IRQ_PEND DMA 4 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
16	R/W	0x0	DMA4_HLAF_IRQ_PEND. DMA 4 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
15	/	/	/
14	R/W	0x0	DMA3_QUEUE_IRQ_PEND. DMA 3 Queue End Transfer Interrupt Pending. Set 1 to the bit

			will clear it. 0: No effect, 1: Pending.
13	R/W	0x0	DMA3_PKG_IRQ_PEND DMA 3 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
12	R/W	0x0	DMA3_HLAF_IRQ_PEND. DMA 3 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
11	/	/	/
10	R/W	0x0	DMA2_QUEUE_IRQ_PEND. DMA 2 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
9	R/W	0x0	DMA2_PKG_IRQ_PEND DMA 2 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
8	R/W	0x0	DMA2_HLAF_IRQ_PEND. DMA 2 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
7	/	/	/
6	R/W	0x0	DMA1_QUEUE_IRQ_PEND. DMA 1 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
5	R/W	0x0	DMA1_PKG_IRQ_PEND DMA 1 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it.

			0: No effect, 1: Pending.
4	R/W	0x0	DMA1_HLAF_IRQ_PEND. DMA 1 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
3	/	/	/
2	R/W	0x0	DMA0_QUEUE_IRQ_PEND. DMA 0 Queue End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
1	R/W	0x0	DMA0_PKG_IRQ_PEND DMA 0 Package End Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.
0	R/W	0x0	DMA0_HLAF_IRQ_PEND. DMA 0 Half Package Transfer Interrupt Pending. Set 1 to the bit will clear it. 0: No effect, 1: Pending.

DMA STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x30			Register Name: DMA_STA_REG
Bit	Read/Writ e	Default/H ex	Description
31:8	/	/	/
7	RO	0x0	DMA7_STATUS DMA Channel 7 Status. 0: Idle, 1: Busy.
6	RO	0x0	DMA6_STATUS DMA Channel 6 Status. 0: Idle, 1: Busy.

5	RO	0x0	DMA5_STATUS DMA Channel 5 Status. 0: Idle, 1: Busy.
4	RO	0x0	DMA4_STATUS DMA Channel 4 Status. 0: Idle, 1: Busy.
3	RO	0x0	DMA3_STATUS DMA Channel 3 Status. 0: Idle, 1: Busy.
2	RO	0x0	DMA2_STATUS DMA Channel 2 Status. 0: Idle, 1: Busy.
1	RO	0x0	DMA1_STATUS DMA Channel 1 Status. 0: Idle, 1: Busy.
0	RO	0x0	DMA0_STATUS DMA Channel 0 Status. 0: Idle, 1: Busy.

DMA CHANNEL ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x100+N*0x40+0x0 (N=0~7)			Register Name: DMA0_EN_REG
Bit	Read/Writ e	Default/H ex	Description
31:1	/	/	/
0	R/W	0x0	DMA_EN. DMA Channel Enable 0: Disable, 1: Enable.

DMA CHANNEL PAUSE REGISTER (DEFAULT: 0X00000000)

Offset:0x100+N*0x40+0x4 (N=0~7)			Register Name: DMA_PAU_REG
Bit	Read/Writ e	Default/H ex	Description
31:1	/	/	/
0	R/W	0x0	DMA_PAUSE. Pausing DMA Channel Transfer Data. 0: Resume Transferring, 1: Pause Transferring.

DMA CHANNEL DESCRIPTOR ADDRESS REGISTER

Offset:0x100+N*0x40+0x8 (N=0~7)			Register Name: DMA_DESC_ADDR_REG
Bit	Read/Writ e	Default/H ex	Description
31:0	R/W	x	DMA_DESC_ADDR DMA Channel Descriptor Address.

DMA CHANNEL CONFIGURATION REGISTER (DEFAULT: 0X00000000)

Offset:0x100+N*0x40+0xC (N=0~7)			Register Name: DMA_CFG_REG
Bit	Read /Write	Default/H ex	Description
31:2 7	/	/	/
26:2 5	RO	0x0	DMA_DEST_DATA_WIDTH. DMA Destination Data Width. 00: 8-bit 01: 16-bit

			10: 32-bit 11: /
24:2 3	RO	0x0	DMA_DEST_BST_LEN. DMA Destination Burst Length. 00: 1 01: / 10: 8 11: /
22:2 1	RO	0x0	DMA_ADDR_MODE. DMA Destination Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: / 0x3: /
20:1 6	RO	0x0	DMA_DEST_DRQ_TYPE. DMA Destination DRQ Type The details in DRQ Type and Port Corresponding Relation.
15:1 1	/	/	/
10:9	RO	0x0	DMA_SRC_DATA_WIDTH. DMA Source Data Width. 00: 8-bit 01: 16-bit 10: 32-bit 11: /
8:7	RO	0x0	DMA_SRC_BST_LEN. DMA Source Burst Length. 00: 1 01: /

			10: 8 11: /
6:5	RO	0x0	DMA_SRC_ADDR_MODE. DMA Source Address Mode 0x0: Linear Mode 0x1: IO Mode 0x2: / 0x3: /
4:0	RO	0x0	DMA_SRC_DRQ_TYPE. DMA Source DRQ Type The details in DRQ Type and Port Corresponding Relation.

Note:

If the DRQ type is dram, then, the corresponding burst length will be fixed, and the options will be invalid.

The address of the *DMA Channel Configuration Register* must be word-aligned.

DMA CHANNEL CURRENT SOURCE ADDRESS REGISTER

Offset:0x100+N*0x40+0x10 (N=0~7)			Register Name: DMA_CUR_SRC_REG
Bit	Read/Writ e	Default/H ex	Description
31:0	RO	0x0	DMA_CUR_SRC. DMA Channel Current Source Address, read only.

Note: The address of the DMA Channel Current Source Address Register must be word-aligned.

DMA CHANNEL CURRENT DESTINATION ADDRESS REGISTER

Offset:0x100+N*0x40+0x14 (N=0~7)			Register Name: DMA_CUR_DEST_REG
Bit	Read/Writ e	Default/H ex	Description

31:0	RO	0x0	DMA_CUR_DEST. DMA Channel Current Destination Address, read only.
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Note: The address of the DMA Channel Current Destination Address Register must be word-aligned.

DMA CHANNEL BYTE COUNTER LEFT REGISTER

Offset:0x100+N*0x40+0x18 (N=0~7)			Register Name: DMA_BCNT_LEFT_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 5	/	/	/
24:0	RO	0x0	DMA_BCNT_LEFT. DMA Channel Byte Counter Left, read only.

Note: The address of the DMA Channel Byte Counter Left Register must be word-aligned.

DMA CHANNEL PARAMETER REGISTER

Offset:0x100+N*0x40+0x1C (N=0~7)			Register Name: DMA_PARA_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	/	/	/
15:8	RO	0x0	DATA_BLK_SIZE. Data Block Size <i>N</i> .
7:0	RO	0x0	WAIT_CYC. Wait Clock Cycles <i>n</i> .

Note:

The number of data block size usually depends on the capacity of the device's FIFO in the practical application.

The data block size must be multiple of **burst*width** (byte). For example: if burst is 4 and the width is 32-bit, so

the data block size must be **$m*16$** (byte), i.e. **$N = m * 16$** .

When DMA controller has completed transferring **N** bytes data, and waiting **n** clock cycles to check the DRQ signal.

This register is only effective to devices, and the *Data Block Size N* should be **0** if it is less than **32**.

CONFIDENTIAL

3.10 GIC

For details about GIC, please refer to the GIC PL400 technical reference manual and ARM GIC Architecture Specification V2.0.

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3.10.1 Interrupt Source

Interrupt Source	SRC	Vector	FIQ	Description
SGI 0	0	0x0000		SGI 0 interrupt
SGI 1	1	0x0004		SGI 1 interrupt
SGI 2	2	0x0008		SGI 2 interrupt
SGI 3	3	0x000C		SGI 3 interrupt
SGI 4	4	0x0010		SGI 4 interrupt
SGI 5	5	0x0014		SGI 5 interrupt
SGI 6	6	0x0018		SGI 6 interrupt
SGI 7	7	0x001C		SGI 7 interrupt
SGI 8	8	0x0020		SGI 8 interrupt
SGI 9	9	0x0024		SGI 9 interrupt
SGI 10	10	0x0028		SGI 10 interrupt
SGI 11	11	0x002C		SGI 11 interrupt
SGI 12	12	0x0030		SGI 12 interrupt
SGI 13	13	0x0034		SGI 13 interrupt
SGI 14	14	0x0038		SGI 14 interrupt
SGI 15	15	0x003C		SGI 15 interrupt
PPI 0	16	0x0040		PPI 0 interrupt
PPI 1	17	0x0044		PPI 1 interrupt
PPI 2	18	0x0048		PPI 2 interrupt
PPI 3	19	0x004C		PPI 3 interrupt
PPI 4	20	0x0050		PPI 4 interrupt
PPI 5	21	0x0054		PPI 5 interrupt
PPI 6	22	0x0058		PPI 6 interrupt
PPI 7	23	0x005C		PPI 7 interrupt

Interrupt Source	SRC	Vector	FIQ	Description
PPI 8	24	0x0060		PPI 8 interrupt
PPI 9	25	0x0064		PPI 9 interrupt
PPI 10	26	0x0068		PPI 10 interrupt
PPI 11	27	0x006C		PPI 11 interrupt
PPI 12	28	0x0070		PPI 12 interrupt
PPI 13	29	0x0074		PPI 13 interrupt
PPI 14	30	0x0078		PPI 14 interrupt
PPI 15	31	0x007C		PPI 15 interrupt
UART 0	32	0x0080		UART 0 interrupt
UART 1	33	0x0084		UART 1 interrupt
UART 2	34	0x0088		UART 2 interrupt
UART 3	35	0x008C		UART 3 interrupt
UART 4	36	0x0090		UART 4 interrupt
/	37	0x0094		/
TWI 0	38	0x0098		TWI 0 interrupt
TWI 1	39	0x009C		TWI 1 interrupt
TWI 2	40	0x00A0		TWI 2 interrupt
/	41	0x00A4		/
/	42	0x00A8		/
PA_EINT	43	0x00AC		PA_EINT interrupt
/	44	0x00B0		/
DAUDIO-0	45	0x00B4		DAUDIO-0 interrupt
DAUDIO-1	46	0x00B8		DAUDIO-1 interrupt
PB_EINT	47	0x00BC		PB_EINT interrupt
/	48	0x00C0		/
PG_EINT	49	0x00C4		PG_EINT interrupt
Timer 0	50	0x00C8		Timer 0 interrupt

Interrupt Source	SRC	Vector	FIQ	Description
Timer 1	51	0x00CC		Timer 1 interrupt
/	52	0x00D0		/
/	53	0x00D4		/
/	54	0x00D8		/
/	55	0x00DC		/
/	56	0x00E0		/
Watchdog	57	0x00E4		Watchdog interrupt
/	58	0x00E8		/
/	59	0x00EC		/
/	60	0x00F0		/
Audio Codec	61	0x00F4		Analogy Audio Codec interrupt
LRADC	62	0x00F8		LRADC interrupt
/	63	0x00FC		/
External NMI	64	0x100		External Non-Mask Interrupt
R_timer 0	65	0x104		R_timer 0 interrupt
R_timer 1	66	0x108		R_timer 1 interrupt
/	67	0x010C		/
R_watchdog	68	0x0110		R_watchdog interrupt
/	69	0x0114		/
R_UART	70	0x0118		R_UART interrupt
R_RSB	71	0x011C		R_RSB interrupt
R_Alarm 0	72	0x0120		R_Alarm 0 interrupt
R_Alarm 1	73	0x0124		R_Alarm 1 interrupt
/	74	0x0128		/
/	75	0x012C		/
R_TWI	76	0x0130		R_TWI interrupt
R_PG_LINT	77	0x0134		R_PG_LINT interrupt

Interrupt Source	SRC	Vector	FIQ	Description
HMIC	78	0x0138		HMIC interrupt
/	79	0x013C		/
/	80	0x0140		/
M-box	81	0x0144		M-box interrupt
DMA	82	0x0148		DMA channel interrupt
HS Timer	83	0x014C		HS Timer interrupt
/	84	0x0150		/
/	85	0x0154		/
/	86	0x0158		/
/	87	0x015C		/
/	88	0x0160		/
/	89	0x0164		/
VE	90	0x0168		VE interrupt
/	91	0x016C		/
SD/MMC 0	92	0x0170		SD/MMC Host Controller 0 interrupt
SD/MMC 1	93	0x0174		SD/MMC Host Controller 1 interrupt
SD/MMC 2	94	0x0178		SD/MMC Host Controller 2 interrupt
/	95	0x017C		/
/	96	0x0180		/
SPI 0	97	0x0184		SPI 0 interrupt
SPI 1	98	0x0188		SPI 1 interrupt
/	99	0x018C		/
/	100	0x0190		/
/	101	0x0194		/
NAND	102	0x0198		NAND Flash Controller interrupt
USB -OTG	103	0x019C		USB-OTG interrupt
USB-EHCI0	104	0x01A0		USB-EHCI0 interrupt

Interrupt Source	SRC	Vector	FIQ	Description
USB-OHCI0	105	0x01A4		USB-OHCI0 interrupt
/	106	0x01A8		/
/	107	0x01AC		/
/	108	0x01B0		/
/	109	0x01B4		/
/	110	0x01B8		/
/	111	0x01BC		/
/	112	0x01C0		/
/	113	0x01C4		/
/	114	0x01C8		/
/	115	0x01CC		/
CSI	116	0x01D0		CSI interrupt
CSI_CCI	117	0x01D4		CSI_CCI interrupt
LCD	118	0x01D8		LCD Controller interrupt
/	119	0x01DC		/
/	120	0x01E0		/
MIPI DSI	121	0x01E4		MIPI DSI interrupt
/	122	0x01E8		/
DRC 0/1	123	0x01EC		DRC 0/1 interrupt
/	124	0x01F0		/
DE_FE	125	0x01F4		DE_FE interrupt
/	126	0x01F8		/
DE_BE	127	0x01FC		DE_BE interrupt
/	128	0x0200		/
GPU-GP	129	0x0204		GPU-GP interrupt
GPU-GPMMU	130	0x0208		GPU-GPMMU interrupt
GPU-PP0	131	0x020C		GPU-PP0 interrupt

Interrupt Source	SRC	Vector	FIQ	Description
GPU-PPMMU0	132	0x0210		GPU-PPMMU0 interrupt
GPU-PMU	133	0x0214		GPU-PMU interrupt
GPU-PP1	134	0x0218		GPU-PP1 interrupt
GPU-PPMMU1	135	0x021C		GPU-PPMMU1 interrupt
/	136	0x0220		/
/	137	0x0224		/
/	138	0x0228		/
/	139	0x022C		/
CTI0	140	0x0230		CTI0 interrupt
CTI1	141	0x0234		CTI1 interrupt
CTI2	142	0x0238		CTI2 interrupt
CTI3	143	0x023C		CTI3 interrupt
COMMTX0	144	0x0240		COMMTX0 interrupt
COMMTX1	145	0x0244		COMMTX1 interrupt
COMMTX2	146	0x0248		COMMTX2 interrupt
COMMTX3	147	0x024C		COMMTX3 interrupt
COMMRX0	148	0x0250		COMM RX0 interrupt
COMM RX1	149	0x0254		COMM RX1 interrupt
COMM RX2	150	0x0258		COMM RX2 interrupt
COMM RX3	151	0x025C		COMM RX3 interrupt
PMU0	152	0x0260		PMU0 interrupt
PMU1	153	0x0264		PMU1 interrupt
PMU2	154	0x0268		PMU2 interrupt
PMU3	155	0x026C		PMU3 interrupt
AXI_ERROR	156	0x0270		AXI_ERROR interrupt

3.11 RTC

3.11.1 Overview

The real time clock (RTC) is for calendar usage. It is built around a 30-bit counter and used to count elapsed time in YY-MM-DD and HH-MM-SS. The unit can be operated by the backup battery while the system power is off. It has a built-in leap year generator and a independent power pin (RTC_VIO).

The alarm generates an alarm signal at a specified time in the power-off mode or normal operation mode. In normal operation mode, both the alarm interrupt and the power management wakeup are activated. In power-off mode, the power management wakeup signal is activated. Two kinds of alarm are supported here: Alarm 0 is a general alarm whose counter is based on seconds, while Alarm 1 is a weekly alarm whose counter is based on the real time.

The 32768Hz oscillator is used only to provide a low power, accurate reference for the RTC.

General Purpose Register can be flag register, and it will save the value all the time when the VDD_RTC is not power off.

3.11.2 RTC Register List

Module Name	Base Address
RTC	0x01F00000

Register Name	Offset	Description
LOSC_CTRL_REG	0x0	Low Oscillator Control Register I
LOSC_AUTO_SWT_STA_REG	0x4	LOSC Auto Switch Status Register
INTOSC_CLK_PRESCAL_REG	0x8	Internal OSC Clock Prescalar Register
RTC YY_MM_DD_REG	0x10	RTC Year-Month-Day Register
RTC HH_MM_SS_REG	0x14	RTC Hour-Minute-Second Register
ALARM0_COUNTER_REG	0x20	Alarm 0 Counter Register
ALARM0_CUR_VLU_REG	0x24	Alarm 0 Counter Current Value Register
ALARM0_ENABLE_REG	0x28	Alarm 0 Enable Register
ALARM0_IRQ_EN	0x2C	Alarm 0 IRQ Enable Register
ALARM0_IRQ_STA_REG	0x30	Alarm 0 IRQ Status Register
ALARM1_WK_HH_MM_SS	0x40	Alarm 1 Week HMS Register
ALARM1_ENABLE_REG	0x44	Alarm 1 Enable Register
ALARM1_IRQ_EN	0x48	Alarm 1 IRQ Enable Register
ALARM1_IRQ_STA_REG	0x4C	Alarm 1 IRQ Status Register
ALARM_CONFIG_REG	0x50	Alarm Configuration Register
LOSC_OUT_GATING_REG	0x60	LOSC output gating register
GP_DATA_REG	0x100 + N*0x4	General Purpose Register (N=0~3)
GPL_HOLD_OUTPUT_REG	0x180	GPL Hold Output Register
VDD_RTC_REG	0x190	VDD RTC Regulate Register
IC_CHAR_REG	0x1F0	IC Characteristic Register

3.11.3 RTC Register Description

LOSC CONTROL (DEFAULT: 0X00004000)

Offset:0x0			Register Name: LOSC_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31:16	W	0x0	/
15	/	/	/
14	R/W	0x1	LOSC_AUTO_SWT_EN. LOSC auto switch enable. 0: Disable, 1: Enable.
13:10	/	/	/
9	R/W	0x0	ALM_DDHHMMSS_ACCE. ALARM DD-HH-MM-SS access. After writing the ALARM DD-HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished.
8	R/W	0x0	RTC_HHMMSS_ACCE. RTC HH-MM-SS access. After writing the RTC HH-MM-SS register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD register, the YY-MM-DD register will be refreshed for at most one second.
7	R/W	0x0	RTC_YYMMDD_ACCE. RTC YY-MM-DD access. After writing the RTC YY-MM-DD register, this bit is set and it will be cleared until the real writing operation is finished. After writing the RTC YY-MM-DD register, the YY-MM-DD

			register will be refreshed for at most one second.
6:4	/	/	/
3:2	R/W	0x0	<p>EXT_LOSC_GSM. External 32768Hz Crystal GSM.</p> <p>00 low 01 10 11 high</p>
1	/	/	/
0	R/W	0x0	<p>LOSC_SRC_SEL. LOSC Clock source Select. 'N' is the value of Internal OSC Clock Prescalar register.</p> <p>0: InternalOSC / N, 1: External 32.768KHz OSC.</p>

Note:

- 1) Any bit of [9:7] is set, the RTC HH-MM-SS, YY-MM-DD and ALARM DD-HH-MM-SS register can't be written.
- 2) Internal OSC is about 600 KHz ~700 KHz.

LOSC AUTO SWITCH STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x4			Register Name: LOSC_AUTO_SWT_STA_REG
Bit	Read/Writ e	Default/H ex	Description
31: 2	/	/	/
1	R/W	0x0	<p>LOSC_AUTO_SWT_PEND. LOSC auto switch pending.</p> <p>0: no effect; 1: auto switches pending.</p> <p>Set 1 to this bit will clear it.</p>
0	RO	0x0	<p>LOSC_SRC_SEL_STA. Checking LOSC Clock Source Status. 'N' is the value of Internal</p>

			OSC Clock Prescalar register. 0: InternalOSC / N; 1: External 32.768KHz OSC.
--	--	--	--

INTERNAL OSC CLOCK PRESCALAR REGISTER (DEFAULT: 0X00000014)

Offset:0x8			Register Name: INTOSC_CLK_PRESCAL_REG
Bit	Read/Writ e	Default/H ex	Description
31: 5	/	/	/
4:0	R/W	0x14	INTOSC_CLK_PRESCAL. Internal OSC Clock Prescalar value N. 00000: 1 00001: 2 00010: 3 11111: 32

RTC YY-MM-DD REGISTER (DEFAULT: 0X00000000)

Offset:0x10			Register Name: RTC YY_MM_DD_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 3	/	/	/
22	R/W	0x0	LEAP. Leap Year. 0: not, 1: Leap year. This bit cannot set by hardware. It should be set or clear by software.
21:1	R/W	x	YEAR.

6			Year. Range from 0~63.
15:1 2	/	/	/
11:8	R/W	x	MONTH. Month. Range from 1~12.
7:5	/	/	/
4:0	R/W	x	DAY. Day. Range from 1~31.

Note:

If the written value is not from 1 to 31 in Day Area, it turns into 31 automatically. Month Area and Year Area are similar to Day Area.

The number of days in different month may be different.

RTC HH-MM-SS REGISTER (DEFAULT: 0X00000000)

Offset:0x14			Register Name: RTC_HH_MM_SS_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	R/W	0x0	WK_NO. Week number. 000: Monday 001: Tuesday 010: Wednesday 011: Thursday 100: Friday 101: Saturday 110: Sunday

			111: /
28:2 1	/	/	/
20:1 6	R/W	x	HOUR. Range from 0~23
15:1 4	/	/	/
13:8	R/W	x	MINUTE. Range from 0~59
7:6	/	/	/
5:0	R/W	x	SECOND. Range from 0~59

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

ALARM 0 COUNTER REGISTER (DEFAULT: 0X00000000)

Offset:0x20			Register Name: ALARM0_COUNTER_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	ALARM0_COUNTER. Alarm 0 Counter is Based on Second.

Note: If the second is set to 0, it will be 1 second in fact.

ALARM 0 CURRENT VALUE REGISTER

Offset:0x24			Register Name: ALARM0_CUR_VLU_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	RO	x	ALARM0_CUR_VLU. Check Alarm 0 Counter Current Values.

Note: If the second is set to 0, it will be 1 second in fact.

ALARM 0 ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x28			Register Name: ALARM0_ENABLE_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	<p>ALM_0_EN</p> <p>Alarm 0 Enable.</p> <p>If this bit is set to “1”, the Alarm 0 Counter register’s valid bits will down count to zero, and the alarm pending bit will be set to “1”.</p> <p>0: disable, 1: enable.</p>

ALARM 0 IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x2C			Register Name: ALARM0_IRQ_EN
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	<p>ALARM0_IRQ_EN.</p> <p>Alarm 0 IRQ Enable.</p> <p>0: disable; 1: enable.</p>

ALARM 0 IRQ STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x30			Register Name: ALARM0_IRQ_STA_REG
Bit	Read/Writ e	Default/H ex	Description
31:	/	/	/

1			
0	R/W	0x0	<p>ALARM0_IRQ_PEND.</p> <p>Alarm 0 IRQ Pending bit.</p> <p>0: No effect;</p> <p>1: Pending, alarm 0 counter value is reached.</p> <p>If alarm 0 irq enable is set to 1, the pending bit will be sent to the interrupt controller.</p>

ALARM 1 WEEK HH-MM-SS REGISTER (DEFAULT: 0X00000000)

Offset:0x40			Register Name: ALARM1_WK_HH_MM-SS
Bit	Read/Writ e	Default/H ex	Description
31:2 1	/	/	/
20:1 6	R/W	x	<p>HOUR.</p> <p>Range from 0~23.</p>
15:1 4	/	/	/
13:8	R/W	x	<p>MINUTE.</p> <p>Range from 0~59.</p>
7:6	/	/	/. Range from 0~59.
5:0	R/W	x	SECOND. Range from 0~59.

Note: If the written value is not from 0 to 59 in Second Area, it turns into 59 automatically. Minute Area and Hour Area are similar to Second Area.

ALARM 1 ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x44			Register Name: ALARM1_EN_REG
Bit	Read/Writ e	Default/H ex	Description

31: 7	/	/	/
6	R/W	0x0	<p>WK6_ALM1_EN.</p> <p>Week 6 (Sunday) Alarm 1 Enable.</p> <p>0: Disable; 1: Enable.</p> <p>If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 6, the week 6 alarm irq pending bit will be set to “1”.</p>
5	R/W	0x0	<p>WK5_ALM1_EN.</p> <p>Week 5 (Saturday) Alarm 1 Enable.</p> <p>0: Disable; 1: Enable.</p> <p>If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 5, the week 5 alarm irq pending bit will be set to “1”.</p>
4	R/W	0x0	<p>WK4_ALM1_EN.</p> <p>Week 4 (Friday) Alarm 1 Enable.</p> <p>0: Disable, 1: Enable.</p> <p>If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 4, the week 4 alarm irq pending bit will be set to “1”.</p>
3	R/W	0x0	<p>WK3_ALM1_EN.</p> <p>Week 3 (Thursday) Alarm 1 Enable.</p> <p>0: Disable; 1: Enable.</p> <p>If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 3, the week 3 alarm irq pending bit will be set to “1”.</p>

2	R/W	0x0	<p>WK2_ALM1_EN.</p> <p>Week 2 (Wednesday) Alarm 1 Enable.</p> <p>0: Disable;</p> <p>1: Enable.</p> <p>If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 2, the week 2 alarm irq pending bit will be set to “1”.</p>
1	R/W	0x0	<p>WK1_ALM1_EN.</p> <p>Week 1 (Tuesday) Alarm 1 Enable.</p> <p>0: Disable;</p> <p>1: Enable.</p> <p>If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 1, the week 1 alarm irq pending bit will be set to “1”.</p>
0	R/W	0x0	<p>WKO_ALM1_EN.</p> <p>Week 0 (Monday) Alarm 1 Enable.</p> <p>0: Disable;</p> <p>1: Enable.</p> <p>If this bit is set to “1”, only when the Alarm 1 Week HH-MM-SS register valid bits is equal to RTC HH-MM-SS register and the register RTC HH-MM-SS bit [31:29] is 0, the week 0 alarm irq pending bit will be set to “1”.</p>

ALARM 1 IRQ ENABLE REGISTER (DEFAULT: 0X00000000)

Offset:0x48			Register Name: ALARM1_IRQ_EN
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	ALARM1_IRQ_EN.

			Alarm 1 IRQ Enable. 0: disable; 1: enable.
--	--	--	--

ALARM 1 IRQ STATUS REGISTER (DEFAULT: 0X00000000)

Offset:0x4C			Register Name: ALARM1_IRQ_STA_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	ALARM1_WEEK_IRQ_PEND. Alarm 1 Week (0/1/2/3/4/5/6) IRQ Pending. 0: No effect; 1: Pending, week counter value is reached. If alarm 1 week irq enable is set to 1, the pending bit will be sent to the interrupt controller.

ALARM CONFIG REGISTER (DEFAULT: 0X00000000)

Offset:0x50			Register Name: ALARM_CONFIG_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	ALARM_WAKEUP. Configuration of alarm wake up output. 0: disable alarm wake up output; 1: enable alarm wake up output.

LOSC OUTPUT GATING REGISTER (DEFAULT: 0X00000000)

Offset:0x60	Register Name: LOSC_OUT_GATING_REG
-------------	------------------------------------

Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	<p>LOSC_OUT_GATING.</p> <p>Configuration of LOSC output, and no LOSC output by default.</p> <p>0: Enable LOSC output gating; 1: Disable LOSC output gating.</p>

GENERAL PURPOSE REGISTER (DEFAULT: 0X00000000)

Offset:0x100+N *0x4 (N=0~3)			Register Name: GP_DATA_REGn
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	<p>GP_DATA.</p> <p>Data [31:0].</p>

Note: general purpose register 0/1/2/3 value can be stored if the VDD_RTC is larger than 1.0v.

GPL HOLD OUTPUT REGISTER (DEFAULT: 0X00000000)

Offset:0x180			Register Name: GPL_HOLD_OUTPUT_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 2	/	/	/
11	R/W	0x0	<p>GPL11_HOLD_OUTPUT.</p> <p>Hold the output of GPIO11 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on.</p> <p>0: Hold disable 1: Hold enable</p>
10	R/W	0x0	GPL10_HOLD_OUTPUT.

			Hold the output of GPIO10 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
9	R/W	0x0	GPL9_HOLD_OUTPUT. Hold the output of GPIO9 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
8	R/W	0x0	GPL8_HOLD_OUTPUT. Hold the output of GPIO8 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
7	R/W	0x0	GPL7_HOLD_OUTPUT. Hold the output of GPIO7 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
6	R/W	0x0	GPL6_HOLD_OUTPUT. Hold the output of GPIO6 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
5	R/W	0x0	GPL5_HOLD_OUTPUT. Hold the output of GPIO5 when system's power is changing. The output must be low level (0) or high level (1) or High-Z;

			any other outputs may not hold on. 0: Hold disable 1: Hold enable
4	R/W	0x0	GPL4_HOLD_OUTPUT. Hold the output of GPIOL4 when system's power is changing. The outputs must be low level (0) or high level (1) or High-Z; any other output may not hold on. 0: Hold disable 1: Hold enable
3	R/W	0x0	GPL3_HOLD_OUTPUT. Hold the output of GPIOL3 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
2	R/W	0x0	GPL2_HOLD_OUTPUT. Hold the output of GPIOL2 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
1	R/W	0x0	GPL1_HOLD_OUTPUT. Hold the output of GPIOL1 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable 1: Hold enable
0	R/W	0x0	GPL0_HOLD_OUTPUT. Hold the output of GPIOL0 when system's power is changing. The output must be low level (0) or high level (1) or High-Z; any other outputs may not hold on. 0: Hold disable

			1: Hold enable
--	--	--	----------------

VDD RTC REGULATION REGISTER (DEFAULT: 0X00000004)

Offset:0x190			Register Name: VDD_RTC_REG
Bit	Read/Writ e	Default/H ex	Description
31: 3	/	/	/
2:0	R/W	0x100	<p>VDD_RTC_REGU.</p> <p>These bits are useful for regulating the RTC_VIO from 0.7v to 1.4v, and the regulation step is 0.1v.</p> <p>000: 0.7v 001: 0.8v 010: 0.9v 011: 1.0v 100: 1.1v 101: 1.2v 110: 1.3v 111: 1.4v</p>

IC CHARACTERISTIC REGISTER (DEFAULT: 0X00000000)

Offset:0x1F0			Register Name: IC_CHARA_REG
Bit	Read/Writ e	Default/H ex	Description
31:0	R/W	0x0	/

3.12 R_Timer

3.12.1 Overview

The A23 supports two general timers: R_timer 0 and R_timer 1, which use the low speed OSC or OSC24M as clock source.

R_timer 0 and R_timer 1 share a programmable 3-bit pre-scale that provides the division of the clock source. They can work in auto-reload mode or no-reload mode. When the current value in *Current Value Register* is counting down to zero, the timer will generate interrupt if interrupt enable bit is set.

3.13 R_INTC

3.13.1 Overview

The interrupt controller has the following feature:

- Controls the nIRQ processor
- Support thirty-one individually maskable interrupt sources
- One external NMI interrupt source
- 4-Level priority controller
- Six external sources of edge-sensitive or level-sensitive
- Support fast forcing

It provides handling of up to thirty-two interrupt sources. The 4-level Priority Controller allows the user to define the priority for each interrupt source, thus permitting higher priority interrupts to be serviced even if a lower priority interrupt is being treated. The fast forcing feature redirects any internal or external source to provide a fast interrupt rather than a normal interrupt.

3.14 R_PWM

3.14.1 Overview

The output of the R_PWM is a toggling signal whose frequency and duty cycle can be modulated by its programmable registers. Each channel has a dedicated internal 16-bit up counter. If the counter reaches the value stored in the channel period register, it resets. At the beginning of a count period cycle, the PWMOUT is set to active state and count from 0.

The R_PWM divider divides the clock (24MHz) by 1~4096 according to the pre-scalar bits in the R_PWM control register.

In R_PWM cycle mode, the output will be a square waveform, the frequency is set to the period register. In R_PWM pulse mode, the output will be a positive pulse or a negative pulse.

3.15 R_Watchdog

3.15.1 Overview

The R_watchdog is used to resume the controller operation when it had been disturbed by malfunctions such as noise and system errors. It features a down counter that allows a watchdog period of up to 16 seconds. It can generate a general reset or interrupt request. The watchdog generates the reset signal to reset CPUS or the whole system.

3.16 System Control

3.16.1 Overview

Area	Address	Size(Bytes)
A1	0x00000000--0x00003FFF	16K
A2	0x00044000--0x00053FFF	64K
CPU0 I-Cache		32K
CPU0 D-Cache		32K
CPU1 I-Cache		32K
CPU1 D-Cache		32K
CPU L2 Cache		256K
Total		464K

3.16.2 System Control Register List

Module Name	Base Address
SRAM	0x01C00000

Register Name	Offset	Description
SRAM_CTRL_REG0	0x0	SRAM Control Register 0
SRAM_CTRL_REG1	0x4	SRAM Control Register 1
/	0x8	/
/	0x14	/
/	0x18	/
/	0x1C	/
/	0x20	/
/	0x24	/
/	0x48	/
/	0x90	/
/	0x94	/

3.16.3 System Control Register Description

SRAM CONTROL REGISTER 0 (DEFAULT: 0X7FFFFFFF)

Offset:0x0			Register Name: SRAM_CTRL_REG0
Bit	Read/Writ e	Default/H ex	Description
31	/	/	/
30:0	R/W	0x7fffffff	SRAM_C1_MAP. SRAM Area C1 50K Bytes Configuration by AHB. 0: map to CPU/DMA 1: map to VE

SRAM CONTROL REGISTER 1 (DEFAULT: 0X00001300)

Offset:0x4			Register Name: SRAM_CTRL_REG1
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0x0	BIST_DMA_CTRL_SEL. Bist and DMA control select. 0: DMA, 1: Bist.
30:0	/	/	/.

3.17 Audio CODEC

3.17.1 Overview

The embedded audio codec is a high-quality stereo audio codec with headphone amplifier and is designed for mobile computing and communications. It provides a stereo DAC for playback and stereo ADC for recording.

It features:

- Two audio digital to analog(DAC) channels
 - Stereo capless headphone drivers
 - Up to 100dB SNR
 - Support DAC sample rates from 8KHz to 192KHz
- Support analog/ digital volume control
- Differential earpiece driver
- Two low-noise analog microphone bias outputs
- Analog low-power loop from line-in /microphone/phonein to headphone/earpiece outputs
- Accessory button press detection
- Support four audio inputs
 - Two differential microphone inputs
 - Stereo line-in input
 - Differential Phonein input
- Two audio analog-to-digital(ADC) channels
 - 94dB SNR
 - Support ADC sample rates from 8KHz to 48KHz

3.17.2 Signal Description

Signal Name	Type	Description
HBIAS	O	Headset microphone bias supply
MBIAS	O	Main analog microphone bias supply
PHONEOUTP	O	Phone positive output
PHONEOUTN	O	Phone negative output
MICIN1P	I	First microphone positive input
MICIN1N	I	First microphone negative input
MICIN2P	I	Second microphone positive input
MICIN2N	I	Second microphone negative input
PHONEP	I	Phone positive input
PHONEN	I	Phone negative input
LINEINL	I	Line in left input
LINEINR	I	Line in right input
HPCOMFB	I	Headphone common reference feedback
HPCOM	O	Headphone common reference
HPOUTL	O	Headphone Left output
HPOUTR	O	Headphone Right output

Power Description:

VRA1	O	Reference
VRA2	O	Reference
VRP	O	Reference
AVCC	I	Analog Power
HPVCCIN	I	Headphone Amplifier Power Supply

HPVCCBP	O	Headphone Amplifier Power Bypass
AGND	GND	Analog Ground

CONFIDENTIAL

3.17.3 Function Description

STEREO ADC

The stereo ADC is used for recording stereo sound. The sample rate of the stereo ADC is independent of DAC sample rate. In order to save power, the left and right ADC can be powered down separately by setting register ADC_AP_EN Bit[7:6].

The volume control of the stereo ADC is set via register HP_VOLC Bit[5:0].

STEREO DAC

The stereo DAC can be configured to different sample rate by setting the register AC_DAC_FIFOC Bit[31:29], In order to save power, the left and right DAC can be powered down separately by setting register DAC_PA_SRC Bit[7:6].

MIXER

The Codec supports two mixers for all function requirements:

- Headphone mixer for 2 channels
- ADC record mixer

HEADPHONE MIXER

The headphone mixer is used to drive stereo output.

The following signals can be mixed into the headphone mixer:

- LINEINL/R
- PHONEP/N
- MIC1P/N, MIC2P/N
- Stereo DAC output

ADC RECORD MIXER

The ADC record mixer is used to mix analog signals as input to the Stereo ADC for recording.

- LINEINL/R
- PHONEP/N
- MIC1P/N, MIC2P/N
- Stereo DAC output

ANALOG AUDIO INPUT PATH

The Codec supports four analog audio input paths:

- LINEINL/R
- MIC1
- MIC2
- PHONEP/N

LINE INPUT

LINEINL and LINEINR provide 2-channel stereo single-ended input that can be mixed into the Headphone mixer and ADC record mixer. The inputs are high impedance and low capacitance, thus ideally suited to receiving line level signals from external hi-fi or audio equipment or audio module FM.

PHONE INPUT

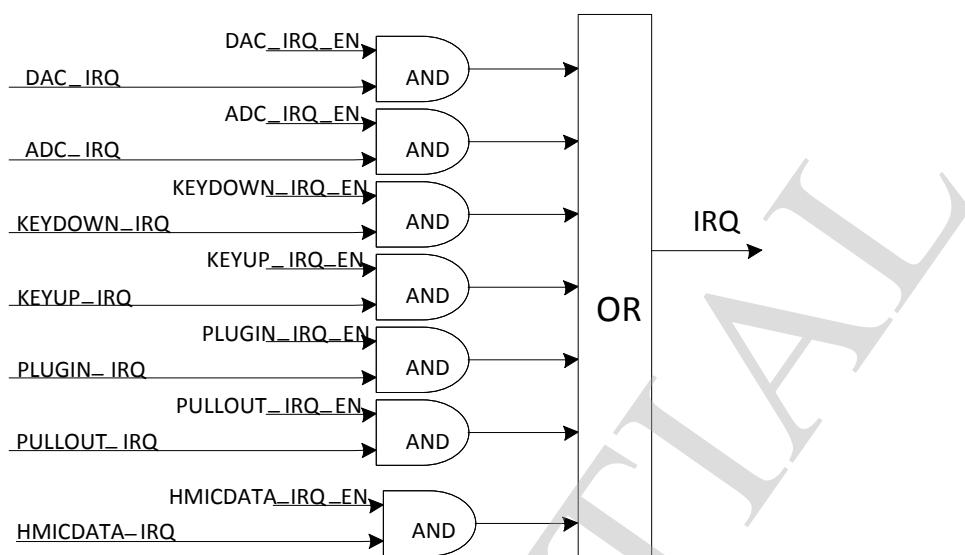
PHONEP/N provides one-channel MONO differential or stereo single-ended input that can be mixed into the ADC record mixer or Headphone mixer.

MICROPHONE INPUT

MICIN1P/N and MICIN2P/N provide differential input that can be mixed into the ADC record mixer, or Headphone Mixer. MICIN is high impedance, low capacitance input suitable for connection to a wide range of differential microphones of different dynamics and sensitivity. There are two microphone pre-amplifiers which can be configured 2 differential microphone inputs. MICIN1P/N are input to the first pre-amplifier, MICIN2P/N are selected to input the 2nd pre-amplifier.

Each microphone preamplifier has a separate enable bit, MICAMP1EN, MICAMP2EN. The gain for each preamp can be set independently using MIC1BOOST, MIC2BOOST.

INTERRUPT



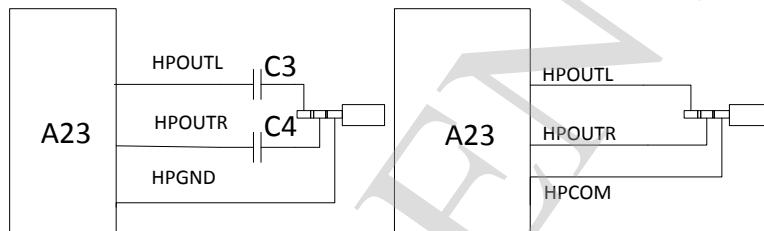
3.17.4 Analog Audio Output Data Path

HEADPHONE OUTPUT

HPOUTL/R provides two-channel single-ended output. The HPOUTL/R source is set in Reg. Sources are shown below:

- DAC
- Headphone mixer

Analogue outputs HPOUTL and HPOUTR can drive a 16R or 32R headphone load, either through DC blocking capacitors, or DC coupled without any capacitor.



Recommended Headphone Output Configuration

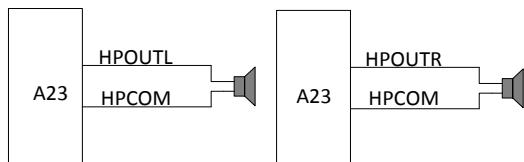
When DC blocking capacitors are used, then their capacitance and the load resistance together determine the lower cut-off frequency, f_c . Increasing the capacitance lowers f_c , improving the bass response. Smaller capacitance values will diminish the bass response. Assuming a 16R load and $C_3, C_4 = 220\mu F$:

$$f_c = 1/(2 * 3.14 * R_L * C) = 1/(2 * 3.14 * 16 * 220\mu F) = 45Hz$$

In the DC coupled configuration, the headphone “ground” is connected to the HPCOM pin. HPCOM is enabled by setting `HPCOMS_FC= 11`. As the HPCOM pin produces a DC voltage of 1.5V, there is no DC offset between HPOUTL/HPOUTR and HPCOM, and therefore no DC blocking capacitors are required. This saves space and material cost in portable applications. It is also connect the line input of another device. It is not only recommended to connect the DC coupled headphone outputs to headphones, but also to the line input of another device, because the HPCOM can dismiss these two conditions. If it is connect the headphone, HPCOM output 1/2AVCC; If it is connect the another device which is grounded, the HPCOM output 0 volts

EARPIECE OUTPUT

The HPCOM can drive a 16R or 32R headphone DC reference or a line output which inverting the HPOUTL/R. So HPCOM can be selected to differential signal with HPOUTL or HPOUTR for e.g. an earpiece drive.



Earpiece Application Drawing

3.17.5 Microphone BIAS

The MICBIAS output provides a low noise reference voltage suitable for biasing electrets type microphones and the associated external resistor biasing network.

A MICBIAS Current Detect function is provided for external accessory detection. This is provided in order to detect the insertion/removal of a microphone or the button press.

When MICBIAS current detect is enabled, ADC will send out 128Hz 5bit data. Digital trigger an interrupt event when the data is changed.

Digital Circuit generate five IRQ signals that can be disable by register, the Data from ADC can be read from register.

3.17.6 Headphone Amplifier

The Codec has a stereo headphone output available on HPOUTL and HPOUTR. The output is designed specifically for driving 16R or 32R headphones with maximum efficiency and low power consumption. The headphone output includes a high quality volume level adjustment and mute function.

HPOUTL and HPOUTR volumes can be adjusted under software control using the HPVOL[5:0] of the headphone output control registers. The adjustment is logarithmic with a 64dB range in 1dB steps from 0dB to -62dB.

The headphone outputs can be muted by writing codes 00000 to HPVOL[5:0] bits.

A zero cross detect circuit is provided at the input to the headphones under the control of the ZCEN bits of the headphone output control register. Using these controls the volume control values are only updated when the input signal to the gain stage is close to the analogue ground level. This minimizes and audible clicks and zipper noise as the gain values are changed or the device muted.

CONFIDENTIAL

3.17.7 Audio Codec Register List

Module Name	Base Address
AC	0x01C22C00

Register Name	Offset	Description
AC_DAC_DPC	0x00	DAC Digital Part Control Register
AC_DAC_FIFOC	0x04	DAC FIFO Control Register
AC_DAC_FIFOS	0x08	DAC FIFO Status Register
AC_DAC_TXDATA	0x0c	DAC TX Data Register
AC_ADC_FIFOC	0x10	ADC FIFO Control Register
AC_ADC_FIFOS	0x14	ADC FIFO Status Register
AC_ADC_RXDATA	0x18	ADC RX Data Register
AC_DAC_CNT	0x1c	DAC TX FIFO Counter Register
AC_ADC_CNT	0x20	ADC RX FIFO Counter Register
AC_ANALOG_CNT	/	Use R_PRCM Register (0x01c0) in CPUS for read/write

3.17.8 Audio Codec Register Description

DAC DIGITAL PART CONTROL REGISTER

Offset: 0x00			Register Name: AC_DAC_DPC
Bit	Read/Write	Default	Description
31	R/W	0x0	EN_DA. DAC Digital Part Enable 0: Disable 1: Enable
30:29	/	/	/
28:25	R/W	0x0	MODQU. Internal DAC Quantization Levels Levels=[7*(21+MODQU[3:0])]/128 Default levels=7*21/128=1.15
24	R/W	0x0	DWA. DWA Function Disable 0: Enable 1: Disable
23:19	/	/	/
18	R/W	0x0	HPF_EN. High Pass Filter Enable 0: Disable 1: Enable
17:12	R/W	0x0	DVOL. Digital volume control: dvc, ATT=DVC[5:0]*(-1.16dB) 64 steps, -1.16dB/step

11:0	/	/	/
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DAC FIFO CONTROL REGISTER

Offset: 0x04			Register Name: AC_DAC_FIFOC
Bit	Read/Wri te	Defau lt	Description
31:29	R/W	0x0	<p>DAC_FS.</p> <p>Sample Rate of DAC</p> <p>000: 48KHz</p> <p>010: 24KHz</p> <p>100: 12KHz</p> <p>110: 192KHz</p> <p>001: 32KHz</p> <p>011: 16KHz</p> <p>101: 8KHz</p> <p>111: 96KHz</p> <p>44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit</p>
28	R/W	0	<p>FIR_VER</p> <p>FIR Version</p> <p>0: 64-Tap FIR; 1: 32-Tap FIR</p>
27	/	/	/
26	R/W	0x0	<p>SEND_LASAT.</p> <p>Audio sample select when TX FIFO under run</p> <p>0: Sending zero</p> <p>1: Sending last audio sample</p>
25:24	R/W	0x0	<p>FIFO_MODE.</p> <p>For 24-bits transmitted audio sample:</p> <p>00/10: FIFO_I[23:0] = {TXDATA[31:8]}</p>

5	R/W	0x0	<p>TX_SAMPLE_BITS.</p> <p>Transmitting Audio Sample Resolution</p> <p>0: 16 bits</p> <p>1: 24 bits</p>
4	R/W	0x0	<p>DAC_DRQ_EN.</p> <p>DAC FIFO Empty DRQ Enable</p> <p>0: Disable</p> <p>1: Enable</p>
3	R/W	0x0	<p>DAC_IRQ_EN.</p> <p>DAC FIFO Empty IRQ Enable</p> <p>0: Disable</p> <p>1: Enable</p>
2	R/W	0x0	<p>FIFO_UNDERRUN_IRQ_EN.</p> <p>DAC FIFO Under Run IRQ Enable</p> <p>0: Disable</p> <p>1: Enable</p>
1	R/W	0x0	<p>FIFO_OVERRUN_IRQ_EN.</p> <p>DAC FIFO Over Run IRQ Enable</p> <p>0: Disable</p> <p>1: Enable</p>
0	R/W	0x0	<p>FIFO_FLUSH.</p> <p>DAC FIFO Flush</p> <p>Write '1' to flush TX FIFO, self clear to '0'</p>

DAC FIFO STATUS REGISTER

Offset: 0x08			Register Name: AC_DAC_FIFOS
Bit	Read/Wri te	Defau lt	Description
31:24	/	/	/

23	R	0x1	<p>TX_EMPTY.</p> <p>TX FIFO Empty</p> <p>0: No room for new sample in TX FIFO</p> <p>1: More than one room for new sample in TX FIFO (>= 1 word)</p>
22:8	R	0x80	<p>TXE_CNT.</p> <p>TX FIFO Empty Space Word Counter</p>
7:4	/	/	/
3	R/W	0x1	<p>TXE_INT.</p> <p>TX FIFO Empty Pending Interrupt</p> <p>0: No Pending IRQ</p> <p>1: FIFO Empty Pending Interrupt</p> <p>Write '1' to clear this interrupt or automatic clear if interrupt condition fails.</p>
2	R/W	0x0	<p>TXU_INT.</p> <p>TX FIFO Under run Pending Interrupt</p> <p>0: No Pending Interrupt</p> <p>1: FIFO Under run Pending Interrupt</p> <p>Write '1' to clear this interrupt</p>
1	R/W	0x0	<p>TXO_INT.</p> <p>TX FIFO Overrun Pending Interrupt</p> <p>0: No Pending Interrupt</p> <p>1: FIFO Overrun Pending Interrupt</p> <p>Write '1' to clear this interrupt</p>
0	/	/	/

DAC TX DATA REGISTER

Offset: 0x0C			Register Name: AC_DAC_TXDATA
Bit	Read/Write	Default	Description
31:0	W	0x0	TX_DATA.

			Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.
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ADC FIFO CONTROL REGISTER

Offset: 0x10			Register Name: AC_ADC_FIFOC
Bit	Read/Write	Default	Description
31:29	R/W	0x0	ADFS. Sample Rate of ADC 000: 48KHz 010: 24KHz 100: 12KHz 110: Reserved 001: 32KHz 011: 16KHz 101: 8KHz 111: Reserved 44.1KHz/22.05KHz/11.025KHz can be supported by Audio PLL Configure Bit
28	R/W	0x0	EN_AD. ADC Digital Part Enable, en_ad 0: Disable 1: Enable
27	R/W	0x0	DigMic_EN Digital Microphone Enable, en_digmic 0: Analog ADC Mode 1: Digital Microphone Mode
26:25	/	/	/
24	R/W	0x0	RX_FIFO_MODE.

			<p>RX FIFO Output Mode (Mode 0, 1)</p> <p>0: Expanding '0' at LSB of TX FIFO register</p> <p>1: Expanding received sample sign bit at MSB of TX FIFO register</p> <p>For 24-bits received audio sample:</p> <p>Mode 0: RXDATA[31:0] = {FIFO_O[23:0], 8'h0}</p> <p>Mode 1: Reserved</p> <p>For 16-bits received audio sample:</p> <p>Mode 0: RXDATA[31:0] = {FIFO_O[23:8], 16'h0}</p> <p>Mode 1: RXDATA[31:0] = {16{FIFO_O[23]}, FIFO_O[23:8]}</p>
23:19	/	/	/
18:17	R/W	0x0	<p>ADCFDT.</p> <p>ADC FIFO Delay Time For writing Data after en_ad</p> <p>00:5ms</p> <p>01:10ms</p> <p>10:20ms</p> <p>11:30ms</p>
16	R/W	0x0	<p>ADCDFEN.</p> <p>ADC FIFO Delay Function For writing Data after en_ad</p> <p>0: Disable</p> <p>1: Enable</p>
15:13	/	/	/
12:8	R/W	0xF	<p>RX_FIFO_TRG_LEVEL.</p> <p>RX FIFO Trigger Level (RXTL[4:0])</p> <p>Interrupt and DMA request trigger level for TX FIFO normal condition</p> <p>IRQ/DRQ Generated when WLEVEL > RXTL[4:0]</p> <p>Note:</p> <p>WLEVEL represents the number of valid samples in the RX FIFO</p>

7	R/W	0x0	<p>ADC_MONO_EN.</p> <p>ADC Mono Enable.</p> <p>0: Stereo, 16 levels FIFO</p> <p>1: mono, 32 levels FIFO</p> <p>When set to '1', Only left channel samples are recorded</p>
6	R/W	0x0	<p>RX_SAMPLE_BITS.</p> <p>Receiving Audio Sample Resolution</p> <p>0: 16 bits</p> <p>1: 24 bits</p>
5	/	/	/
4	R/W	0x0	<p>ADC_DRQ_EN.</p> <p>ADC FIFO Data Available DRQ Enable.</p> <p>0: Disable</p> <p>1: Enable</p>
3	R/W	0x0	<p>ADC_IRQ_EN.</p> <p>ADC FIFO Data Available IRQ Enable.</p> <p>0: Disable</p> <p>1: Enable</p>
2	/	/	/
1	R/W	0x0	<p>ADC_OVERRUN_IRQ_EN.</p> <p>ADC FIFO Over Run IRQ Enable</p> <p>0: Disable</p> <p>1: Enable</p>
0	R/W	0x0	<p>ADC_FIFO_FLUSH.</p> <p>ADC FIFO Flush.</p> <p>Write '1' to flush TX FIFO, self clear to '0'.</p>

ADC FIFO STATUS REGISTER

Offset: 0x14			Register Name: AC_ADC_FIFOS
Bit	Read/Wri te	Defau lt	Description
31:24	/	/	/
23	R	0x0	RXA. RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
22:14	/	/	/
13:8	R	0x0	RXA_CNT. RX FIFO Available Sample Word Counter
7:4	/	/	/
3	R/W	0x0	RXA_INT. RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ Write '1' to clear this interrupt or automatic clear if interrupt condition fails.
2	/	/	/
1	R/W	0x0	RXO_INT. RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ Write '1' to clear this interrupt
0	/	/	/

ADC RX DATA REGISTER

Offset: 0x18	Register Name: AC_ADC_RXDATA
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Bit	Read/Write	Default	Description
31:0	R	0x0	<p>RX_DATA.</p> <p>RX Sample</p> <p>Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.</p>

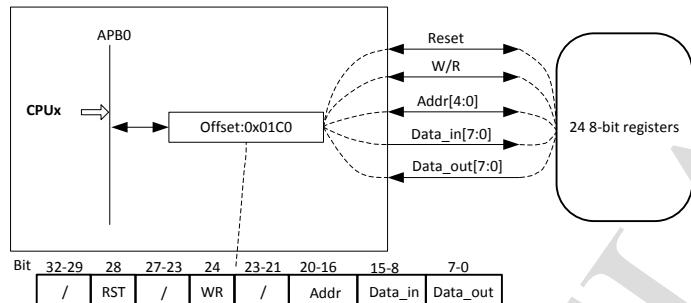
DAC TX COUNTER REGISTER

Offset: 0x1c			Register Name: AC_DAC_CNT
Bit	Read/Write	Default	Description
31:0	R/W	0x0	<p>TX_CNT.</p> <p>TX Sample Counter</p> <p>The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.</p> <p>Note: It is used for Audio/ Video Synchronization</p>

ADC RX COUNTER REGISTER

Offset: 0x20			Register Name: AC_ADC_CNT
Bit	Read/Write	Default	Description
31:0	R/W	0x0	<p>RX_CNT.</p> <p>RX Sample Counter</p> <p>The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.</p> <p>Note: It is used for Audio/ Video Synchronization</p>

Note that the following 25 8-bit registers can be controlled by configuring 0x01F015C0 register through the APBO BUS, as shown below. (Reset: register reset; ADDR[4:0]: offset of corresponding 8-bit registers; W/R: W/R enable; WDAT[7:0]: write; RDAT[7:0]: read)



HEADPHONE VOLUME CONTROL REGISTER

Offset:0x00			Register Name: HP_VOLC
Bit	R/W	Default	Description
7	R/W	0x0	PA clock gating control; when system VDD is off and Audio analog channel is working, this bit must be set to 1, because the PA clock come from system VDD domain. When this bit is 1, the Zero cross over function will be disabled automatically. 0: not gating; 1: gating
6	R/W	0x0	/
5:0	R/W	0x0	HPVOL Headphone Volume Control, (HPVOL): Total 64 level, from 0dB to -62dB, 1dB/step, mute when 000000

LEFT OUTPUT MIXER SOURCE CONTROL REGISTER

Offset:0x01			Register Name: LOMIXSC
Bit	R/W	Default	Description
7	R/W	0x0	/
6:0	R/W	0x0	LMIXMUTE

		Left Output Mixer Mute Control 0-Mute, 1-Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEN Bit 2: LINEINL Bit 1: Left channel DAC Bit 0: Right channel DAC
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RIGHT OUTPUT MIXER SOURCE CONTROL REGISTER

Offset:0x02			Register Name: ROMIXSC
Bit	R/W	Default	Description
7	R/W	0x0	/
6:0	R/W	0x0	RMIXMUTE Right Output Mixer Mute Control 0-Mute, 1-Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEP Bit 2: LINEINR Bit 1: Right channel DAC Bit 0: Left channel DAC

DAC ANALOG ENABLE AND PA SOURCE CONTROL REGISTER

Offset:0x03			Register Name: DAC_PA_SRC
Bit	R/W	Default	Description

7	R/W	0x0	DACAREN Internal Analog Right channel DAC Enable 0:Disable; 1:Enable
6	R/W	0x0	DACALEN Internal Analog Left channel DAC Enable 0:Disable; 1:Enable
5	R/W	0x0	RMIXEN Right Analog Output Mixer Enable 0:Disable; 1:Enable
4	R/W	0x0	LMIXEN Left Analog Output Mixer Enable 0:Disable; 1:Enable
3	R/W	0x0	RHPPAMUTE All input source to Right Headphone PA mute, including Right Output mixer and Internal Right channel DAC: 0:Mute, 1: Not mute
2	R/W	0x0	LHPPAMUTE All input source to Left Headphone PA mute, including Left Output mixer and Internal Left channel DAC: 0:Mute, 1: Not mute
1	R/W	0x0	RHPIS Right Headphone Power Amplifier (PA) Input Source Select 0: Right channel DAC 1: Right Analog Mixer
0	R/W	0x0	LHPIS Left Headphone Power Amplifier (PA) Input Source Select 0: Left channel DAC 1: Left Analog Mixer

PHONEIN STEREO GAIN CONTROL REGISTER

Offset:0x04			Register Name: PHONEIN_GCTRL
Bit	R/W	Default	Description
7	R/W	0x0	/
6:4	R/W	0x3	PHONEPG, (volppn) PHONEP to Right output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	R/W	0x0	/
2:0	R/W	0x3	PHONENG, (volpnn) PHONEN to Left output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

LINEIN AND PHONE_P-N GAIN CONTROL REGISTER

Offset:0x05			Register Name: LINEIN_GCTRL
Bit	R/W	Default	Description
7	R/W	0x0	/
6:4	R/W	0x3	LINEING, (volln) LINEINL/R to L/R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	R/W	0x0	/
2:0	R/W	0x3	PHONEG, (volpg) PHONE(P-N) gain stage to L/R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

MIC1 AND MIC2 GAIN CONTROL REGISTER

Offset:0x06			Register Name: MICIN_GCTRL
Bit	R/W	Default	Description
7	R/W	0x0	/

6:4	R/W	0x3	MIC1G, (volm1) MIC1 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
3	R/W	0x0	/
2:0	R/W	0x3	MIC2G, (volm2) MIC2 BOOST stage to L or R output mixer Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB

PA ENABLE AND HP CONTROL REGISTER

Offset:0x07			Register Name: PAEN_HP_CTRL
Bit	R/W	Default	Description
7	R/W	0x0	HPPAEN Right & Left Headphone Power Amplifier Enable 0-disable 1-enable
6:5	R/W	0x0	HPCOM_FC HPCOM function control 00: HPCOM off & output is floating 01: HPL inverting output 10: HPR inverting output 11: Direct driver for HPL & HPR
4	R/W	0x1	COMPTEEN HPCOM output protection enable when it is set as Direct driver for HPL/R 0: protection disable 1: protection enable
3:2	R/W	0x1	PA_ANTI_POP_CTRL, (slopelengthsel) PA Anti-pop time Control

			00:131ms; 01: 262ms; 10: 393ms; 11:524ms
1	R/W	0x0	LTRNMUTE, (hprisinvhpl) Left HPOUT Negative To Right HPOUT Mute 0: Mute, 1: Not mute
0	R/W	0x0	RTLNMMUTE, (hplisinvhpr) Right HPOUT Negative To Left HPOUT Mute 0: Mute, 1: Not mute

PHONEOUT CONTROL REGISTER

Offset:0x08			Register Name: PHONEOUT_CTRL
Bit	R/W	Default	Description
7:5	R/W	0x3	PHONEOUTG Phone-out Gain Control From -4.5dB to 6dB, 1.5dB/step, default is 0dB
4	R/W	0x0	PHONEOUT enable 0: Enable, 1: Disable
3	R/W	0x0	PHONEOUTS3 MIC1 Boost stage to Phone out mute 0: Mute, 1: Not mute
2	R/W	0x0	PHONEOUTS2 MIC2 Boost stage to Phone out mute 0: Mute, 1: Not mute
1	R/W	0x0	PHONEOUTS1 Right Output mixer to Phone out mute 0: Mute, 1: Not mute
0	R/W	0x0	PHONEOUTS0 Left Output mixer to Phone out mute 0: Mute, 1: Not mute

PHONEP-N GAIN CONTROL REGISTER

Offset:0x09			Register Name: PHONEP-N_GAIN_CTR
Bit	R/W	Default	Description
7:3	R/W	0x0	/
2:0	R/W	0x4	PHONEPREG PHONEP-PHONEN pre-amplifier gain control -12dB to 9dB, 3dB/step, default is 0dB

MIC2 BOOST ENABLE CONTROL REGISTER

Offset:0x0A			Register Name: MIC2G_LINEEN_CTRL
Bit	R/W	Default	Description
7	R/W	0x0	MIC2AMPEN MIC2 Boost AMP Enable 0-Disable; 1-Enable
6:4	R/W	0x4	MIC2BOOST MIC2 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB
3:0	R/W	0x0	/

MIC1 BOOST AND MICBIAS CONTROL REGISTER

Offset:0x0B			Register Name: MIC1G_MICBIAS_CTRL
Bit	R/W	Default	Description
7	R/W	0x0	HMICBIASEN Headset Microphone Bias enable 0: disable, 1: enable

6	R/W	0x0	MMICBIASEN Master Microphone Bias enable 0: disable, 1: enable
5	R/W	0x0	HMICBIAS MODE Headset MIC Bias Mode select 0:HMICBIAS auto suspend when HMIC is absent 1:HMICBIAS always on when MMICBIASEN IS 1
4	R/W	0x1	/
3	R/W	0x0	MIC1AMPEN MIC1 Boost AMP Enable 0-Disable; 1-Enable
2:0	R/W	0x4	MIC1BOOST MIC1 Boost AMP Gain Control 0dB when 000, 24dB to 42dB when 001 to 111, 3dB/step, default is 33dB

LEFT ADC MIXER SOURCE CONTROL REGISTER

Offset:0x0C			Register Name: LADCMIXSC
Bit	R/W	Default	Description
7	R/W	0x0	/
6:0	R/W	0x0	LADCMIXMUTE Left ADC Mixer Mute Control: 0-Mute, 1-Not mute Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEN Bit 2: LINEINL

			Bit 1: Left output mixer Bit 0: Right output mixer
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RIGHT ADC MIXER SOURCE CONTROL REGISTER

Offset:0x0D			Register Name: RADCMIXSC
Bit	R/W	Default	Description
7	R/W	0x0	/
6:0	R/W	0x0	RADCMIXMUTE Right ADC Mixer Mute Control: 0: Mute; 1:On Bit 6: MIC1 Boost stage Bit 5: MIC2 Boost stage Bit 4: PHONEP-PHONEN Bit 3: PHONEP Bit 2: LINEINR Bit 1: Right output mixer Bit 0: Left output mixer

RESERVED REGISTER

Offset:0x0E			Register Name: Reserved Register
Bit	R/W	Default	Description
7:0	R/W	0x0	PA_ANTI_POP_CTRL, (slopeLengthSel) PA Anti-pop time Control 000: 131ms; 001: 262ms; 010: 393ms; 011: 524ms; 100: 655ms; 101: 786ms; 110: 786ms; 111: 1048ms;

ADC ANALOG PART ENABLE REGISTER

Offset:0x0F	Register Name: ADC_AP_EN
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Bit	R/W	Default	Description
7	R/W	0x0	ADCREN ADC Right Channel Enable 0-Disable; 1-Enable
6	R/W	0x0	ADCLEN ADC Left Channel Enable 0-Disable; 1-Enable
5:3	R/W	0x0	/
2:0	R/W	0x3	ADCG ADC Input Gain Control From -4.5dB to 6dB, 1.5dB/step default is 0dB

ADDA ANALOG PERFORMANCE TURNING 2 REGISTER

Offset:0x12			Register Name: ADDA_APT2
Bit	R/W	Default	Description
7	R/W	0x0	function enable for master volume change at zero cross over 0: disable; 1: enable
6	R/W	0x1	Timeout control for master volume change at zero cross over 0: 32ms; 1: 64ms
5:4	R/W	0x0	PTDBS HPCOM protect de-bounce time setting 00: 2-3ms; 01: 4-6ms; 10: 8-12ms; 11: 16-24ms
3	R/W	0x0	PA_SLOPE_SELECT PA slope select cosine or ramp 0: select cosine 1: select ramp
2:0	R/W	0x2	USB_BIAS_CUR. USB bias current tuning

			From 23uA to 30uA, Default is 25uA
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BIAS CALIBRATION DATA REGISTER

Offset:0x17			Register Name: BIASCALI
Bit	R/W	Default	Description
7:0	R	0x20	BIASCALI Bias Calibration Data, 6bit

BIAS REGISTER SETTING DATA REGISTER

Offset:0x18			Register Name: BIASVERIFY
Bit	R/W	Default	Description
7:0	R/W	0x20	BIAVERIFY Bias Register Setting Data, 6bit

3.18 LRADC

3.18.1 Overview

The A23 supports a 6-bit LRADC for key application.

It features:

- Supports APB 32-bits bus width
- Support interrupt
- Support Hold Key and General Key
- Support single key and continue key mode
- Support 6-bit resolution
- Support voltage input range between 0 to 2V
- Support sample rate up to 250Hz

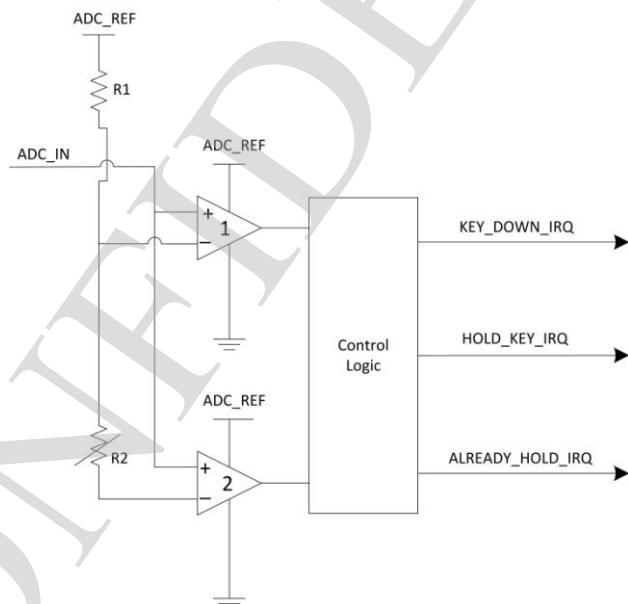
3.18.2 Principles of Operation

BLOCK DIAGRAM

The LRADC converted data can be accessed by interrupt and polling method. If software can't access the last converted data instantly, the new converted data would update the old one at new sampling data.

HOLD KEY AND GENERAL KEY FUNCTION

When ADC_IN Signal change from ADC_REF to 2/3 ADC_REF (Level A), the comparator24 send first interrupt to control logic; When ADC_IN Signal change from 2/3 ADC_REF to certain level (Program can set), the comparator25 give second interrupt. If the control Logic get the first interrupt, In a certain time range (program can set), doesn't get second interrupt, it will send hold key interrupt to the host; If the control Logic get the first interrupt, In a certain time range (program can set), get second interrupt, it will send key down interrupt to the host; If the control logic only get the second interrupt, doesn't get the first interrupt, it will send already hold interrupt to the host.



3.18.3 LRADC Register List

Module Name	Base Address
LRADC	0x01C22800

Register Name	Offset	Description
LRADC_CTRL	0x00	LRADC Control Register
LRADC_INTC	0x04	LRADC Interrupt Control Register
LRADC_INTS	0x08	LRADC Interrupt Status Register
LRADC_DATA	0x0c	LRADC Data Register

3.18.4 LRADC Register Description

LRADC CONTROL REGISTER

Offset: 0x00w			Register Name: LRADC_CTRL
Bit	Read/Writ e	Default/H ex	Description
31: 24	R/W	0x1	FIRST_CONCERT_DLY. ADC First Convert Delay setting, ADC conversion is delayed by n samples
23:22	R/W	0x0	Reserved to 0
21:20	/	/	/
19:16	R/W	0x0	CONTINUE_TIME_SELECT. Continue Mode time select, one of 8*(N+1) sample as a valuable sample data
15:14	/	/	/
13:12	R/W	0x0	KEY_MODE_SELECT. Key Mode Select: 00: Normal Mode 01: Single Mode 10: Continue Mode
11:8	R/W	0x1	LEVELA_B_CNT. Level A to Level B time threshold select, judge ADC convert value in level A to level B in n+1 samples
7	/	/	/
6	R/W	0x1	LRADC_HOLD_EN. LRADC Sample hold Enable 0: Disable

			1: Enable
5: 4	R/W	0x2	<p>LEVELB_VOL.</p> <p>Level B Corresponding Data Value setting (the real voltage value)</p> <p>00: 0x3C (~1.9v)</p> <p>01: 0x39 (~1.8v)</p> <p>10: 0x36 (~1.7v)</p> <p>11: 0x33 (~1.6v)</p>
3: 2	R/W	0x2	<p>LRADC_SAMPLE_RATE.</p> <p>LRADC Sample Rate</p> <p>00: 250 Hz</p> <p>01: 125 Hz</p> <p>10: 62.5 Hz</p> <p>11: 32.25 Hz</p>
1	/	/	/
0	R/W	0x0	<p>LRADC_EN.</p> <p>LRADC enable</p> <p>0: Disable</p> <p>1: Enable</p>

LRADC INTERRUPT CONTROL REGISTER

Offset: 0x04			Register Name: LRADC_INTC
Bit	Read/Writ e	Default/H ex	Description
31: 5	/	/	/
4	R/W	0x0	ADC0_KEYUP_IRQ_EN. ADC 0 Key Up IRQ Enable 0: Disable 1: Enable
3	R/W	0x0	ADC0_ALRDY_HOLD_IRQ_EN. ADC 0 Already Hold IRQ Enable 0: Disable 1: Enable
2	R/W	0x0	ADC0_HOLD_IRQ_EN. ADC 0 Hold Key IRQ Enable 0: Disable 1: Enable
1	R/W	0x0	ADC0_KEYDOWN_EN ADC 0 Key Down Enable 0: Disable 1: Enable
0	R/W	0x0	ADC0_DATA_IRQ_EN. ADC 0 Data IRQ Enable 0: Disable 1: Enable

LRADC INTERRUPT STATUS REGISTER

Offset: 0x08			Register Name: LRADC_INT
Bit	Read/Writ e	Default/H ex	Description
31: 5	/	/	/
4	R/W	0x0	<p>ADCO_KEYUP_PENDING. ADC 0 Key up pending Bit When general key pull up, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Note: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable</p>
3	R/W	0x0	<p>ADCO_ALRDY_HOLD_PENDING. ADC 0 Already Hold Pending Bit When hold key pull down and pull the general key down, if the corresponding interrupt is enabled. 0: No IRQ 1: IRQ Pending Notes: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable</p>
2	R/W	0x0	<p>ADCO_HOLDKEY_PENDING. ADC 0 Hold Key pending Bit When Hold key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled. 0: NO IRQ 1: IRQ Pending Note: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.</p>
1	R/W	0x0	ADCO_KEYDOWN_PENDING.

			<p>ADC 0 Key Down IRQ Pending Bit</p> <p>When General key pull down, the status bit is set and the interrupt line is set if the corresponding interrupt is enabled.</p> <p>0: No IRQ</p> <p>1: IRQ Pending</p> <p>Note: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.</p>
0	R/W	0x0	<p>ADC0_DATA_PENDING.</p> <p>ADC 0 Data IRQ Pending Bit</p> <p>0: No IRQ</p> <p>1: IRQ Pending</p> <p>Note: Writing 1 to the bit will clear it and its corresponding interrupt if the interrupt is enable.</p>

LRADC DATA REGISTER

Offset: 0x0c			Register Name: LRADC_DATA
Bit	Read/Writ e	Default/H ex	Description
31: 6	/	/	/
5:0	R	0x0	<p>LRADC_DATA.</p> <p>LRADC Data</p>

3.19 Thermal Sensor Controller

3.19.1 Overview

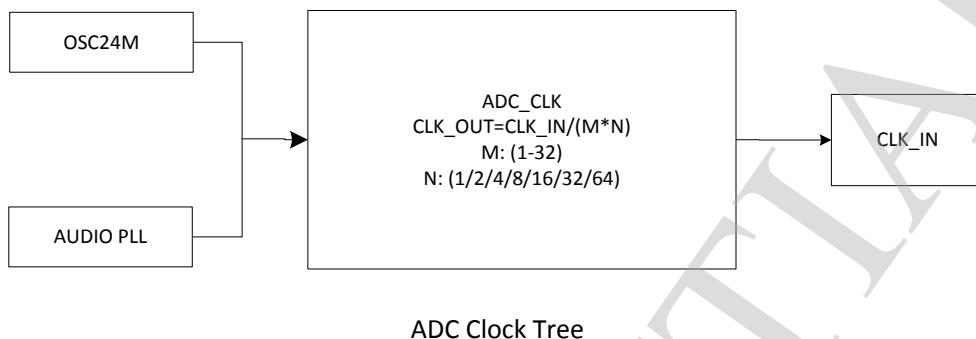
The A23 supports thermal sensor controller to monitor the chip temperature.

It features:

- Low power consumption
- Median and averaging filter to reduce noise

3.19.2 Clock Tree and ADC Conversion Time

CLOCK TREE



A/D CONVERSION TIME

When the clock source is 24MHz and the prescaler value M*N is 6, total 12-bit conversion time is as follows.

$$\text{CLK_IN} = 24\text{MHz}/6 = 4\text{MHz}$$

$$\text{Conversion Time} = 1/(4\text{MHz}/14\text{Cycles}) = 3.50\mu\text{s}$$

$$\text{If ADC acquire time divider is 5, then TACQ} = 1/(4\text{MHz}/6) = 1.50\mu\text{s}$$

FS_TIME (configured by the FS_DIV register) bases on the summation of Conversion Time and TACQ. The FS_TIME must be greater or equal than (TACQ + Conversion Time)

$$\text{FS_TIME} \geq \text{TACQ} + \text{Conversion Time} = 5.0\mu\text{s}$$

This A/D converter was designed to operate at maximum 24MHz clock, and the conversion rate can go up to 1 MSPS.

3.19.3 Thermal Measurement

$$T = (V_{AL} - 1669)/6.25 \text{ Celsius degree}$$

The V_{AL} should read from thermal value register.

3.19.4 Thermal Sensor Controller Register List

Module Name	Base Address
THS	0x01C25000

Register Name	Offset	Description
THS_CTRL0	0x00	THS Control Register0
THS_CTRL1	0x04	THS Control Register1
THS_DATA_PENDING	0x14	THS Data Status
THSPER	0x18	THS Period Register
THSATA	0x20	THS Data Register

3.19.5 Thermal Sensor Controller Register Description

THS CONTROL REGISTER 0

Offset: 0x00			Register Name: THS_CTRL0
Bit	Read/ Write	Default /Hex	Description
31:24	R/W	0xF	<p>DATA_FIRST_DLY.</p> <p>DATA First Convert Delay Time(T_FCDT)setting</p> <p>Based on Data First Convert Delay Mode select (Bit 23)</p> <p>T_FCDT = DATA_FIRST_DLY * DATA_FIRST_DLY_MODE</p>
23	R/W	0x1	<p>DATA_FIRST_DLY_MODE.</p> <p>DATA First Convert Delay Mode Select</p> <p>0: CLK_IN/16</p> <p>1: CLK_IN/16*256</p>
22	/	/	/
21:20	R/W	0x0	<p>DATA_CLK_DIVIDER.</p> <p>DATA Clock Divider(CLK_IN)</p> <p>00: CLK/2</p> <p>01: CLK/3</p> <p>10: CLK/6</p> <p>11: CLK/1</p>
19:16	R/W	0x0	<p>FS_DIV.</p> <p>DATA Sample Frequency Divider</p> <p>0000: CLK_IN/2⁽²⁰⁻ⁿ⁾</p> <p>0001: CLK_IN/2⁽²⁰⁻ⁿ⁾</p> <p>0010: CLK_IN/2⁽²⁰⁻ⁿ⁾</p> <p>....</p> <p>....</p> <p>1111: CLK_IN/32</p>

15:0	R/W	0x0	TACQ. DATA acquire time CLK_IN/(16*(N+1))
------	-----	-----	---

THS CONTROL REGISTER 1

Offset: 0x04			Register Name: THS_CTRL1
Bit	Read/ Write	Default /Hex	Description
31:9	/	/	/
8	R/W	0x1	CHOP_TEMP_EN Chop temperature calibration enable 0: Disable 1: Enable
7:6	/	/	/
5	R/W	0x0	DATA_EN. DATA Function Enable 0: Disable 1: Enable
4:0	R/W	0x1	/

THS DATA STATUS REGISTER

Offset: 0x14			Register Name: DATA_FIFOS
Bit	Read/ Write	Default /Hex	Description
31:19	/	/	/
18	R/W	0x0	THS_DATA_PENDING. Thermal sensor data pending 0: No Pending 1: Thermal sensor data Pending Write '1' to clear this interrupt or automatic clear if data pending condition fails
17:1	/	/	

THS PERIOD REGISTER

Offset: 0x18			Register Name: THS_TPR
Bit	Read/ Write	Default /Hex	Description
31:16	/	/	/
16	R/W	0x0	THS_EN. Thermal sensor enable
15:0	R/W	0x0	THS_PER. Thermal sensor Period 4096*(1/clk_in)

THS DATA REGISTER

Offset: 0x20			Register Name: THS_DATA
Bit	Read/ Write	Default /Hex	Description
31:12	/	/	/
11:0	R	0x0	THS_DATA Thermal sensor data

3.20 Security System

The security system of A23 platform supports eight bonding package ID.

CONFIDENTIAL

3.21 Port Controller

3.21.1 Port Description

The chip has 8 ports for multi-functional input/out pins. They are shown below:

- Port A(PA): 8 input/output port
- Port B(PB): 8 input/output port
- Port C(PC): 19 input/output port
- Port D(PD): 28 input/output port
- Port E(PE) : 18 input/output port
- Port F(PF) : 6 input/output port
- Port G(PG) : 14 input/output port
- Port H(PH) : 10 input/output port
- Port L(PL) : 12 input/output port

For various system configurations, these ports can be easily configured by software. All these ports can be configured as GPIO if multiplexed functions are not used. The external PIO interrupt sources are supported and interrupt mode can be configured by software.

3.21.2 Port Register List

Module Name	Base Address
PIO	0x01C20800

Register Name	Offset	Description
Pn_CFG0	n*0x24+0x00	Port n Configure Register 0 (n from 0 to 6)
Pn_CFG1	n*0x24+0x04	Port n Configure Register 1 (n from 0 to 6)
Pn_CFG2	n*0x24+0x08	Port n Configure Register 2 (n from 0 to 6)
Pn_CFG3	n*0x24+0x0C	Port n Configure Register 3 (n from 0 to 6)
Pn_DAT	n*0x24+0x10	Port n Data Register (n from 0 to 6)
Pn_DRV0	n*0x24+0x14	Port n Multi-Driving Register 0 (n from 0 to 6)
Pn_DRV1	n*0x24+0x18	Port n Multi-Driving Register 1 (n from 0 to 6)
Pn_PUL0	n*0x24+0x1C	Port n Pull Register 0 (n from 0 to 6)
Pn_PUL1	n*0x24+0x20	Port n Pull Register 1 (n from 0 to 6)
Pn_INT_CFG0	0x200+n*0x20+0x00	PIO Interrupt Configure Register 0
Pn_INT_CFG1	0x200+n*0x20+0x04	PIO Interrupt Configure Register 1
Pn_INT_CFG2	0x200+n*0x20+0x08	PIO Interrupt Configure Register 2
Pn_INT_CFG3	0x200+n*0x20+0x0C	PIO Interrupt Configure Register 3
Pn_INT_CTL	0x200+n*0x20+0x10	PIO Interrupt Control Register
Pn_INT_STA	0x200+n*0x20+0x14	PIO Interrupt Status Register
Pn_INT_DEB	0x200+n*0x20+0x18	PIO Interrupt Debounce Register

3.21.3 Port Register Description

PA CONFIGURE REGISTER 0

Offset: 0x00			Register Name: PA_CFG0
Default Value: 0x7777_7777			
Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0x7	PA7_SELECT 000: Input 001: Output 010: UART4_CTS 011: Reserved 100: PA_EINT7 101: Reserved 110: Reserved 111: IO Disable
27	/	/	Reserved
26:24	R/W	0x7	PA6_SELECT 000: Input 001: Output 010: UART4_RTS 011: Reserved 100: PA_EINT6 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PA5_SELECT 000: Input 001: Output 010: UART4_RX 011: Reserved 100: PA_EINT5 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PA4_SELECT 000: Input 001: Output 010: UART4_TX 011: Reserved

			100: PA_EINT4	101: Reserved
			110: Reserved	111: IO Disable
15	/	/	/	
			PA3_SELECT	
			000: Input	001: Output
			010: SPI1_MISO	011: JTAG_DIO
			100: PA_EINT3	101: Reserved
14:12	R/W	0x7	110: Reserved	111: IO Disable
11	/	/	/	
			PA2_SELECT	
			000: Input	001: Output
			010: SPI1_MOSI	011: JTAG_D00
			100: PA_EINT2	101: Reserved
10:8	R/W	0x7	110: Reserved	111: IO Disable
7	/	/	/	
			PA1_SELECT	
			000: Input	001: Output
			010: SPI1_CLK	011: JTAG_CK0
			100: PA_EINT1	101: Reserved
6:4	R/W	0x7	110: Reserved	111: IO Disable
3	/	/	Reserved	
			PA0_SELECT	
			000: Input	001: Output
			010: SPI1_CS	011: JTAG_MS0
			100: PA_EINT0	101: Reserved
2:0	R/W	0x7	110: Reserved	111: IO Disable

PA CONFIGURE REGISTER 1

Offset: 0x04	Register Name: PA_CFG1
--------------	------------------------

			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PA CONFIGURE REGISTER 2

			Register Name: PA_CFG2
Offset: 0x08			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PA CONFIGURE REGISTER 3

			Register Name: PA_CFG3
Offset: 0x0C			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PA DATA REGISTER

			Register Name: PA_DAT
Offset: 0x10			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0	<p>PA_DAT</p> <p>If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.</p>

PA MULTI-DRIVING REGISTER 0

Offset: 0x14	Register Name: PA_DRV0
--------------	------------------------

			Default Value: 0x0000_5555
Bit	Read/Write	Default	Description
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x1	PA_DRV PA[n] Multi-Driving Select (n = 0~7) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

PA MULTI-DRIVING REGISTER 1

			Register Name: PA_DRV1
Offset: 0x18			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PA PULL REGISTER 0

			Register Name: PA_PULL0
Offset: 0x1C			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:16	/	/	/
[2i+1:2i] (i=0~7)	R/W	0x0	PA_PULL PA[n] Pull-up/down Select (n = 0~7) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PA PULL REGISTER 1

			Register Name: PA_PULL1
Offset: 0x20			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

Bit	Read/Write	Default	Description
31:0	/	/	/

PB CONFIGURE REGISTER 0

Offset: 0x24			Register Name: PB_CFG0 Default Value: 0x7777_7777
Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0x7	PB7_SELECT 000: Input 010: PCMO_DIN 100: PB_EINT7 110: Reserved 001: Output 011: Reserved 101: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PB6_SELECT 000: Input 010: PCMO_DOUT 100: PB_EINT6 110: Reserved 001: Output 011: Reserved 101: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PB5_SELECT 000: Input 010: PCMO_CLK 100: PB_EINT5 110: Reserved 001: Output 011: Reserved 101: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PB4_SELECT 000: Input 001: Output

			010: PCMO_SYNC	011: Reserved
			100: PB_EINT4	101: Reserved
			110: Reserved	111: IO Disable
15	/	/	/	
			PB3_SELECT	
			000: Input	001: Output
			010: UART2_CTS	011: Reserved
			100: PB_EINT3	101: Reserved
14:12	R/W	0x7	110: Reserved	111: IO Disable
11	/	/	/	
			PB2_SELECT	
			000: Input	001: Output
			010: UART2_RTS	011: Reserved
			100: PB_EINT2	101: Reserved
10:8	R/W	0x7	110: Reserved	111: IO Disable
7	/	/	/	
			PB1_SELECT	
			000: Input	001: Output
			010: UART2_RX	011: Reserved
			100: PB_EINT1	101: Reserved
6:4	R/W	0x7	110: Reserved	111: IO Disable
3	/	/	/	
			PB0_SELECT	
			000: Input	001: Output
			010: UART2_TX	011: Reserved
			100: PB_EINT0	101: Reserved
2:0	R/W	0x7	110: Reserved	111: IO Disable

PB CONFIGURE REGISTER 1

			Register Name: PB_CFG1
Offset: 0x28			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PB CONFIGURE REGISTER 2

			Register Name: PB_CFG2
Offset: 0x2C			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PB CONFIGURE REGISTER 3

			Register Name: PB_CFG3
Offset: 0x30			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PB DATA REGISTER

			Register Name: PB_DAT
Offset: 0x34			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0	<p>PB_DAT</p> <p>If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.</p>

PB MULTI-DRIVING REGISTER 0

Offset: 0x38			Register Name: PB_DRV0 Default Value: 0x0000_5555
Bit	Read/Write	Default	Description
31:16	/	/	Reserved
[2i+1:2i] (i=0~7)	R/W	0x1	PB_DRV PB[n] Multi-Driving Select (n = 0~7) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

PB MULTI-DRIVING REGISTER 1

Offset: 0x3C			Register Name: PB_DRV1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PB PULL REGISTER 0

Offset: 0x40			Register Name: PB_PULL0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:16	/	/	Reserved
[2i+1:2i] (i=0~7)	R/W	0x0	PB_PULL PB[n] Pull-up/down Select (n = 0~7) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PB PULL REGISTER 1

Offset: 0x44			Register Name: PB_PULL1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PC CONFIGURE REGISTER 0

Offset: 0x48			Register Name: PC_CFG0 Default Value: 0x7777_7777
Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0x7	PC7_SELECT 000: Input 010: NAND_RB1 100: Reserved 110: Reserved 001: Output 011: Reserved 101: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PC6_SELECT 000: Input 001: Output 010: NAND_RB0 011: SDC2_CMD 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PC5_SELECT 000: Input 001: Output 010: NAND_RE 011: SDC2_CLK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

19	/	/	/	
18:16	R/W	0x7	PC4_SELECT 000: Input 010: NAND_CE0 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PC3_SELECT 000: Input 010: NAND_CE1 100: Reserved 110: Reserved	001: Output 011: SPI0_CS 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PC2_SELECT 000: Input 010: NAND_CLE 100: Reserved 110: Reserved	001: Output 011: SPI0_CLK 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PC1_SELECT 000: Input 010: NAND_ALE 100: Reserved 110: Reserved	001: Output 011: SPI0_MISO 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PC0_SELECT 000: Input 010: NAND_WE 100: Reserved	001: Output 011: SPI0_MOSI 101: Reserved

			110: Reserved	111: IO Disable
--	--	--	---------------	-----------------

PC CONFIGURE REGISTER 1

Offset: 0x4C			Register Name: PC_CFG1	
Bit	Read/Write	Default	Description	
31	/	/	/	
30:28	R/W	0x7	PC15_SELECT 000: Input 010: NAND_DQ7 100: Reserved 110: Reserved	001: Output 011: SDC2_D7 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PC14_SELECT 000: Input 010: NAND_DQ6 100: Reserved 110: Reserved	001: Output 011: SDC2_D6 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PC13_SELECT 000: Input 010: NAND_DQ5 100: Reserved 110: Reserved	001: Output 011: SDC2_D5 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PC12_SELECT 000: Input 010: NAND_DQ4 100: Reserved	001: Output 011: SDC2_D4 101: Reserved

			110: Reserved	111: IO Disable
15	/	/	/	
			PC11_SELECT	
			000: Input	001: Output
			010: NAND_DQ3	011: SDC2_D3
			100: Reserved	101: Reserved
14:12	R/W	0x7	110: Reserved	111: IO Disable
11	/	/	/	
			PC10_SELECT	
			000: Input	001: Output
			010: NAND_DQ2	011: SDC2_D2
			100: Reserved	101: Reserved
10:8	R/W	0x7	110: Reserved	111: IO Disable
7	/	/	/	
			PC9_SELECT	
			000: Input	001: Output
			010: NAND_DQ1	011: SDC2_D1
			100: Reserved	101: Reserved
6:4	R/W	0x7	110: Reserved	111: IO Disable
3	/	/	/	
			PC8_SELECT	
			000: Input	001: Output
			010: NAND_DQ0	011: SDC2_D0
			100: Reserved	101: Reserved
2:0	R/W	0x7	110: Reserved	111: IO Disable

PC CONFIGURE REGISTER 2

Offset: 0x50	Register Name: PC_CFG2 Default Value: 0x0000_0777
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Bit	Read/Write	Default	Description
31:11	/	/	/
10:8	R/W	0x7	PC18_SELECT 000: Input 001: Output 010: NAND_CE3 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
7	/	/	/
6:4	R/W	0x7	PC17_SELECT 000: Input 001: Output 010: NAND_CE2 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
3	/	/	/
2:0	R/W	0x7	PC16_SELECT 000: Input 001: Output 010: NAND_DQS 011: SDC2_RST 100: Reserved 101: Reserved 110: Reserved 111: IO Disable

PC CONFIGURE REGISTER 3

Offset: 0x54			Register Name: PC_CFG3 Default Value: 0x0000_0000
Bit Read/Write Default Description			
31:0	/	/	/

PC DATA REGISTER

Offset: 0x58			Register Name: PC_DAT Default Value: 0x0000_0000
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Bit	Read/Write	Default	Description
31:19	/	/	/
18:0	R/W	0	<p>PC_DAT</p> <p>If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.</p>

PC MULTI-DRIVING REGISTER 0

Offset: 0x5C			Register Name: PC_DRV0 Default Value: 0x5555_5555				
Bit	Read/Write	Default	Description				
[2i+1:2i] (i=0~15)	R/W	0x1	<p>PC_DRV</p> <p>PC[n] Multi-Driving_SELECT (n = 0~15)</p> <table> <tr> <td>00: Level 0</td> <td>01: Level 1</td> </tr> <tr> <td>10: Level 2</td> <td>11: Level 3</td> </tr> </table>	00: Level 0	01: Level 1	10: Level 2	11: Level 3
00: Level 0	01: Level 1						
10: Level 2	11: Level 3						

PC MULTI-DRIVING REGISTER 1

Offset: 0x60			Register Name: PC_DRV1 Default Value: 0x0000_0015				
Bit	Read/Write	Default	Description				
31:6	/	/	/				
[2i+1:2i] (i=0~2)	R/W	0x1	<p>PC_DRV</p> <p>PC[n] Multi-Driving Select (n = 16~18)</p> <table> <tr> <td>00: Level 0</td> <td>01: Level 1</td> </tr> <tr> <td>10: Level 2</td> <td>11: Level 3</td> </tr> </table>	00: Level 0	01: Level 1	10: Level 2	11: Level 3
00: Level 0	01: Level 1						
10: Level 2	11: Level 3						

PC PULL REGISTER 0

Offset: 0x64			Register Name: PC_PULL0 Default Value: 0x0000_5140
Bit	Read/Writ e	Default	Description
[2i+1:2i] (i=0~15)	R/W	0x00005140	PC_PULL PC[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PC PULL REGISTER 1

Offset: 0x68			Register Name: PC_PULL1 Default Value: 0x0000_0014
Bit	Read/Writ e	Default	Description
31:6	/	/	/
[2i+1:2i] (i=0~2)	R/W	0x00000014	PC_PULL PC[n] Pull-up/down Select (n = 16~18) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PD CONFIGURE REGISTER 0

Offset: 0x6C			Register Name: PD_CFG0 Default Value: 0x7777_7777
Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0x7	PD7_SELECT 000: Input 001: Output 010: LCD_D7 011: SDC1_D3

			100: Reserved 110: Reserved	101: Reserved 111: IO Disable
27	/	/	Reserved	
			PD6_SELECT 000: Input 010: LCD_D6 100: Reserved 110: Reserved	001: Output 011: SDC1_D2 101: Reserved 111: IO Disable
26:24	R/W	0x7		
23	/	/	/	
			PD5_SELECT 000: Input 010: LCD_D5 100: Reserved 110: Reserved	001: Output 011: SDC1_D1 101: Reserved 111: IO Disable
22:20	R/W	0x7		
19	/	/	/	
			PD4_SELECT 000: Input 010: LCD_D4 100: Reserved 110: Reserved	001: Output 011: SDC1_D0 101: Reserved 111: IO Disable
18:16	R/W	0x7		
15	/	/	/	
			PD3_SELECT 000: Input 010: LCD_D3 100: Reserved 110: Reserved	001: Output 011: SD1_CMD 101: Reserved 111: IO Disable
14:12	R/W	0x7		
11	/	/	/	
10:8	R/W	0x7	PD2_SELECT 000: Input	001: Output

			010: LCD_D2 100: Reserved 110: Reserved	011: SDC1_CLK 101: Reserved 111: IO Disable
7	/	/	/	
			PD1_SELECT 000: Input 010: LCD_D1 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
6:4	R/W	0x7		
3	/	/	/	
			PDO_SELECT 000: Input 010: LCD_D0 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
2:0	R/W	0x7		

PD CONFIGURE REGISTER 1

Offset: 0x70			Register Name: PD_CFG1 Default Value: 0x7777_7777
Bit	Read/Write	Default	Description
31	/	/	/
			PD15_SELECT 000: Input 010: LCD_D15 100: Reserved 110: Reserved
30:28	R/W	0x7	001: Output 011: PCM1_CLK 101: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PD14_SELECT 000: Input 001: Output

			010: LCD_D14 100: Reserved 110: Reserved	011: PCM1_SYNC 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PD13_SELECT 000: Input 010: LCD_D13 100: Reserved 110: Reserved	001: Output 011: UART1_CTS 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PD12_SELECT 000: Input 010: LCD_D12 100: Reserved 110: Reserved	001: Output 011: UART1_RTS 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PD11_SELECT 000: Input 010: LCD_D11 100: Reserved 110: Reserved	001: Output 011: UART1_RX 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PD10_SELECT 000: Input 010: LCD_D10 100: Reserved 110: Reserved	001: Output 011: UART1_TX 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PD9_SELECT	

			000: Input 010: LCD_D9 100: Reserved 110: Reserved	001: Output 011: UART3_RX 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PD8_SELECT 000: Input 010: LCD_D8 100: Reserved 110: Reserved	001: Output 011: UART3_TX 101: Reserved 111: IO Disable

PD CONFIGURE REGISTER 2

Offset: 0x74			Register Name: PD_CFG2	
Default Value: 0x7777_7777				
Bit	Read/Write	Default	Description	
31	/	/	/	
30:28	R/W	0x7	PD23_SELECT 000: Input 010: LCD_D23 100: Reserved 110: Reserved	001: Output 011: LVDS_VN2 101: Reserved 111: IO Disable
27	/	/	/	
26:24	R/W	0x7	PD22_SELECT 000: Input 010: LCD_D22 100: Reserved 110: Reserved	001: Output 011: LVDS_VP2 101: Reserved 111: IO Disable
23	/	/	/	
22:20	R/W	0x7	PD21_SELECT	

			000: Input 010: LCD_D21 100: Reserved 110: Reserved	001: Output 011: LVDS_VN1 101: Reserved 111: IO Disable
19	/	/	/	
18:16	R/W	0x7	PD20_SELECT 000: Input 010: LCD_D20 100: Reserved 110: Reserved	001: Output 011: LVDS_VP1 101: Reserved 111: IO Disable
15	/	/	/	
14:12	R/W	0x7	PD19_SELECT 000: Input 010: LCD_D19 100: Reserved 110: Reserved	001: Output 011: LVDS_VN0 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PD18_SELECT 000: Input 010: LCD_D18 100: Reserved 110: Reserved	001: Output 011: LVDS_VP0 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x7	PD17_SELECT 000: Input 010: LCD_D17 100: Reserved 110: Reserved	001: Output 011: PCM1_DIN 101: Reserved 111: IO Disable
3	/	/	/	

			PD16_SELECT
2:0	R/W	0x7	000: Input 001: Output
			010: LCD_D16 011: PCM1_DOUT
			100: Reserved 101: Reserved
			110: Reserved 111: IO Disable

PD CONFIGURE REGISTER 3

Offset: 0x78			Register Name: PD_CFG3
Default Value: 0x0000_7777			
Bit	Read/Write	Default	Description
31:16	/	/	/
15	/	/	/
			PD27_SELECT
			000: Input 001: Output
			010: LCD_VSYNC 011: LVDS_VN3
			100: Reserved 101: Reserved
14:12	R/W	0x7	110: Reserved 111: IO Disable
11	/	/	Reserved
			PD26_SELECT
			000: Input 001: Output
			010: LCD_HSYNC 011: LVDS_VP3
			100: Reserved 101: Reserved
10:8	R/W	0x7	110: Reserved 111: IO Disable
7	/	/	/
			PD25_SELECT
			000: Input 001: Output
			010: LCD_DE 011: LVDS_VNC
			100: Reserved 101: Reserved
6:4	R/W	0x7	110: Reserved 111: IO Disable

3	/	/	/
			PD24_SELECT
			000: Input 001: Output
			010: LCD_CLK 011: LVDS_VPC
			100: Reserved 101: Reserved
2:0	R/W	0x7	110: Reserved 111: IO Disable

PD DATA REGISTER

Offset: 0x7C			Register Name: PD_DAT Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:28	/	/	/
27:0	R/W	0	PD_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

PD MULTI-DRIVING REGISTER 0

Offset: 0x80			Register Name: PD_DRV0 Default Value: 0x5555_5555
Bit	Read/Write	Default	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

PD MULTI-DRIVING REGISTER 1

Offset: 0x84			Register Name: PD_DRV1 Default Value: 0x0055_5555
Bit	Read/Write	Default	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x1	PD_DRV PD[n] Multi-Driving Select (n = 16~27) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

PD PULL REGISTER 0

Offset: 0x88			Register Name: PD_PULL0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PD PULL REGISTER 1

Offset: 0x8C			Register Name: PD_PULL1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:24	/	/	/
[2i+1:2i] (i=0~11)	R/W	0x0	PD_PULL PD[n] Pull-up/down Select (n = 16~27) 00: Pull-up/down disable 01: Pull-up enable

)			10: Pull-down	11: Reserved	
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PE CONFIGURE REGISTER 0

Offset: 0x90			Register Name: PE_CFG0		
Bit	Read/Write	Default	Description		
31	/	/	/		
30:28	R/W	0x7	PE7_SELECT		
			000: Input	001: Output	
			010: CSI_D3	011: Reserved	
			100: Reserved	101: Reserved	
			110: Reserved	111: IO Disable	
27	/	/	/		
26:24	R/W	0x7	PE6_SELECT		
			000: Input	001: Output	
			010: CSI_D2	011: Reserved	
			100: Reserved	101: Reserved	
			110: Reserved	111: IO Disable	
23	/	/	/		
22:20	R/W	0x7	PE5_SELECT		
			000: Input	001: Output	
			010: CSI_D1	011: Reserved	
			100: Reserved	101: Reserved	
			110: Reserved	111: IO Disable	
19	/	/	/		
18:16	R/W	0x7	PE4_SELECT		
			000: Input	001: Output	
			010: CSI_D0	011: Reserved	
			100: Reserved	101: Reserved	

			110: Reserved	111: IO Disable
15	/	/	/	
			PE3_SELECT	
			000: Input	001: Output
			010: CSI_VSYNC	011: Reserved
			100: Reserved	101: Reserved
14:12	R/W	0x7	110: Reserved	111: IO Disable
11	/	/	/	
			PE2_SELECT	
			000: Input	001: Output
			010: CSI_HSYNC	011: Reserved
			100: Reserved	101: Reserved
10:8	R/W	0x7	110: Reserved	111: IO Disable
7	/	/	/	
			PE1_SELECT	
			000: Input	001: Output
			010: CSI_MCLK	011: Reserved
			100: Reserved	101: Reserved
6:4	R/W	0x7	110: Reserved	111: IO Disable
3	/	/	/	
			PE0_SELECT	
			000: Input	001: Output
			010: CSI_PCLK	011: Reserved
			100: Reserved	101: Reserved
2:0	R/W	0x7	110: Reserved	111: IO Disable

PE CONFIGURE REGISTER 1

Offset: 0x94	Register Name: PE_CFG1 Default Value: 0x7777_7777
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Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0x7	PE15_SELECT 000: Input 001: Output 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PE14_SELECT 000: Input 001: Output 010: Reserved 011: Reserved 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PE13_SELECT 000: Input 001: Output 010: CSI_SDA 011: TWI2_SDA 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PE12_SELECT 000: Input 001: Output 010: CSI_SCK 011: TWI2_SCK 100: Reserved 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/
14:12	R/W	0x7	PE11_SELECT 000: Input 001: Output 010: CSI_D7 011: Reserved

			100: Reserved	101: Reserved
			110: Reserved	111: IO Disable
11	/	/	/	
			PE10_SELECT	
			000: Input	001: Output
			010: CSI_D6	011: Reserved
			100: Reserved	101: Reserved
10:8	R/W	0x7	110: Reserved	111: IO Disable
7	/	/	/	
			PE9_SELECT	
			000: Input	001: Output
			010: CSI_D5	011: Reserved
			100: Reserved	101: Reserved
6:4	R/W	0x7	110: Reserved	111: IO Disable
3	/	/	/	
			PE8_SELECT	
			000: Input	001: Output
			010: CSI_D4	011: Reserved
			100: Reserved	101: Reserved
2:0	R/W	0x7	110: Reserved	111: IO Disable

PE CONFIGURE REGISTER 2

Offset: 0x98			Register Name: PE_CFG2
			Default Value: 0x0000_0077
Bit	Read/Write	Default	Description
31:7	/	/	/
6:4	R/W	0x7	PE17_SELECT 000: Input 001: Output 010: Reserved 011: Reserved

			100: Reserved 110: Reserved	101: Reserved 111: IO Disable
3	/	/	/	
			PE16_SELECT 000: Input 010: Reserved 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
2:0	R/W	0x7		

PE CONFIGURE REGISTER 3

Offset: 0x9C			Register Name: PE_CFG2 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PE DATA REGISTER

Offset: 0xA0			Register Name: PE_DAT Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:18	/	/	/
17:0	R/W	0	PE_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

PE MULTI-DRIVING REGISTER 0

Offset: 0xA4			Register Name: PE_DRV0 Default Value: 0x5555_5555
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Bit	Read/Write	Default	Description
[2i+1:2i] (i=0~15)	R/W	0x1	PE_DRV PE[n] Multi-Driving Select (n = 0~15) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

PE MULTI-DRIVING REGISTER 1

Offset: 0xA8			Register Name: PE_DRV1
			Default Value: 0x0000_0005
Bit	Read/Write	Default	Description
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x1	PE_DRV PE[n] Multi-Driving Select (n = 16~17) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

PE PULL REGISTER 0

Offset: 0xAC			Register Name: PE_PULL0
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
[2i+1:2i] (i=0~15)	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 0~15) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PE PULL REGISTER 1

Offset: 0xB0	Register Name: PE_PULL1
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			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:4	/	/	/
[2i+1:2i] (i=0~1)	R/W	0x0	PE_PULL PE[n] Pull-up/down Select (n = 16~17) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PF CONFIGURE REGISTER 0

			010: SDC0_CMD 100: Reserved 110: Reserved	011: JTAG_DO1 101: Reserved 111: IO Disable
11	/	/	/	
10:8	R/W	0x7	PF2_SELECT 000: Input 010: SDC0_CLK 100: Reserved 110: Reserved	001: Output 011: UART0_TX 101: Reserved 111: IO Disable
7	/	/	/	
6:4	R/W	0x3	PF1_SELECT 000: Input 010: SDC0_D0 100: Reserved 110: Reserved	001: Output 011: JTAG_DI1 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x3	PF0_SELECT 000: Input 010: SDC0_D1 100: Reserved 110: Reserved	001: Output 011: JTAG_MS1 101: Reserved 111: IO Disable

PF CONFIGURE REGISTER 1

Offset: 0xB8			Register Name: PF_CFG1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PF CONFIGURE REGISTER 2

			Register Name: PF_CFG2
Offset: 0xBC			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PF CONFIGURE REGISTER 3

			Register Name: PF_CFG3
Offset: 0xC0			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PF DATA REGISTER

			Register Name: PF_DAT
Offset: 0xC4			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:6	/	/	/
5:0	R/W	0	<p>PF_DAT</p> <p>If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.</p>

PF MULTI-DRIVING REGISTER 0

			Register Name: PF_DRV0
Offset: 0xC8			Default Value: 0x0000_0555
Bit	Read/Write	Default	Description
31:12	/	/	/

[2i+1:2i] (i=0~5)	R/W	0x1	PF_DRV PF[n] Multi-Driving Select (n = 0~5) 00: Level 0 01: Level 1 10: Level 2 11: Level 3
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PF MULTI-DRIVING REGISTER 1

Offset: 0xCC			Register Name: PF_DRV1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PF PULL REGISTER 0

Offset: 0xD0			Register Name: PF_PULL0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:12	/	/	/
[2i+1:2i] (i=0~5)	R/W	0x0	PF_PULL PF[n] Pull-up/down Select (n = 0~5) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PF PULL REGISTER 1

Offset: 0xD4			Register Name: PF_PULL1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PG CONFIGURE REGISTER 0

Offset: 0xD8			Register Name: PG_CFG0
Default Value: 0x7777_7777			
Bit	Read/Write	Default	Description
31	/	/	/
30:28	R/W	0x7	PG7_SELECT 000: Input 001: Output 010: UART1_RX 011: Reserved 100: PG_EINT7 101: Reserved 110: Reserved 111: IO Disable
27	/	/	/
26:24	R/W	0x7	PG6_SELECT 000: Input 001: Output 010: UART1_TX 011: Reserved 100: PG_EINT6 101: Reserved 110: Reserved 111: IO Disable
23	/	/	/
22:20	R/W	0x7	PG5_SELECT 000: Input 001: Output 010: SDC1_D3 011: Reserved 100: PG_EINT5 101: Reserved 110: Reserved 111: IO Disable
19	/	/	/
18:16	R/W	0x7	PG4_SELECT 000: Input 001: Output 010: SDC1_D2 011: Reserved 100: PG_EINT4 101: Reserved 110: Reserved 111: IO Disable
15	/	/	/

			PG3_SELECT
			000: Input 001: Output
			010: SDC1_D1 011: Reserved
			100: PG_EINT3 101: Reserved
14:12	R/W	0x7	110: Reserved 111: IO Disable
11	/	/	/
			PG2_SELECT
			000: Input 001: Output
			010: SDC1_D0 011: Reserved
			100: PG_EINT2 101: Reserved
10:8	R/W	0x7	110: Reserved 111: IO Disable
7	/	/	/
			PG1_SELECT
			000: Input 001: Output
			010: SDC1_CMD 011: Reserved
			100: PG_EINT1 101: Reserved
6:4	R/W	0x7	110: Reserved 111: IO Disable
3	/	/	/
			PG0_SELECT
			000: Input 001: Output
			010: SDC1_CLK 011: Reserved
			100: PG_EINT0 101: Reserved
2:0	R/W	0x7	110: Reserved 111: IO Disable

PG CONFIGURE REGISTER 1

Offset: 0xDC			Register Name: PG_CFG1 Default Value: 0x0077_7777
Bit	Read/Write	Default	Description
31:23	/	/	/

			PG13_SELECT	
			000: Input	001: Output
			010: PCM1_DIN	011: Reserved
			100: PG_EINT13	101: Reserved
22:20	R/W	0x7	110: Reserved	111: IO Disable
19	/	/	/	
			PG12_SELECT	
			000: Input	001: Output
			010: PCM1_DOUT	011: Reserved
			100: PG_EINT12	101: Reserved
18:16	R/W	0x7	110: Reserved	111: IO Disable
15	/	/	/	
			PG11_SELECT	
			000: Input	001: Output
			010: PCM1_CLK	011: Reserved
			100: PG_EINT11	101: Reserved
14:12	R/W	0x7	110: Reserved	111: IO Disable
11	/	/	/	
			PG10_SELECT	
			000: Input	001: Output
			010: PCM1_SYNC	011: Reserved
			100: PG_EINT10	101: Reserved
10:8	R/W	0x7	110: Reserved	111: IO Disable
7	/	/	/	
			PG9_SELECT	
			000: Input	001: Output
			010: UART1_CTS	011: Reserved
			100: PG_EINT9	101: Reserved
6:4	R/W	0x7	110: Reserved	111: IO Disable

3	/	/	/	
2:0	R/W	0x7	PG8_SELECT 000: Input 001: Output 010: UART1_RTS 011: Reserved 100: PG_EINT8 101: Reserved 110: Reserved 111: IO Disable	

PG CONFIGURE REGISTER 2

Offset: 0xE0			Register Name: PG_CFG2
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PG CONFIGURE REGISTER 3

Offset: 0xE4			Register Name: PG_CFG3
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PG DATA REGISTER

Offset: 0xE8			Register Name: PG_DAT
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:14	/	/	/
13:0	R/W	0	PG_DAT If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.

PG MULTI-DRIVING REGISTER 0

Offset: 0xEC			Register Name: PG_DRV0 Default Value: 0x0555_5555
Bit	Read/Write	Default	Description
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x1	PG_DRV PG[n] Multi-Driving Select (n = 0~13) 00: Level 0 01: Level 1 10: Level 2 11: Level 3

PG MULTI-DRIVING REGISTER 1

Offset: 0xF0			Register Name: PG_DRV1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PG PULL REGISTER 0

Offset: 0xF4			Register Name: PG_PULL0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:28	/	/	/
[2i+1:2i] (i=0~13)	R/W	0x0	PG_PULL PG[n] Pull-up/down Select (n = 0~13) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PG PULL REGISTER 1

Offset: 0xF8			Register Name: PG_PULL1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PH CONFIGURE REGISTER 0

			100: Reserved 110: Reserved	101: Reserved 111: IO Disable
19	/	/	/	
			PH4_SELECT 000: Input 010: TWI1_SCK 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
18:16	R/W	0x7		
15	/	/	/	
			PH3_SELECT 000: Input 010: TWI0_SDA 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
14:12	R/W	0x7		
11	/	/	/	
			PH2_SELECT 000: Input 010: TWI0_SCK 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
10:8	R/W	0x7		
7	/	/	/	
			PH1_SELECT 000: Input 010: PWM1 100: Reserved 110: Reserved	001: Output 011: Reserved 101: Reserved 111: IO Disable
6:4	R/W	0x7		
3	/	/	/	
2:0	R/W	0x7	PH0_SELECT 000: Input	001: Output

			010: PWM0	011: Reserved
			100: Reserved	101: Reserved
			110: Reserved	111: IO Disable

PH CONFIGURE REGISTER 1

Offset: 0x100			Register Name: PH_CFG1	
			Default Value: 0x0000_0077	
Bit	Read/Write	Default	Description	
31:7	/	/	/	
6:4	R/W	0x7	PH9_SELECT 000: Input 010: SPI0_DIN 100: Reserved 110: Reserved	001: Output 011: UART3_CTS 101: Reserved 111: IO Disable
3	/	/	/	
2:0	R/W	0x7	PH8_SELECT 000: Input 010: SPI0_DOUT 100: Reserved 110: Reserved	001: Output 011: UART3_RTS 101: Reserved 111: IO Disable

PH CONFIGURE REGISTER 2

Offset: 0x104			Register Name: PH_CFG2	
			Default Value: 0x0000_0000	
Bit	Read/Write	Default	Description	
31:0	/	/	/	

PH CONFIGURE REGISTER 3

Offset: 0x108	Register Name: PH_CFG3
---------------	------------------------

			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PH DATA REGISTER

			Register Name: PH_DAT
			Offset: 0x10C
Bit	Read/Write	Default	Description
31:10	/	/	/
9:0	R/W	0	<p>PH_DAT</p> <p>If the port is configured as input, the corresponding bit is the pin state. If the port is configured as output, the pin state is the same as the corresponding bit. The read bit value is the value setup by software. If the port is configured as functional pin, the undefined value will be read.</p>

PH MULTI-DRIVING REGISTER 0

			Register Name: PH_DRV0				
			Offset: 0x110				
Bit	Read/Write	Default	Description				
31:20	/	/	/				
[2i+1:2i] (i=0~9)	R/W	0x1	<p>PH_DRV</p> <p>PH[n] Multi-Driving Select (n = 0~9)</p> <table> <tr> <td>00: Level 0</td> <td>01: Level 1</td> </tr> <tr> <td>10: Level 2</td> <td>11: Level 3</td> </tr> </table>	00: Level 0	01: Level 1	10: Level 2	11: Level 3
00: Level 0	01: Level 1						
10: Level 2	11: Level 3						

PH MULTI-DRIVING REGISTER 1

			Register Name: PH_DRV1
			Offset: 0x114
			Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:0	/	/	/

PH PULL REGISTER 0

Offset: 0x118			Register Name: PH_PULL0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:20	/	/	/
[2i+1:2i] (i=0~9)	R/W	0	PH_PULL PH[n] Pull-up/down Select (n = 0~9) 00: Pull-up/down disable 01: Pull-up 10: Pull-down 11: Reserved

PH PULL REGISTER 1

Offset: 0x11C			Register Name: PH_PULL1 Default Value: 0x0000_0000
Bit	Read/Writ	Default	Description
31:0	/	/	/

PA EXTERNAL INTERRUPT CONFIGURE REGISTER 0

Offset: 0x200			Register Name: PA_EINT_CFG0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge

		0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved
--	--	--

PA EXTERNAL INTERRUPT CONFIGURE REGISTER 1

Offset: 0x204			Register Name: PA_EINT_CFG1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PA EXTERNAL INTERRUPT CONFIGURE REGISTER 2

Offset: 0x208			Register Name: PA_EINT_CFG2 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PA EXTERNAL INTERRUPT CONFIGURE REGISTER 3

Offset: 0x20C			Register Name: PA_EINT_CFG3 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PA EXTERNAL INTERRUPT CONTROL REGISTER

Offset: 0x210			Register Name: PA_EINT_CTL Default Value: 0x0000_0000
---------------	--	--	--

Bit	Read/Write	Default	Description
31:8	/	/	/
[n] (n=0~7)	R/W	0	EINT_CTL External INTn Enable (n = 0~7) 0: Disable 1: Enable

PA EXTERNAL INTERRUPT STATUS REGISTER

Offset: 0x214			Register Name: PA_EINT_STATUS Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
[n] (n=0~7)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~7) 0: No IRQ pending 1: IRQ pending Write '1' to clear

PA EXTERNAL INTERRUPT DEBOUNCE REGISTER

Offset: 0x218			Register Name: PA_EINT_DEB Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n.
3:1	/	/	/

			PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz
0	R/W	0	

PB EXTERNAL INTERRUPT CONFIGURE REGISTER 0

Offset: 0x220			Register Name: PB_EINT_CFG0 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
[4i+3:4i]] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

PB EXTERNAL INTERRUPT CONFIGURE REGISTER 1

Offset: 0x224			Register Name: PB_EINT_CFG1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PB EXTERNAL INTERRUPT CONFIGURE REGISTER 2

Offset: 0x228			Register Name: PB_EINT_CFG2 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description

		t	
31:0	/	/	/

PB EXTERNAL INTERRUPT CONFIGURE REGISTER 3

Offset: 0x22C			Register Name: PB_EINT_CFG3 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PB EXTERNAL INTERRUPT CONTROL REGISTER

Offset: 0x230			Register Name: PB_EINT_CTL Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
[n] (n=0~7)	R/W	0	EINT_CTL External INTn Enable (n = 0~7) 0: Disable 1: Enable

PB EXTERNAL INTERRUPT STATUS REGISTER

Offset: 0x234			Register Name: PB_EINT_STATUS Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
[n] (n=0~7)	R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~7) 0: No IRQ pending

			1: IRQ pending Write '1' to clear
--	--	--	--------------------------------------

PB EXTERNAL INTERRUPT DEBOUNCE REGISTER

Offset: 0x238			Register Name: PB_EINT_DEB
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
31:7	/	/	/
6:4	R/W	0	DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n The selected clock source is prescaled by 2^n .
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

PG EXTERNAL INTERRUPT CONFIGURE REGISTER 0

Offset: 0x240			Register Name: PG_EINT_CFG0
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
[4i+3:4i] (i=0~7)	R/W	0	EINT_CFG External INTn Mode (n = 0~7) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level

			0x4: Double Edge (Positive/ Negative) Others: Reserved
--	--	--	---

PG EXTERNAL INTERRUPT CONFIGURE REGISTER 1

Offset: 0x244			Register Name: PG_EINT_CFG1 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:24	/	/	/
[4i+3:4i] (i=0~5)	R/W	0	ENT_CFG External INTn Mode (n = 8~13) 0x0: Positive Edge 0x1: Negative Edge 0x2: High Level 0x3: Low Level 0x4: Double Edge (Positive/ Negative) Others: Reserved

PG EXTERNAL INTERRUPT CONFIGURE REGISTER 2

Offset: 0x248			Register Name: PG_EINT_CFG2 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	/	/	/

PG EXTERNAL INTERRUPT CONFIGURE REGISTER 3

Offset: 0x24C			Register Name: PG_EINT_CFG3 Default Value: 0x0000_0000
Bit	Read/Write	Default	Description

31:0	/	/	/	
------	---	---	---	--

PG EXTERNAL INTERRUPT CONTROL REGISTER

Offset: 0x250			Register Name: PG_EINT_CTL
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
31:14	/	/	/
[n] (n=0~13)	R/W	0	EINT_CTL External INTn Enable (n = 0~13) 0: Disable 1: Enable

PG EXTERNAL INTERRUPT STATUS REGISTER

Offset: 0x254			Register Name: PG_EINT_STATUS
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
31:14	/	/	/
[n] (n=0~13)	5R/W	0	EINT_STATUS External INTn Pending Bit (n = 0~13) 0: No IRQ pending 1: IRQ pending Write '1' to clear

PG EXTERNAL INTERRUPT DEBOUNCE REGISTER

Offset: 0x258			Register Name: PG_EINT_DEB
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description

31:7	/	/	/
			DEB_CLK_PRE_SCALE Debounce Clock Pre-scale n
6:4	R/W	0	The selected clock source is prescaled by 2^n .
3:1	/	/	/
0	R/W	0	PIO_INT_CLK_SELECT PIO Interrupt Clock Select 0: LOSC 32Khz 1: HOSC 24Mhz

Chapter 4

Memory

This chapter describes the memory subsystem of A23 processor from following perspectives:

- SDRAM Controller
- NAND Flash Controller

CONFIDENTIAL

4.1 SDRAM Controller

4.1.1 Overview

The SDRAM Controller (DRAMC) provides a simple, flexible, burst-optimized interface to all industry standard DDR3/DDR3L SDRAM.

The DRAMC automatically handles memory management, initialization, and refresh operations. It gives the host CPU a simple command interface, hiding details of the required address, page, and burst handling procedures. All memory parameters are runtime-configurable, including timing, memory setting, SDRAM type, and Extended-Mode-Register settings.

The DRAMC includes the following features:

- Support 16-bit single-channel DDR3/DDR3L SDRAM
- Support power voltage of 1.35V and 1.5V
- Support memory capacity up to 1GB
- Support 16 address lines and 3 bank address lines per channel
- Automatically generate initialization and refresh sequences
- Runtime-configurable parameters setting
- Configurable clock frequency
- Priority of transferring through multiple ports is programmable
- Support random read or write operations

4.2 NAND Flash Controller

4.2.1 Overview

The NDFC is the NAND Flash Controller which supports all NAND/MLC flash memory available in the market. New type flash can be supported by software re-configuration.

The On-the-fly error correction code (ECC) is built-in NDFC for enhancing reliability. BCH is implemented and it can detect and correct up to 64 bits error per 512 or 1024 bytes data. The on chip ECC and parity checking circuitry of NDFC frees CPU for other tasks. The ECC function can be disabled by software.

The data can be transferred by DMA or by CPU memory-mapped IO method. The NDFC provides automatic timing control for reading or writing external Flash. The NDFC maintains the proper relativity for CLE, CE# and ALE control signal lines. Three modes are supported for serial read access. The conventional serial access is mode 0 and mode 1 is for EDO type and mode 2 for extension EDO type. NDFC can monitor the status of R/B# signal line.

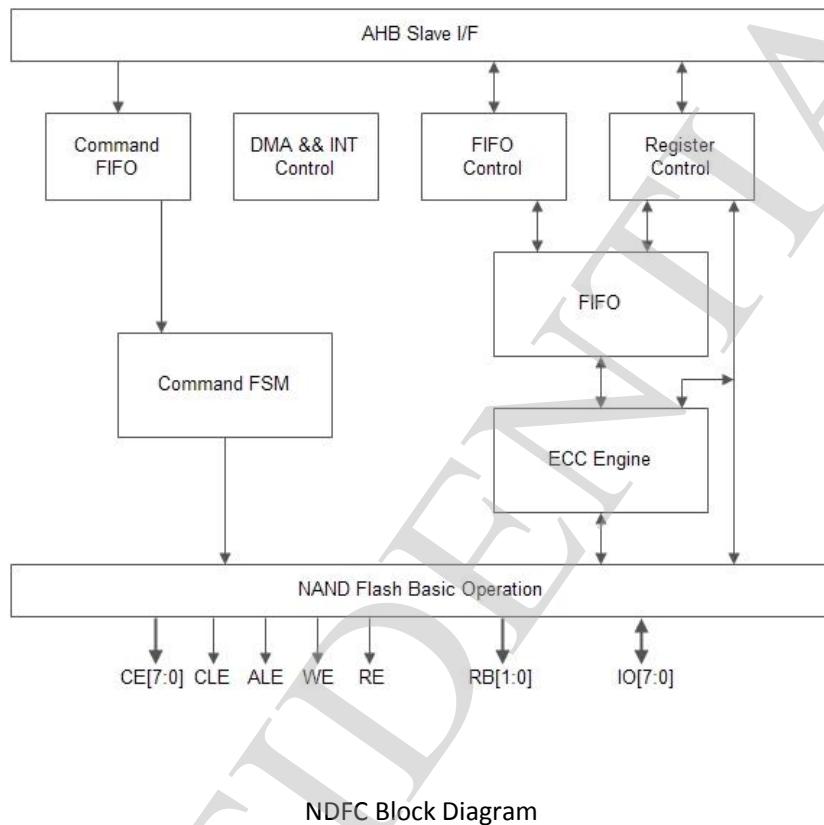
Block management and wear leveling management are implemented in software.

The NAND Flash Controller (NDFC) includes the following features:

- Comply to ONFI 2.3 and Toggle 1.0
- Support 64-bit ECC per 512 bytes or 1024 bytes
- 8-bit RAW NAND flash controller sharing pin with eMMC
- Support 3.0V IO voltage only
- Support up to 4 CE and 2 RB signals
- Support SLC/MLC/TLC NAND and EF-NAND

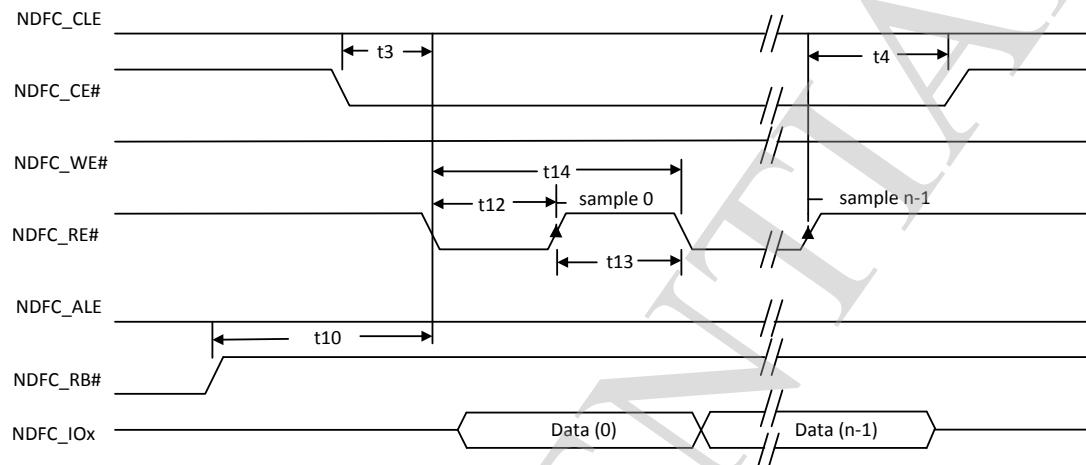
4.2.2 Block Diagram

The NAND Flash Controller (NDFC) system block diagram is shown below:

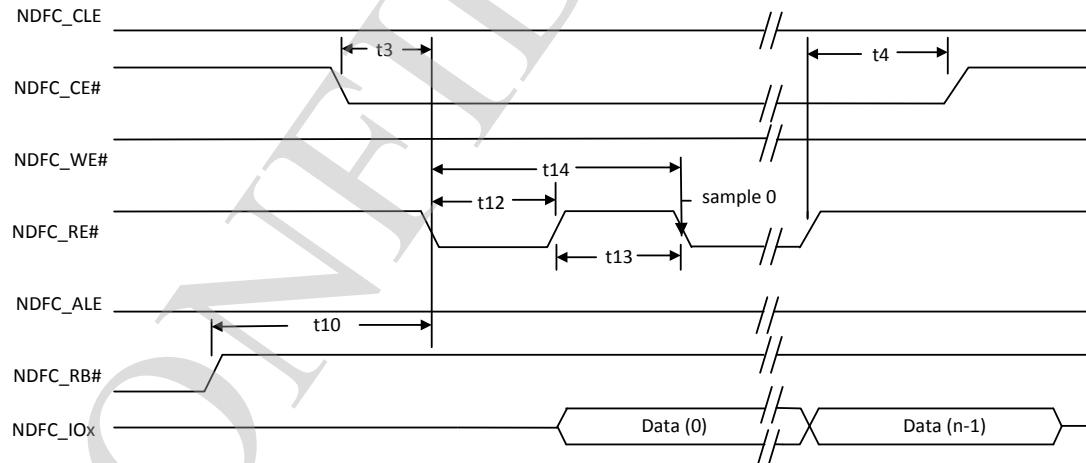


4.2.3 NDFC Timing Diagram

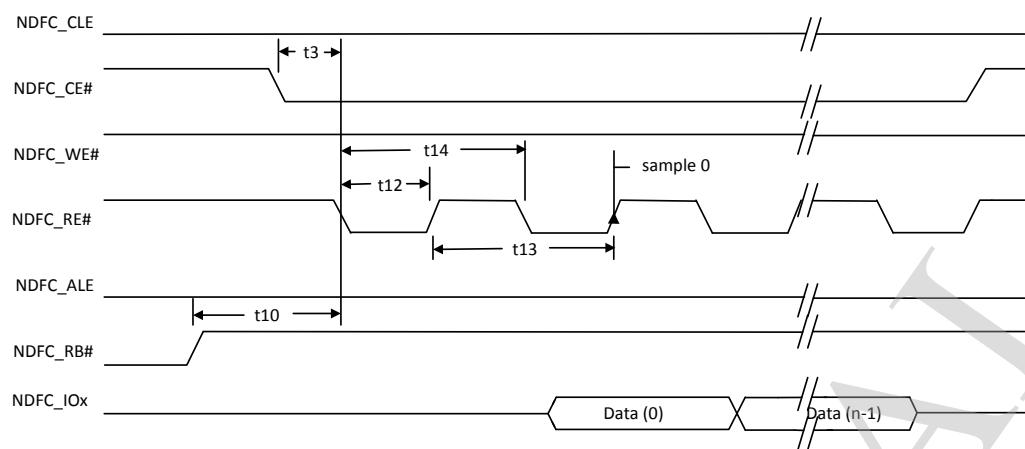
Typically, there are two kinds of serial access method. One method is conventional method which fetching data at the rise edge of NDFC_RE# signal line. Another one is EDO type which fetching data at the next fall edge of NDFC_RE# signal line.



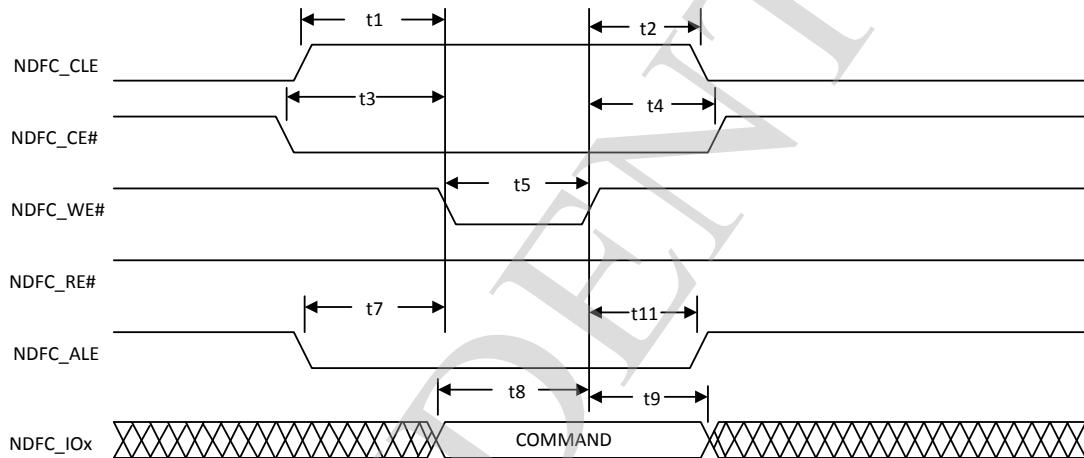
Conventional Serial Access Cycle Diagram (SAM0)



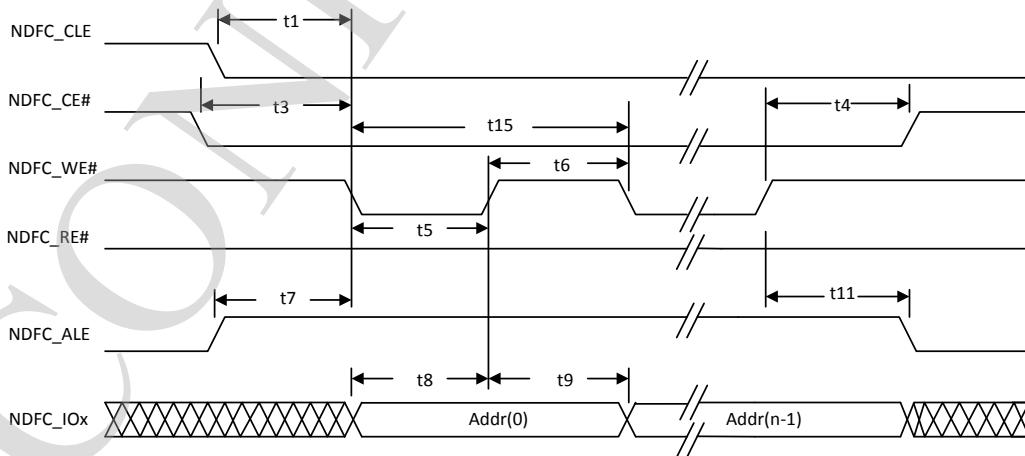
EDO type Serial Access after Read Cycle (SAM1)



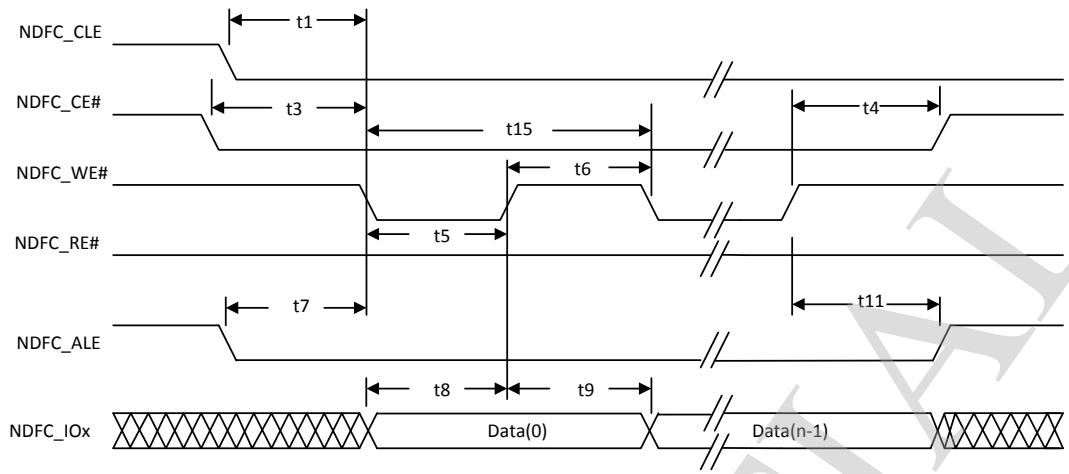
Extending EDO type Serial Access Mode (SAM2)



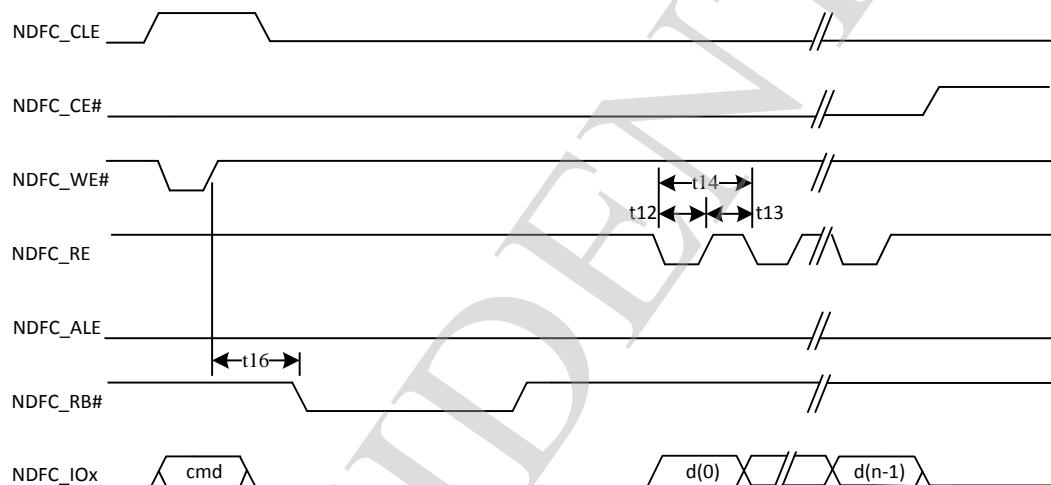
Command Latch Cycle



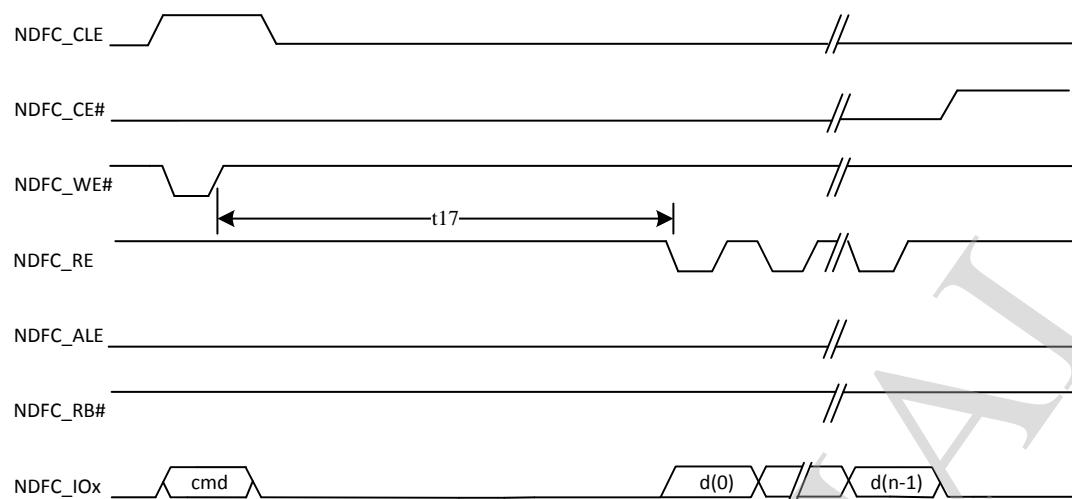
Address Latch Cycle



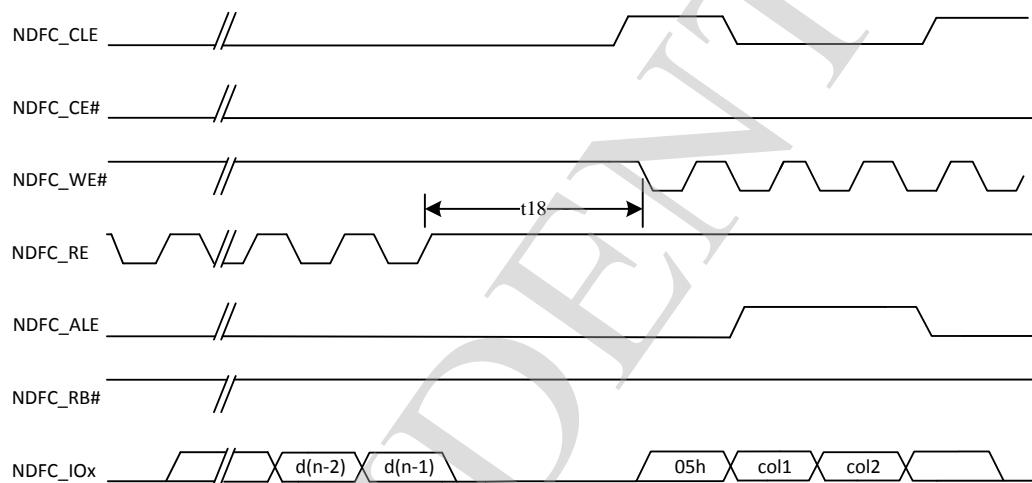
Write Data to Flash Cycle



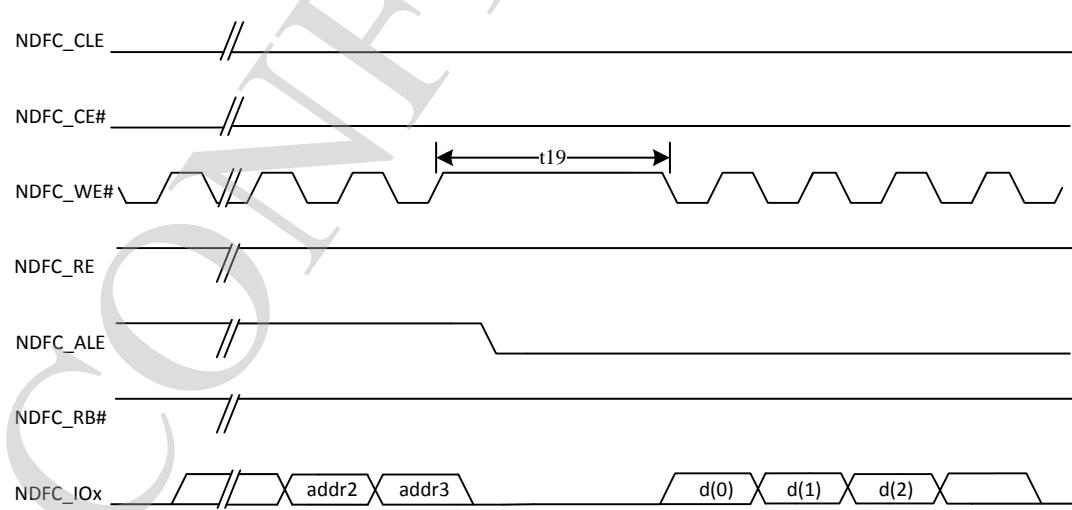
Waiting R/B# ready Diagram



WE# high to RE# low Timing Diagram



RE# high to WE# low Timing Diagram



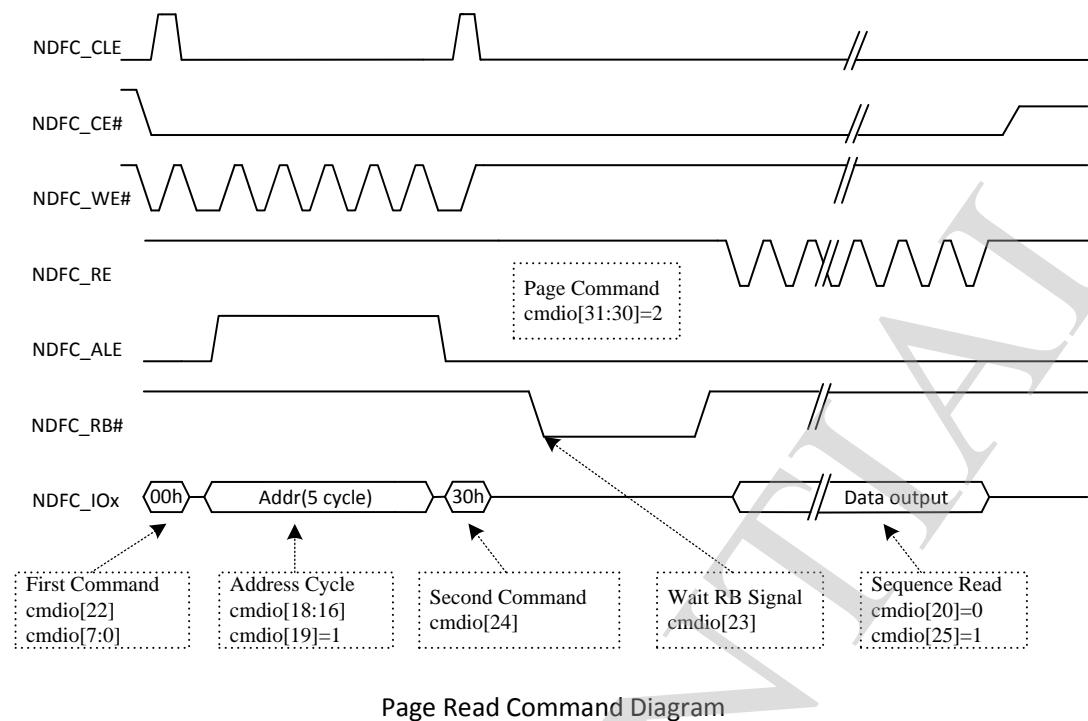
Address to Data Loading Timing Diagram

Timing cycle list

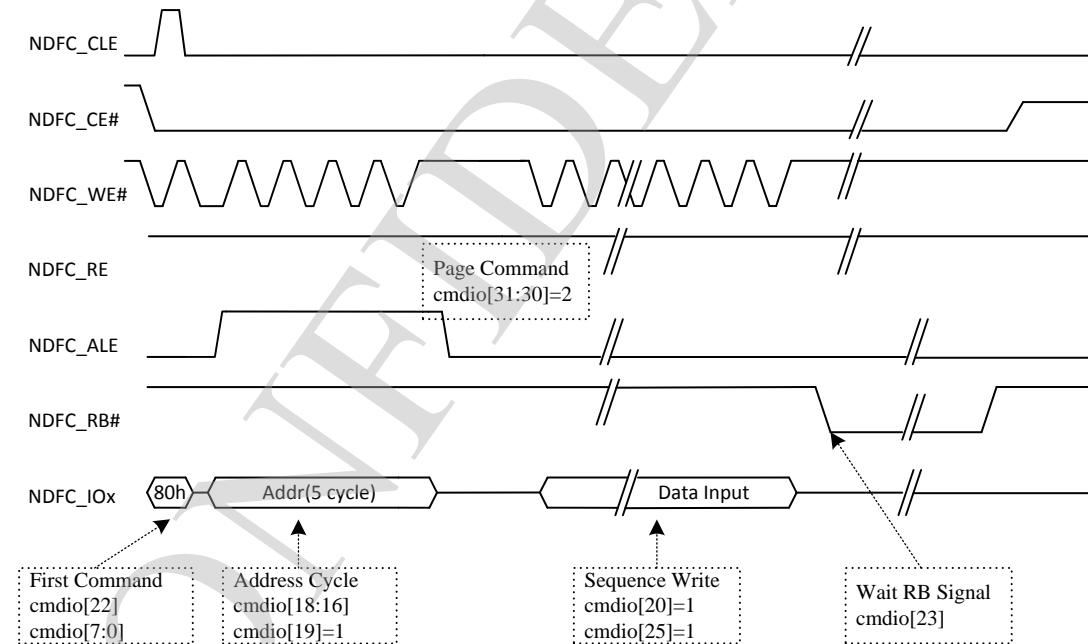
ID	Parameter	Timing	Notes
T1	NDFC_CLE setup time	T	
T2	NDFC_CLE hold time	T	
T3	NDFC_CE setup time	T	
T4	NDFC_CE hold time	T	
T5	NDFC_WE# pulse width	T	
T6	NDFC_WE# hold time	T	
T7	NDFC_ALE setup time	T	
T8	Data setup time	T	
T9	Data hold time	T	
T10	Ready to NDFC_RE# low	3T	
T11	NDFC_ALE hold time	T	
T12	NDFC_RE# pulse width	T	
T13	NDFC_RE# hold time	T	
T14	Read cycle time	2T	
T15	Write cycle time	2T	
T16	NDFC_WE# high to R/B# busy	tWB	Specified by timing configure register(NDFC_TIMING_CFG)
T17	NDFC_WE# high to NDFC_RE# low	tWHR	Specified by timing configure register(NDFC_TIMING_CFG)
T18	NDFC_RE# high to NDFC_WE# low	tRHW	Specified by timing configure register(NDFC_TIMING_CFG)
T19	Address to Data Loading time	tADL	Specified by timing configure register(NDFC_TIMING_CFG)

Note: T is the clock period duration of NDFC_CLK (x2).

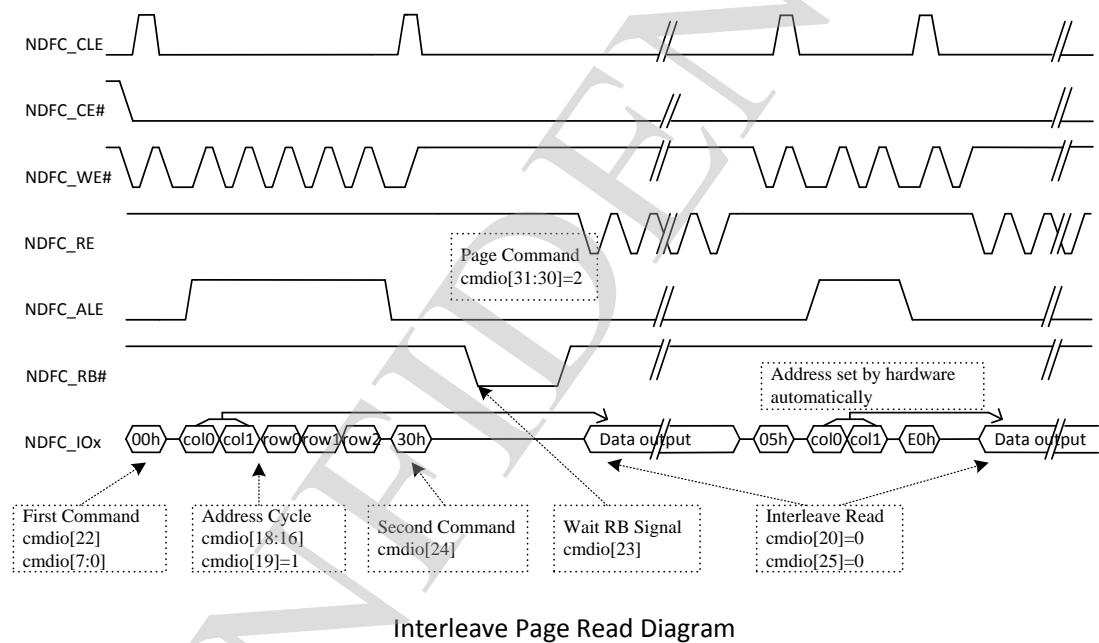
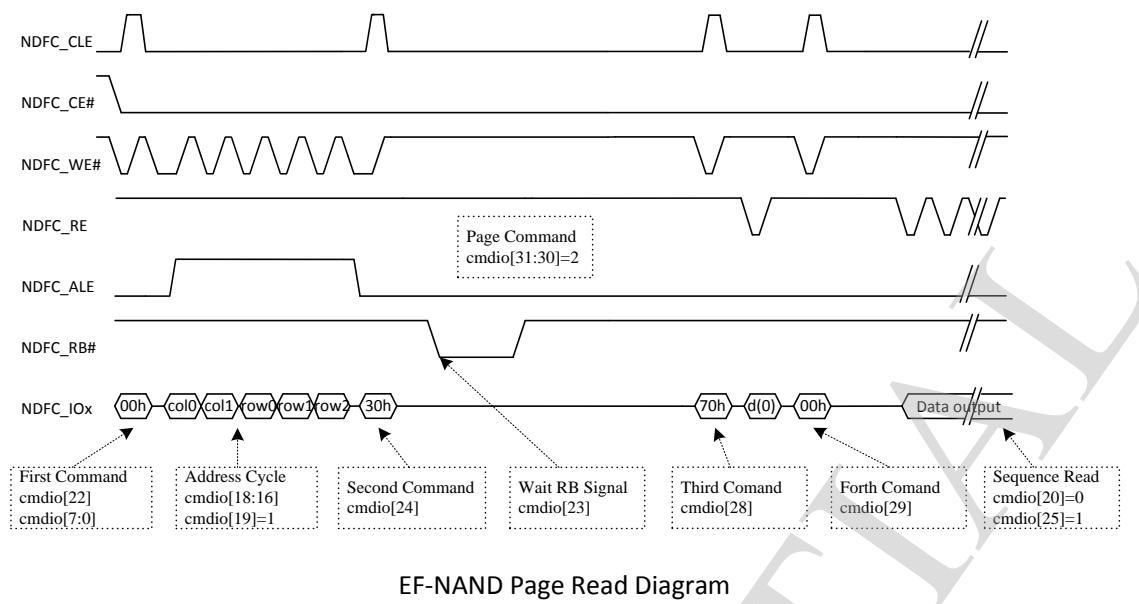
NDFC Operation Guide



Page Read Command Diagram



Page Program Diagram



Chapter 5

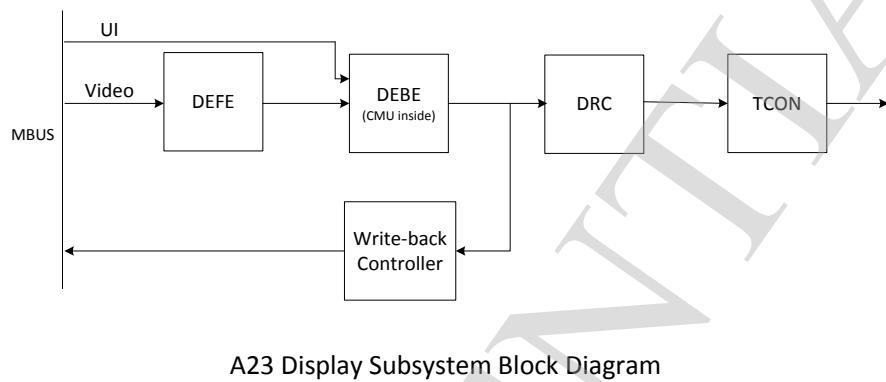
Display

This section describes the display subsystem from following perspectives:

- TCON
- Display Engine Front-End
- Display Engine Back-End
- MIPI DSI
- IEP (CMU, DRC, Write-back Controller)

5.1 Display Subsystem Block Diagram

The display subsystem of A23 processor consists of 6 sections, including DEFE, DEBE, CMU, DRC, TCON, and write-back controller. The six sections play different role in this subsystem, and cooperate with each other to meet diversified display requirements.



DEFE: video scaling, color space conversion, etc

DEBE: layer blending, etc

CMU: color adjustment for better vision effect

DRC: content-based backlight control for energy efficiency

TCON: LCD driver

Write-Back Controller: capture data between display engine and TCON for Miracast application

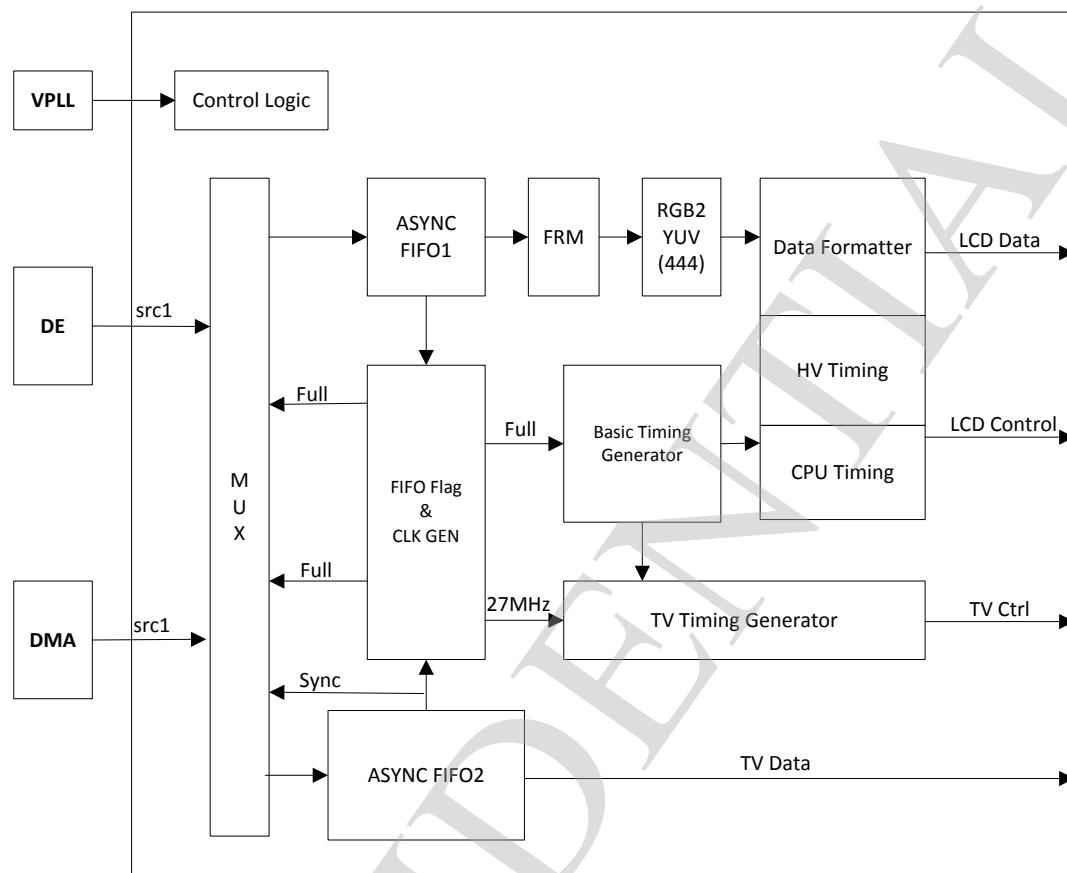
5.2 TCON

This section describes the timing controller of A23 platform.

5.2.1 Overview

- Support LVDS interface with single link, up to 1280X800@60fps
- Support RGB interface with DE/SYNC mode, up to 1280X800@60fps
- Support serial RGB/dummy RGB/CCIR656 interface, up to 1280X800@60fps
- Support i80 interface with 18/16/9/8 bit, support TE, up to 1280X800@60fps
- Supported pixel formats: RGB888, RGB666 and RGB565
- Support dither function from RGB666/RGB565 to RGB888
- Support Gamma correction with R/G/B channel independence

5.2.2 Block Diagram



TCON Block Diagram

5.2.3 TCON Function Description

PANEL INTERFACE

HV_I/F (Sync+DE mode)

HV I/F is also known as Sync + DE mode, which is widely used in TFT LCD module for PMP/MP4 applications.

Its signals are defined as below:

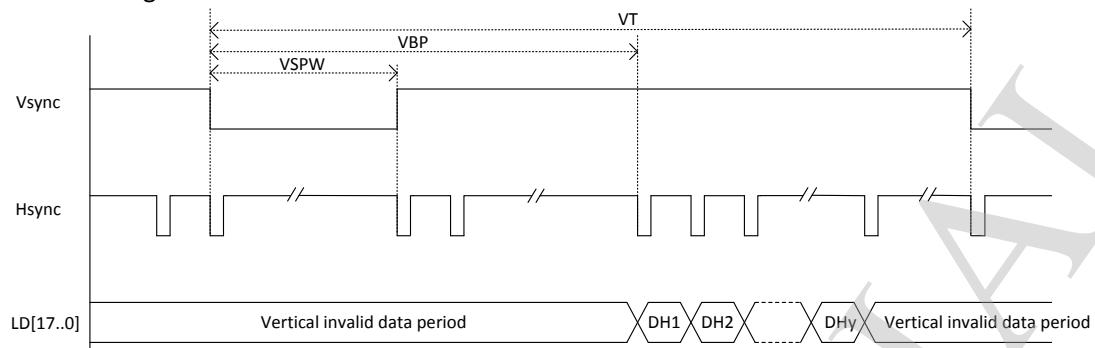
Main Signal	I/O Type	Description
Vsync	O	Vertical sync, indicating one new frame
Hsync	O	Horizontal sync, indicating one new scan line
DCLK	O	Dot clock, pixel data are synchronized by this clock
LDE	O	LCD data enable
LCD[17:0]	O	18-bit RGB/YUV output from input FIFO for panel

HV control signals are active low.

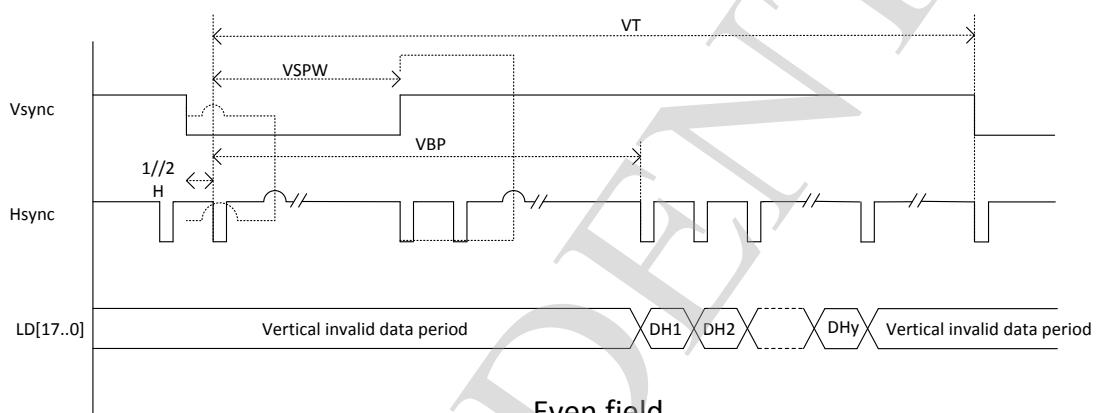
Following is the panel interface timing diagram:

Panel Interface Timing

Vertical Timing



Odd/Even field



Even field

When in HV serial YUV output mode, its timing is CCIR656 /601 compatible. SAV add right before active area every line; EAV add right after active area every line.

Its logic:

$$F = "0" \text{ for Field 1} \quad F = "1" \text{ for Field 2}$$

$$V = "1" \text{ during vertical blanking}$$

$$H = "0" \text{ at SAV} \quad H = "1" \text{ at EAV}$$

$$P3-P0 = \text{protection bits}$$

$$P3 = V \oplus H$$

$$P2 = F \oplus H$$

$$P1 = F \oplus V$$

$$P0 = F \oplus V \oplus H$$

Where \oplus represents the exclusive-OR function

The 4 byte SAV/EAV sequences are:

	8-bit Data								10-bit Data	
	D9 (MSB)	D8	D7	D6	D5	D4	D3	D2	D1	D0
Preamble	1	1	1	1	1	1	1	1	1	1
	0	0	0	0	0	0	0	0	0	0
	0	0	0	0	0	0	0	0	0	0
Status word	1	F	V	H	P3	P2	P1	P0	0	0

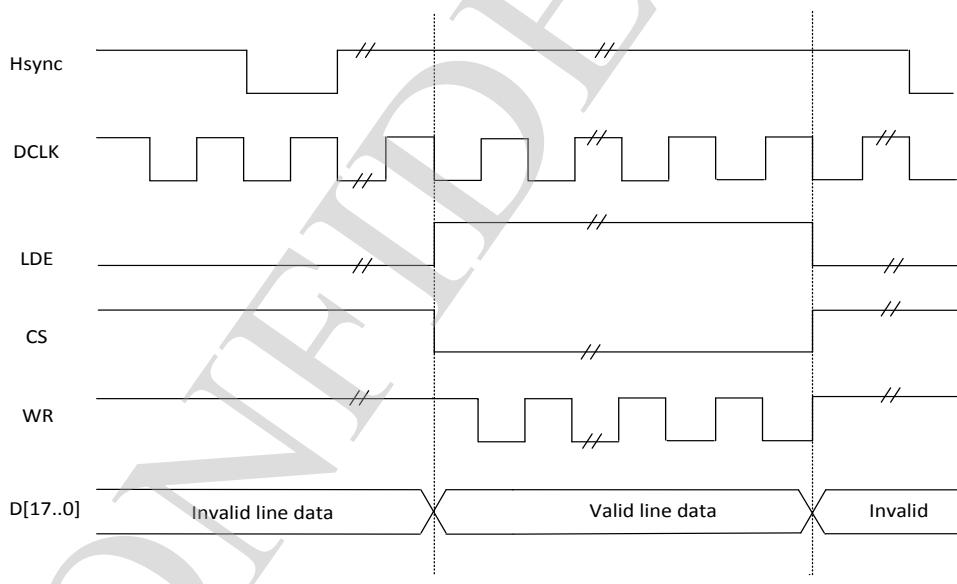
CPU_I/F

CPU I/F LCD panel is the most commonly used interface for small size, low resolution LCD panels.

CPU control signals are active low.

Main Signal	I/O Type	Description
CS	O	Chip select, active low
WR	O	Write strobe, active low
RD	O	Read strobe, active low
A1	O	Address bit, controlled by LCD_CPUI/F bit 21
D[17:0]	I/O	Digital RGB output signal

Following figure describes the relationship between basic timing and CPU timing. WR is 180 degree delay of DCLK; CS is active when pixel data are valid; RD is always set to 1; A1 are set by “**LCD_CPU I/F**”.

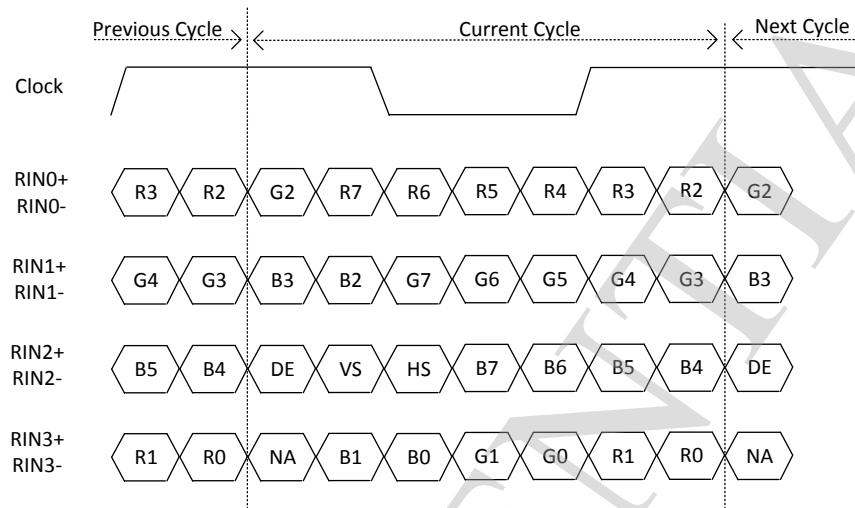


Relations between Basic Timing and CPU Timing

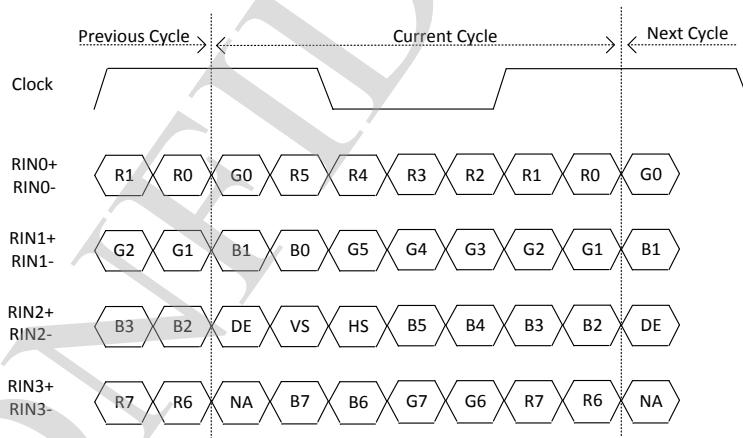
When CPU I/F is in IDLE state, it can generate WR/RD timing by setting “**LCD_CPUI/F**”. CS strobe is one DCLK width, WR/RD strobe is half DCLK width.

LVDS_IF

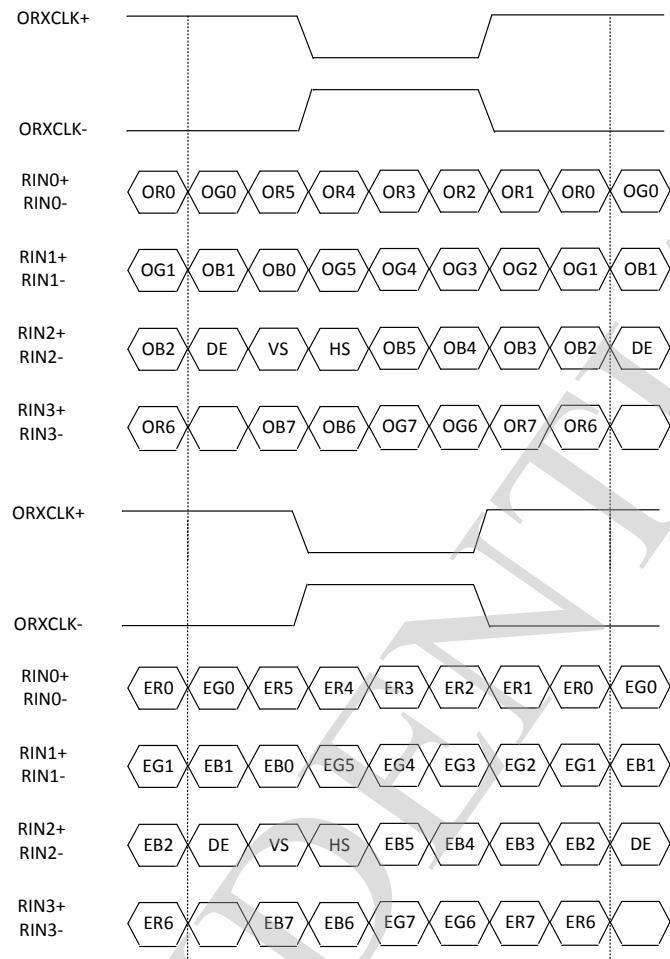
Single channel: JEDIA mode



Single channel: NS mode



Dual-channel: NS mode



Note: odd data is the first data

CMAP Module

This module is used to map color data from DE.

Every 4 input pixels as a unit and a unit is divided into 12 bytes. Output byte can select one of these 12 bytes.

Note that even line and odd line can be different, and output can be 12 bytes(4 pixels) or reduced to 6 bytes(2 pixels).

Input

r0(2)	r1(6)	r2(a)	r3(d)
g0(1)	g1(5)	g2(9)	g3(c)
b0(0)	b1(4)	b2(8)	b3(b)

Output

D23:16	odd0			
D15:08	odd0	odd1	odd2	odd3
D07:00	odd0			

In mode: 4 pixels
Out mode: 4 pixels/2 pixels

	eve0	eve1	eve2	eve3
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5.2.4 TCON Register List

Module Name	Base Address
TCON	0x01C0C000

Register Name	Offset	Description
TCON_GCTL_REG	0x000	TCON Global Control Register
TCON_GINT0_REG	0x004	TCON Global Interrupt Register0
TCON_GINT1_REG	0x008	TCON Global Interrupt Register1
TCON0_FRM_CTL_REG	0x010	TCON FRM Control Register
TCON0_CTL_REG	0x040	TCON0 Control Register
TCON0_DCLK_REG	0x044	TCON0 Data Clock Register
TCON0_BASIC0_REG	0x048	TCON0 Basic Timing Register0
TCON0_BASIC1_REG	0x04C	TCON0 Basic Timing Register1
TCON0_BASIC2_REG	0x050	TCON0 Basic Timing Register2
TCON0_BASIC3_REG	0x054	TCON0 Basic Timing Register3
TCON0_HV_IF_REG	0x058	TCON0 Hv Panel Interface Register
TCON0_CPU_IF_REG	0x060	TCON0 CPU Panel Interface Register
TCON0_CPU_WR_REG	0x064	TCON0 CPU Panel Write Data Register
TCON0_CPU_RDO_REG	0x068	TCON0 CPU Panel Read Data Register0
TCON0_CPU_RD1_REG	0x06C	TCON0 CPU Panel Read Data Register1
TCON0_LVDS_IF_REG	0x084	TCON0 LVDS Panel Interface Register
TCON0_IO_POL_REG	0x088	TCON0 IO Polarity Register
TCON0_IO_TRI_REG	0x08C	TCON0 IO Control Register
TCON_ECC_FIFO_REG	0x0F8	TCON ECC FIFO Register
/	0x0FC	/
TCON_CEU_CTL_REG	0x100	TCON CEU Control Register

TCON_CEU_COEF_MUL_REG	0x110+N*0x04	TCON CEU Coefficient Register0 (N=0,1,2,4,5,6,8,9,10)
TCON_CEU_COEF_ADD_REG	0x11C+N*0x10	TCON CEU Coefficient Register1 (N=0,1,2)
TCON_CEU_COEF_RANG_REG	0x140+N*0x04	TCON CEU Coefficient Register2 (N=0,1,2)
TCON0_CPU_TRI0_REG	0x160	TCON0 CPU Panel Trigger Register0
TCON0_CPU_TRI1_REG	0x164	TCON0 CPU Panel Trigger Register1
TCON0_CPU_TRI2_REG	0x168	TCON0 CPU Panel Trigger Register2
TCON0_CPU_TRI3_REG	0x16C	TCON0 CPU Panel Trigger Register3
TCON_CMAP_CTL_REG	0x180	TCON Color Map Control Register
TCON_CMAP_ODD0_REG	0x190	TCON Color Map Odd Line Register0
TCON_CMAP_ODD1_REG	0x194	TCON Color Map Odd Line Register1
TCON_CMAP_EVEN0_REG	0x198	TCON Color Map Even Line Register0
TCON_CMAP_EVEN1_REG	0x19C	TCON Color Map Even Line Register1
TCON_SAFE_PERIOD_REG	0x1F0	TCON Safe Period Register
TCON_MUX_CTL_REG	0x200	TCON MUX Control Register
TCON0_LVDS_ANA0_REG	0x220	TCON LVDS Analog Register0
TCON0_LVDS_ANA1_REG	0x224	TCON LVDS Analog Register1
TCON1_FILL_CTL_REG	0x300	TCON1 Fill Data Control Register
TCON1_FILL_BEGIN_REG	0x304+N*0x0C	TCON1 Fill Data Begin Register (N=0,1,2)
TCON1_FILL_END_REG	0x308+N*0x0C	TCON1 Fill Data End Register (N=0,1,2)
TCON1_FILL_DATA0_REG	0x30C+N*0x0C	TCON1 Fill Data Value Register (N=0,1,2)
/	0xFF0	
/	0xFF8	

/	0xFFC	
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5.2.5 TCON Register Description

TCON_GCTL_REG

Offset: 0x000			Register Name: TCON_GCTL_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	<p>TCON_En</p> <p>0: disable</p> <p>1: enable</p> <p>When it's disabled, the module will be reset to idle state.</p>
30	R/W	0	<p>TCON_Gamma_En</p> <p>0: disable</p> <p>1: enable</p>
29: 1	/	/	/
0	R/W	0	<p>IO_Map_Sel</p> <p>0: TCON0</p> <p>1: TCON1</p> <p>Note: this bit determined which IO_INV/IO_TRI are valid</p>

TCON_GINT0_REG

Offset: 0x004			Register Name: TCON_GINT0_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	<p>TCON0_Vb_Int_En</p> <p>0: disable</p> <p>1: enable</p>
30	R/W	0	<p>TCON1_Vb_Int_En</p> <p>0: disable</p>

			1: enable
29	R/W	0	TCON0_Line_Int_En 0: disable 1: enable
28	R/W	0	TCON1_Line_Int_En 0: disable 1: enable
27	R/W	0	TCON0_Tri_Finish_Int_En 0: disable 1: enable
26:	R/W	0	TCON0_Tri_Counter_Int_En 0: disable 1: enable
25:1 6	/	/	/
15	R/W	0	TCON0_Vb_Int_Flag Asserted during vertical no-display period every frame. Write 0 to clear it.
14	R/W	0	TCON1_Vb_Int_Flag Asserted during vertical no-display period every frame. Write 0 to clear it.
13	R/W	0	TCON0_Line_Int_Flag trigger when SY0 match the current TCON0 scan line Write 0 to clear it.
12	R/W	0	TCON1_Line_Int_Flag trigger when SY1 match the current TCON1 scan line Write 0 to clear it.
11	R/W	0	TCON0_Tri_Finish_Int_Flag trigger when CPU trigger mode finish

			Write 0 to clear it.
10	R/W	0	TCON0_Tri_Counter_Int_Flag trigger when tri counter reaches this value Write 0 to clear it.
9	R/W	0	TCON0_Tri_Underflow_Flag only used in dsi video mode, tri when sync by dsi but not finish Write 0 to clear it.
8:0	/	/	/

TCON_GINT1_REG

Offset: 0x008			Register Name: TCON_GINT1_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 8	/	/	/
27:1 6	R/W	0	TCON0_Line_Int_Num scan line for TCON0 line trigger(including inactive lines) Setting it for the specified line for trigger0. Note: SY0 is writable only when LINE_TRG0 disable.
15:1 2	/	/	/
11:0	R/W	0	TCON1_Line_Int_Num scan line for TCON1 line trigger(including inactive lines) Setting it for the specified line for trigger 1. Note: SY1 is writable only when LINE_TRG1 disable.

TCON0_FRM_CTL_REG

Offset: 0x010			Register Name: TCON0_FRM_CTL_REG
Bit	Read/Writ e	Default/H ex	Description

31	R/W	0	TCON0_Frm_En 0:disable 1:enable
30: 7	/	/	/
6	R/W	0	TCON0_Frm_Mode_R 0: 6bit frm output 1: 5bit frm output
5	R/W	0	TCON0_Frm_Mode_G 0: 6bit frm output 1: 5bit frm output
4	R/W	0	TCON0_Frm_Mode_B 0: 6bit frm output 1: 5bit frm output
3:2	/	/	/
1:0	R/W	0	TCON0_Frm_Test 00: FRM 01: half 5/6bit, half FRM 10: half 8bit, half FRM 11: half 8bit, half 5/6bit

TCON0_CTL_REG

Offset: 0x040		Register Name: TCON0_CTL_REG	
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	TCON0_En 0: disable 1: enable Note: It executes at the beginning of the first blank line of TCON0 timing.

30:2 9	/	/	/
28	R/W	0	TCON0_Work_Mode 0: normal 1: dynamic freq
27:2 6	/	/	/
25:2 4	R/W	0	TCON0_IF 00: HV(Sync+DE) 01: 8080 I/F 1x:reserved
23	R/W	0	TCON0_RB_Swap 0: default 1: swap RED and BLUE data at FIFO1
22	/	/	/
21	R/W	0	TCON0_FIFO1_Rst Write 1 and then 0 at this bit will reset FIFO 1 Note: 1 holding time must more than 1 DCLK
20:9	/	/	/
8:4	R/W	0	TCON0_Start_Delay STA delay NOTE: valid only when TCON0_EN == 1
3	/	/	/
2:0	R/W	0	TCON0_SRC_SEL: 000: DE0 001: reserved 010: DMA RGBA888 input(FIFO1 enable) 011: DMA RGB565 input(FIFO1 enable) 100: Test Data all 0 101: Test Data all 1

			<p>11x: reserved</p> <p>when set as DMA RGBA888 input DMA Des Bus Width should be configured as “32bit”</p> <p>when set as DMA RGB565 input DMA Des Bus Width should be configured as “16bit”</p>
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TCON0_DCLK REG

Offset: 0x044			Register Name: TCON0_DCLK REG
Bit	Read/Writ e	Default/ Hex	Description
31:28	R/W	0	<p>TCON0_Dclk_En</p> <p>LCLK_EN[3:0] :TCON0 clock enable</p> <p>4'h0, 'h4,4'h6,4'ha7:dclk_en=0;dclk1_en=0;dclk2_en=0;dclkm2_en=0;</p> <p>4'h1: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 0;</p> <p>4'h2: dclk_en = 1; dclk1_en = 0; dclk2_en = 0; dclkm2_en = 1;</p> <p>4'h3: dclk_en = 1; dclk1_en = 1; dclk2_en = 0; dclkm2_en = 0;</p> <p>4'h5: dclk_en = 1; dclk1_en = 0; dclk2_en = 1; dclkm2_en = 0;</p> <p>4'h8,4'h9,4'ha,4'hb,4'hc,4'hd,4'he,4'hf:</p> <p style="padding-left: 40px;">dclk_en = 1;</p> <p style="padding-left: 40px;">dclk1_en = 1;</p> <p style="padding-left: 40px;">dclk2_en = 1;</p> <p style="padding-left: 40px;">dclkm2_en = 1;</p>
27:7	/	/	/
6:0	R/W	0	<p>TCON0_Dclk_Div</p> <p>Tdclk = Tsclk * DCLKDIV</p> <p>Note:</p> <p>1.if dclk1&dclk2 used, DCLKDIV >=6</p> <p>2.if dclk only, DCLKDIV >=1</p>

TCON0_BASIC0_REG

Offset: 0x048			Register Name: TCON0_BASIC0_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 8	/	/	/
27:1 6	R/W	0	TCON0_X Panel width is X+1
15:1 2	/	/	/
11:0	R/W	0	TCON0_Y Panel height is Y+1

TCON0_BASIC1_REG

Offset: 0x04C			Register Name: TCON0_BASIC1_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	Reserved
30:2 9	/	/	/
28:1 6	R/W	0	HT Thcycle = (HT+1) * Tdclk Computation 1) parallel: HT = X + BLANK Limitation: 1) parallel : HT >= (HBP +1) + (X+1) +2 2) serial 1: HT >= (HBP +1) + (X+1) *3+2 3) serial 2: HT >= (HBP +1) + (X+1) *3/2+2
15:1 2	/	/	/
11:0	R/W	0	HBP

			horizontal back porch (in dclk) $\text{Thbp} = (\text{HBP} + 1) * \text{Tdclk}$
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TCON0_BASIC2_REG

Offset: 0x050			Register Name: TCON0_BASIC2_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28:1 6	R/W	0	VT $\text{TVT} = (\text{VT})/2 * \text{Thsync}$ Note: $\text{VT}/2 \geq (\text{VBP}+1) + (\text{Y}+1) + 2$
15:1 2	/	/	/
11:0	R/W	0	VBP $\text{Tvbp} = (\text{VBP} + 1) * \text{Thsync}$

TCON0_BASIC3_REG

Offset: 0x054			Register Name: TCON0_BASIC3_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 6	/	/	/
25:1 6	R/W	0	HSPW $\text{Thspw} = (\text{HSPW}+1) * \text{Tdclk}$ Note: $\text{HT} > (\text{HSPW}+1)$
15:1 0	/	/	/
9:0	R/W	0	VSPW $\text{Tvspw} = (\text{VSPW}+1) * \text{Thsync}$ Note: $\text{VT}/2 > (\text{VSPW}+1)$

TCON0_HV_IF_REG

Offset: 0x058			Register Name: TCON0_HV_IF_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 8	R/W	0	<p>HV_Mode</p> <p>0000: 24bit/1cycle parallel mode</p> <p>1000: 8bit/3cycle RGB serial mode(RGB888)</p> <p>1010: 8bit/4cycle Dummy RGB(DRGB)</p> <p>1011: 8bit/4cycle RGB Dummy(RGBD)</p> <p>1100: 8bit/2cycle YUV serial mode(CCIR656)</p>
27:2 6	R/W	0	<p>RGB888_SM0</p> <p>serial RGB888 mode Output sequence at odd lines of the panel (line 1, 3, 5, 7...)</p> <p>00: R→G→B</p> <p>01: B→R→G</p> <p>10: G→B→R</p> <p>11: R→G→B</p>
25:2 4	R/W	0	<p>RGB888_SM1</p> <p>serial RGB888 mode Output sequence at even lines of the panel (line 2, 4, 6, 8...)</p> <p>00: R→G→B</p> <p>01: B→R→G</p> <p>10: G→B→R</p> <p>11: R→G→B</p>
23:2 2	R/W	0	<p>YUV_SM</p> <p>serial YUV mode Output sequence 2-pixel-pair of every scan line</p> <p>00: YUYV</p> <p>01: YVYU</p>

			10: UYVY 11: VYUY
21:2 0	R/W	0	YUV EAV/SAV F line delay 0:F toggle right after active video line 1:delay 2 line(CCIR NTSC) 2:delay 3 line(CCIR PAL) 3:reserved
19:0	/	/	/

TCON0_CPU_IF_REG

Offset: 0x060			Register Name: TCON0_CPU_IF_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 8	R/W	0	CPU_Mode 0000: 18bit/256K mode 0010: 16bit mode0 0100: 16bit mode1 0110: 16bit mode2 1000: 16bit mode3 1010: 9bit mode 1100: 8bit 256K mode 1110: 8bit 65K mode xxx1: 24bit for DSI
27	/	/	/
26	R/W	0	DA pin A1 value in 8080 mode auto/flash states
25	R/W	0	CA pin A1 value in 8080 mode WR/RD execute
24	/	/	/

23	R	0	Wr_Flag 0:write operation is finishing 1:write operation is pending
22	R	0	Rd_Flag 0:read operation is finishing 1:read operation is pending
21:1 8	/	/	/
17	R/W	0	AUTO auto Transfer Mode: If it's 1, all the valid data during this frame are write to panel. Note: This bit is sampled by Vsync
16	R/W	0	FLUSH direct transfer mode: If it's enabled, FIFO1 is regardless of the HV timing, pixels data keep being transferred unless the input FIFO was empty. Data output rate control by DCLK.
15:6	/	/	/
5:4	R/W	0	Trigger_Sync_Mode 0: start frame flush immediately by bit1. 1: start frame flush sync to TE PIN. rising by bit1. 2. start frame flush sync to TE PIN. falling by bit1. when set as 1 or 2, io0 is map as TE input.
3	R/W	0	Trigger_FIFO_Bist_En 0: disable 1: enable Entry addr is 0xFF8
2	R/W	0	Trigger_FIFO_En 0:enable 1:disable

1	R/W	0	Trigger_Start write '1' to start a frame flush, write'0' has no effect. this flag indicated frame flush is running software must make sure write '1' only when this flag is '0'.
0	R/W	0	Trigger_En 0: trigger mode disable 1: trigger mode enable

TCON0_CPU_WR_REG

Offset: 0x064			Register Name: TCON0_CPU_WR_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:0	W	0	Data_Wr data write on 8080 bus, launch a write operation on 8080 bus

TCON0_CPU_RD0_REG

Offset: 0x068			Register Name: TCON0_CPU_RD0_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:0	R	/	Data_Rd0 data read on 8080 bus, launch a new read operation on 8080 bus

TCON0_CPU_RD1_REG

Offset: 0x06C			Register Name: TCON0_CPU_RD1_REG
Bit	Read/Writ e	Default/H ex	Description

31:2 4	/	/	/
23:0	R	/	Data_Rd1 data read on 8080 bus, without a new read operation on 8080 bus

TCON0_LVDS_IF_REG

Offset: 0x084			Register Name: TCON0_LVDS_IF_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	TCON0_LVDS_En 0: disable 1: enable
30	R/W	0	TCON0_LVDS_Link_Sel 0: single link 1: dual link
29	R/W	0	TCON0_LVDS_Even_Odd_Dir 0: normal 1: reverse
28	R/W	0	TCON0_LVDS_Dir 1: normal 2: reverse NOTE: LVDS direction
27	R/W	0	TCON0_LVDS_Mode 0: NS mode 1: JEIDA mode
26	R/W	0	TCON0_LVDS_BitWidth 0: 24bit 1: 18bit
25:2	R/W	0	/

4			
23	R/W	0	TCON0_LVDS_Correct_Mode 0: mode0 1: mode1
22:2 1	/	/	/
20	R/W	0	TCON0_LVDS_Clk_Sel 0: MIPI PLL 1: TCON0 CLK
19:0	/	/	/

TCON0_IO_POL_REG

Offset: 0x088			Register Name: TCON0_IO_POL_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	IO_Output_Sel 0: normal output 1: register output when set as '1', d[23:0], io0, io1, io3 sync to dclk
30:2 8	R/W	0	DCLK_Sel 000: used DCLK0(normal phase offset) 001: used DCLK1(1/3 phase offset) 010: used DCLK2(2/3 phase offset) 101: DCLK0/2 phase 0 100: DCLK0/2 phase 90 reserved
27	R/W	0	IO3_Inv 0: not invert 1: invert

26	R/W	0	IO2_Inv 0: not invert 1: invert
25	R/W	0	IO1_Inv 0: not invert 1: invert
24	R/W	0	IO0_Inv 0: not invert 1: invert
23:0	R/W	0	Data_Inv TCON0 output port D[23:0] polarity control, with independent bit control: 0s: normal polarity 1s: invert the specify output

TCON0_IO_TRI_REG

Offset: 0x08C			Register Name: TCON0_IO_TRI_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28	/	/	RGB_Endian 0: normal 1: bits_invert
27	R/W	1	IO3_Output_Tri_En 1: disable 0: enable
26	R/W	1	IO2_Output_Tri_En 1: disable 0: enable

25	R/W	1	IO1_Output_Tri_En 1: disable 0: enable
24	R/W	1	IO0_Output_Tri_En 1: disable 0: enable
23:0	R/W	0xFFFFF	Data_Output_Tri_En TCON0 output port D[23:0] output enable, with independent bit control: 1s: disable 0s: enable

TCON_ECC_FIFO_REG

Offset: 0x0F8			Register Name: TCON_ECC_FIFO_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	/	ECC_FIFO_BIST_EN 0: disable 1: enable
30	R/W	/	ECC_FIFO_ERR_FLAG
29:2 4	/	/	/
23:1 6	R/W	/	ECC_FIFO_ERR_BITS
15:9	/	/	/
8	R/W	/	ECC_FIFO_BLANK_EN 0: disable ecc function in blanking 1: enable ecc function in blanking ECC function is tent to triggered in blanking area at hv mode, set '0' when in hv mode

7:0	R/W	/	ECC_FIFO_SETTING Note: bit3 0 enable, 1 disable
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TCON_CEU_CTL_REG

Offset: 0x100			Register Name: TCON_CEU_CTL_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	CEU_en 0: bypass 1: enable
30: 0	/	/	/

TCON_CEU_COEF_MUL_REG

Offset: 0x110+N*0x04 (N=0,1,2,4,5,6,8,9,10)			Register Name: TCON_CEU_COEF_MUL_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0	CEU_Coef_Mul_Value signed 13bit value, range of (-16,16) N=0: Rr N=1: Rg N=2: Rb N=4: Gr N=5: Gg N=6: Gb N=8: Br N=9: Bg

			N=10: Bb
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TCON_CEU_COEF_ADD_REG

Offset: 0x11C+N*0x10 (N=0,1,2)			Register Name: TCON_CEU_COEF_ADD_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 9	/	/	/
18:0	R/W	0	CEU_Coef_Add_Value signed 19bit value, range of (-16384, 16384) N=0: Rc N=1: Gc N=2: Bc

TCON_CEU_COEF_RANG_REG

Offset: 0x140+N*0x04 (N=0,1,2)			Register Name: TCON_CEU_COEF_RANG_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:1 6	R/W	0	CEU_Coef_Range_Min unsigned 8bit value, range of [0,255]
15:8	/	/	/
7:0	R/W	0	CEU_Coef_Range_Max unsigned 8bit value, range of [0,255]

TCON0_CPU_TRI0_REG

Offset: 0x160			Register Name: TCON0_CPU_TRI0_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 8	/	/	/
27:1 6	R/W	0	Block_Space should be set >20*pixel_cycle
15:1 2	/	/	/
11:0	R/W	0	Block_Size

TCON0_CPU_TRI1_REG

Offset: 0x164			Register Name: TCON0_CPU_TRI1_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R	0	Block_Current_Num
15:0	R/W	0	Block_Num

TCON0_CPU_TRI2_REG

Offset: 0x168			Register Name: TCON0_CPU_TRI2_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R/W	0x20	Start_Delay Tdly = (Start_Delay +1) * be_clk*8
15	R/W	0	Trans_Start_Mode 0: ecc_FIFO+tri_FIFO

			1: tri_FIFO
14:1 3	R/W	0	Sync_Mode 0x: auto 10: 0 11: 1
12:0	R/W	0	Trans_Start_Set

TCON0_CPU_TRI3_REG

Offset: 0x16C			Register Name: TCON0_CPU_TRI3_REG
Bit	Read/Writ e	Default/H ex	Description
31:3 0	/	/	/
29:2 8	R/W	0	Tri_Int_Mode 00: disable 01: counter mode 10: te rising mode 11: te falling mode when set as 01, Tri_Counter_Int occur in cycle of (Count_N+1)×(Count_M+1)×4 dclk. when set as 10 or 11, io0 is map as TE input.
27:2 4	/	/	/
23:8	R/W	0	Counter_N
7:0	R/W	0	Counter_M

TCON_CMAP_CTL_REG

Offset: 0x180	Register Name: TCON_CMAP_CTL_REG
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Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	<p>Color_Map_En</p> <p>0: bypass</p> <p>1: enable</p> <p>This module only work when X is divided by 4</p>
30: 1	/	/	/
0	R/W	0	<p>Out_Format</p> <p>0: 4 pixel output mode: Out0 -> Out1 -> Out2 -> Out3</p> <p>1: 2 pixel output mode: Out0 -> Out1</p>

TCON_CMAP_ODD0_REG

Offset: 0x190			Register Name: TCON_CMAP_ODD0_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R/W	0	Out_Odd1
15:0	R/W	0	<p>Out_Odd0</p> <p>bit15-12: Reserved</p> <p>bit11-08: Out_Odd0[23:16]</p> <p>bit07-04: Out_Odd0[15:8]</p> <p>bit03-00: Out_Odd0[7:0]</p> <p>0x0: in_b0</p> <p>0x1: in_g0</p> <p>0x2: in_r0</p> <p>0x3: reserved</p> <p>0x4: in_b1</p> <p>0x5: in_g1</p> <p>0x6: in_r1</p>

			0x7: reservd 0x8: in_b2 0x9: in_g2 0xa: in_r2 0xb: reserved 0xc: in_b3 0xd: in_g3 0xe: in_r3 0xf: reserved
--	--	--	--

TCON_CMAP_ODD1_REG

Offset: 0x194			Register Name: TCON_CMAP_ODD1_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R/W	0	Out_Odd3
15:0	R/W	0	Out_Odd2

TCON_CMAP_EVEN0_REG

Offset: 0x198			Register Name: TCON_CMAP_EVEN0_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R/W	0	Out_Even1
15:0	R/W	0	Out_Even0

TCON_CMAP_EVEN1_REG

Offset: 0x19C			Register Name: TCON_CMAP_EVEN1_REG
Bit	Read/Writ e	Default/H ex	Description

31:1 6	R/W	0	Out_Even3
15:0	R/W	0	Out_Even2

TCON_SAFE_PERIOD_REG

Offset: 0x1F0			Register Name: TCON_SAFE_PERIOD_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28:1 6	R/W	0	Safe_Period_FIFO_Num
15:2	/	/	/
1:0	R/W	0	Safe_Period_Mode 0: unsafe 1: safe 2: safe at ecc_FIFO_curr_num > safe_period_FIFO_num 3: safe at 2 and safe at sync active

TCON_MUX_CTL_REG

Offset: 0x200			Register Name: TCON_MUX_CTL_REG
Bit	Read/Writ e	Default/H ex	Description
31:2	/	/	/
1:0	R/W	0	MIPI_DSI_OUTPUT_SRC 00: LCDCO TCON0 01: LCDC1 TCON0 1x: close(clock gate)

TCON0_LVDS_ANA0_REG

Offset: 0x220			Register Name: TCON0_LVDS_ANA0_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	lvds0_en_mb enable the bias circuit of the LVDS_Ana module
30	R/W	0	lvds0_en_ldo
29:25	/	/	/
24	R/W	0	lvds0_en_drvc enable all circuits working when transmitting the data in channel clock of LVDS_tx0
23:20	R/W	0	lvds0_en_drv enable all circuits working when transmitting the data in channel<3:0> of LVDS_tx0
19	/	/	/
18:17	R/W	0	lvds0_reg_c adjust current flowing through Rload of Rx to change the differential signals amplitude 0:250mV 1:300mV 2:350mV 3:400mV
16	R/W	0	lvds0_reg_denc choose data output or PLL test clock output in LVDS_tx
15:12	R/W	0	lvds0_reg_den choose data output or PLL test clock output in LVDS_tx
11:10	/	/	/
9:8	R/W	0	lvds0_reg_v adjust common mode voltage of the differential signals in five

			channels
7:6	/	/	/
5:4	R/W	0	lvds0_reg_pd fine adjust the slew rate of output data
3:2	/	/	/
1	R/W	0	lvds0_reg_pwslv adjust voltage amplitude of low power in LVDS_Ana
0	R/W	0	lvds0_reg_pwsmb adjust voltage amplitude of mbias voltage reference in LVDS_Ana

TCON0_LVDS_ANA1_REG

Offset: 0x224			Register Name: TCON0_LVDS_ANA1_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	lvds1_en_mb
30	R/W	0	lvds1_en_ldo
29:25	/	/	/
24	R/W	0	lvds1_en_drvc
23:20	R/W	0	lvds1_en_drv
19	/	/	/
18:17	R/W	0	lvds1_reg_c
16	R/W	0	lvds1_reg_denc
15:12	R/W	0	lvds1_reg_den
11:10	/	/	/
9:8	R/W	0	lvds1_reg_v

7:6	/	/	/
5:4	R/W	0	lvds1_reg_pd
3:2	/	/	/
1	R/W	0	lvds1_reg_pwslv
0	R/W	0	lvds1_reg_pwsmb

TCON1_FILL_CTL_REG

Offset: 0x300			Register Name: TCON1_FILL_CTL_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	TCON1_Fill_En 0: bypass 1: enable
30:0	/	/	/

TCON1_FILL_BEGIN_REG

Offset: 0x304+N*0x0C (N=0,1,2)			Register Name: TCON1_FILL_BEGIN_REG
Bit	Read/Writ e	Default/H ex	Description
31:24	/	/	/
23:0	R/W	0	Fill_Begin

TCON1_FILL_END_REG

Offset: 0x308+N*0x0C (N=0,1,2)			Register Name: TCON1_FILL_END_REG
Bit	Read/Writ e	Default/H ex	Description

31:2 4	/	/	/
23:0	R/W	0	Fill_End

TCON1_FILL_DATA_REG

Offset: 0x30C+N*0x0C (N=0,1,2)			Register Name: TCON1_FILL_DATA_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:0	R/W	0	Fill_Value

5.2.6 Control Signal and Data Port Mapping

PD	I/F	Sync RGB					CPU/I80 Interface					LVDS Interface	
		Para RGB	Serial RGB			CCIR 656	Para RGB 666	Para RGB 565	Serial RGB 666	Serial RGB 565	Sing Link		
	Cycle		1st	2nd	3rd				1st	2nd	1st	2nd	
PD27	IO0	VSYNC					CS					D3N	
PD26	IO1	HSYNC					RD					D3P	
PD25	IO3	DE					RS					CKN	
PD24	IO2	DCLK					WR					CKP	
PD23	D23	R5					R5	R4				D2N	
PD22	D22	R4					R4	R3				D2P	
PD21	D21	R3					R3	R2				D1N	
PD20	D20	R2					R2	R1				D1P	
PD19	D19	R1					R1	R0				D0N	
PD18	D18	R0					R0	G5				D0P	
PD15	D15	G5					G5	G4					
PD14	D14	G4					G4	G3					
PD13	D13	G3					G3						
PD12	D12	G2	D17	D27	D37	D7	G2	G2	R5	G2	R4	G2	
PD11	D11	G1	D16	D26	D36	D6	G1	G1	R4	G1	R3	G1	
PD10	D10	G0	D15	D25	D35	D5	G0	G0	R3	G0	R2	G0	
PD7	D7	B5	D14	D24	D34	D4	B5	B4	R2	B5	R1	B4	
PD6	D6	B4	D13	D23	D33	D3	B4	B3	R1	B4	R0	B3	
PD5	D5	B3	D12	D22	D32	D2	B3	B2	R0	B3	G5	B2	
PD4	D4	B2	D11	D21	D31	D1	B2	B1	G5	B2	G4	B1	
PD3	D3	B1	D10	D20	D30	D0	B1	B0	G4	B1	G3	B0	

PD2	D2	B0				B0		G3	B0			
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5.3 Display Engine Front-End

5.3.1 Overview

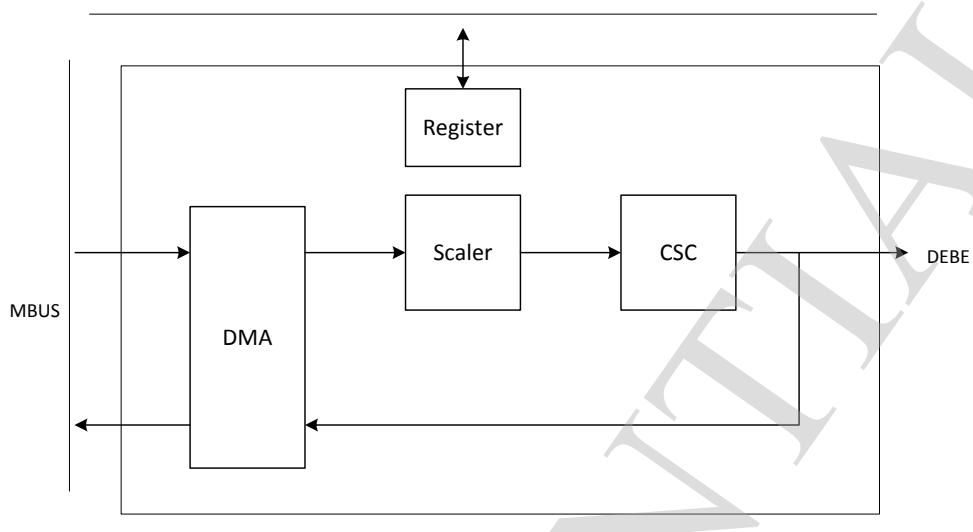
The display engine front-end (DEFE) provides image resizing function for display engine. It receives data from memory bus, performs the image resizing function, and outputs to display engine back-end or memory.

The DEFE can receive most of YUV and RGB data formats, and then converts to RGB888 for display. It also can function as a format converter through the memory-to-memory path. Horizontal and vertical direction scaling are implemented independently.

The DEFE features:

- Supported input format: YUV444/YUV420/YUV422/YUV411/ARGB8888
- Support Planar/Interleaved/non-tile-based UV combined/tile-based UV combined
- Support input and output size from 8x4 to 8192x8192
- Support 32-phase 4-tap horizontal and vertical anti-alias filter with coefficient programmable
- Support point-to-point display size up to 1366 pixel/line

5.3.2 DEFE Block Diagram



DEFE Block Diagram

5.3.3 DEFE Register List

Module Name	Base Address
DEFE	0x01e00000

Register Name	Offset	Description
DEFE_EN_REG	0x0000	DEFE Module Enable Register
DEFE_FRM_CTRL_REG	0x0004	DEFE Frame Process Control Register
DEFE_BYPASS_REG	0x0008	DEFE CSC By-Pass Register
DEFE_AGTH_SEL_REG	0x000C	DEFE Algorithm Selection Register
DEFE_LINT_CTRL_REG	0x0010	DEFE Line Interrupt Control Register
DEFE_BUF_ADDR0_REG	0x0020	DEFE Input Channel 0 Buffer Address Register
DEFE_BUF_ADDR1_REG	0x0024	DEFE Input Channel 1 Buffer Address Register
DEFE_BUF_ADDR2_REG	0x0028	DEFE Input Channel 2 Buffer Address Register
DEFE_FIELD_CTRL_REG	0x002C	DEFE Field Sequence Register
DEFE_TB_OFF0_REG	0x0030	DEFE Channel 0 Tile-Based Offset Register
DEFE_TB_OFF1_REG	0x0034	DEFE Channel 1 Tile-Based Offset Register
DEFE_TB_OFF2_REG	0x0038	DEFE Channel 2 Tile-Based Offset Register
DEFE_LINESTRD0_REG	0x0040	DEFE Channel 0 Line Stride Register
DEFE_LINESTRD1_REG	0x0044	DEFE Channel 1 Line Stride Register
DEFE_LINESTRD2_REG	0x0048	DEFE Channel 2 Line Stride Register
DEFE_INPUT_FMT_REG	0x004C	DEFE Input Format Register
DEFE_WB_ADDR_REG	0x0050	DEFE Write Back Address Register
DEFE_OUTPUT_FMT_REG	0x005C	DEFE Output Format Register
DEFE_INT_EN_REG	0x0060	DEFE Interrupt Enable Register
DEFE_INT_STATUS_REG	0x0064	DEFE Interrupt Status Register
DEFE_STATUS_REG	0x0068	DEFE Status Register
DEFE_CSC_COEF00_REG	0x0070	DEFE CSC Coefficient 00 Register

DEFE_CSC_COEF01_REG	0x0074	DEFE CSC Coefficient 01 Register
DEFE_CSC_COEF02_REG	0x0078	DEFE CSC Coefficient 02 Register
DEFE_CSC_COEF03_REG	0x007C	DEFE CSC Coefficient 03 Register
DEFE_CSC_COEF10_REG	0x0080	DEFE CSC Coefficient 10 Register
DEFE_CSC_COEF11_REG	0x0084	DEFE CSC Coefficient 11 Register
DEFE_CSC_COEF12_REG	0x0088	DEFE CSC Coefficient 12 Register
DEFE_CSC_COEF13_REG	0x008C	DEFE CSC Coefficient 13 Register
DEFE_CSC_COEF20_REG	0x0090	DEFE CSC Coefficient 20 Register
DEFE_CSC_COEF21_REG	0x0094	DEFE CSC Coefficient 21 Register
DEFE_CSC_COEF22_REG	0x0098	DEFE CSC Coefficient 22 Register
DEFE_CSC_COEF23_REG	0x009C	DEFE CSC Coefficient 23 Register
DEFE_WB_LINESTRD_EN_REG	0x00D0	DEFE Write Back Line Stride Enable Register
DEFE_WB_LINESTRD_REG	0x00D4	DEFE Write Back Channel 3 Line Stride Register
DEFE_CH0_INSIZE_REG	0x0100	DEFE Channel 0 Input Size Register
DEFE_CH0_OUTSIZE_REG	0x0104	DEFE Channel 0 Output Size Register
DEFE_CH0_HORZFACT_REG	0x0108	DEFE Channel 0 Horizontal Factor Register
DEFE_CH0_VERTFACT_REG	0x010C	DEFE Channel 0 Vertical Factor Register
DEFE_CH0_HORZPHASE_REG	0x0110	DEFE Channel 0 Horizontal Initial Phase Register
DEFE_CH0_VERTPHASE0_REG	0x0114	DEFE Channel 0 Vertical Initial Phase 0 Register
DEFE_CH0_VERTPHASE1_REG	0x0118	DEFE Channel 0 Vertical Initial Phase 1 Register
DEFE_CH0_HORZTAP_REG	0x0120	DEFE Channel 0 Horizontal Tap Offset Register
DEFE_CH0_VERTTAP_REG	0x0128	DEFE Channel 0 Vertical Tap Offset Register
DEFE_CH1_INSIZE_REG	0x0200	DEFE Channel 1 Input Size Register
DEFE_CH1_OUTSIZE_REG	0x0204	DEFE Channel 1 Output Size Register
DEFE_CH1_HORZFACT_REG	0x0208	DEFE Channel 1 Horizontal Factor Register
DEFE_CH1_VERTFACT_REG	0x020C	DEFE Channel 1 Vertical Factor Register
DEFE_CH1_HORZPHASE_REG	0x0210	DEFE Channel 1 Horizontal Initial Phase Register
DEFE_CH1_VERTPHASE0_REG	0x0214	DEFE Channel 1 Vertical Initial Phase 0 Register

DEFE_CH1_VERTPHASE1_REG	0x0218	DEFE Channel 1 Vertical Initial Phase 1 Register
DEFE_CH1_HORZTAP_REG	0x0220	DEFE Channel 1 Horizontal Tap Offset Register
DEFE_CH1_VERTTAP_REG	0x0228	DEFE Channel 1 Vertical Tap Offset Register
DEFE_CH0_HORZCOEF_REGN	0x0400+N*4	DEFE Channel 0 Horizontal Filter Coefficient Register N=0:31
DEFE_CH0_VERTCOEF_REGN	0x0500+N*4	DEFE Channel 0 Vertical Filter Coefficient Register N=0:31
DEFE_CH1_HORZCOEF_REGN	0x0600+N*4	DEFE Channel 1 Horizontal Filter Coefficient Register N=0:31
DEFE_CH1_VERTCOEF_REGN	0x0700+N*4	DEFE Channel 1 Vertical Filter Coefficient Register N=0:31

5.3.4 DEFE Register Description

DEFE_EN_REG

Offset: 0x0			Register Name: DEFE_EN_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0x0	<p>EN</p> <p>DEFE enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>When DEFE enable bit is disabled, the clock of DEFE module will be disabled</p> <p>If this bit is transition from 0 to 1, the frame process control register and the interrupt enable register will be initiated to default value, and the state machine of the module is reset</p>

DEFE_FRM_CTRL_REG

Offset: 0x4			Register Name: DEFE_FRM_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23	R/W	0x0	<p>COEF_ACCESS_CTRL</p> <p>Fir coef ram access control</p> <p>0: CPU doesn't access fir coef ram</p> <p>1: CPU will access fir coef ram</p> <p>This bit will be set to 1 before CPU access fir coef ram</p>
22:1 7	/	/	/

16	R/W	0x0	<p>FRM_START</p> <p>Frame start & reset control</p> <p>0: reset</p> <p>1: start</p> <p>If the bit is written to zero, the whole state machine and data paths of DEFE module will be reset.</p> <p>When the bit is written to 1, DEFE will start a new frame process.</p>
15:1 2	/	/	/
11	R/W	0x0	<p>OUT_CTRL</p> <p>DEFE output control</p> <p>0: enable DEFE output to DEBE</p> <p>1: disable DEFE output to DEBE</p> <p>If DEFE write back function is enabled, DEFE output to DEBE isn't recommended.</p>
10:3	/	/	/
2	R/W	0x0	<p>WB_EN</p> <p>Write back enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>If output to DEBE is enabled, the writing back process will start when write back enable bit is set and a new frame processing begins. The bit will be self-cleared when writing-back frame process starts.</p>
1	/	/	
0	R/W	0x0	<p>REG_RDY_EN</p> <p>Register ready enable</p>

			<p>0: not ready 1: registers configuration ready</p> <p>As same as filter coefficients configuration, in order to ensure the display is correct, the correlative display configuration registers are buffered too, the programmer also can change the value of correlative registers in any time. When the registers setting is finished, the programmer should set the bit if the programmer need the new configuration in next scaling frame.</p> <p>When the new frame start, the bit will also be self-cleared.</p>
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DEFE_BYPASS_REG

Offset: 0x8			Register Name: DEFE_BYPASS_REG
Bit	Read/Writ e	Default/H ex	Description
31: 2	/	/	/
1	R/W	0x0	<p>CSC_BYPASS_EN</p> <p>CSC by-pass enable</p> <p>0: CSC enable</p> <p>1: CSC will be by-passed</p> <p>Actually, in order ensure the module working be correct, This bit only can be set when input data format is the same as output data format (both YUV or both RGB)</p>
0	/	/	/

DEFE_AGTH_SEL_REG

Offset: 0xC			Register Name: DEFE_AGTH_SEL_REG
Bit	Read/Writ e	Default/H ex	Description
31:	/	/	/

9			
8	R/W	0x0	<p>LINEBUF_AGTH</p> <p>DEFE line buffer algorithm select</p> <p>0: horizontal filtered result</p> <p>1: original data</p>
7:0	/	/	/

DEFE_LINT_CTRL_REG

Offset: 0x10			Register Name: DEFE_LINT_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31:28	/	/	/
27:16	R	0x0	CURRENT_LINE
15	R/W	0x0	<p>FIELD_SEL</p> <p>Field select</p> <p>0: each field</p> <p>1: end field(field counter in reg0x2c)</p>
14:13	/	/	/
12:0	R/W	0x0	<p>TRIG_LINE</p> <p>Trigger line number of line interrupt</p>

DEFE_BUF_ADDRO_REG

Offset: 0x20			Register Name: DEFE_BUF_ADDRO_REG
Bit	Read/Writ e	Default/H ex	Description
31:0	R/W	0x0	<p>BUF_ADDR</p> <p>DEFE frame buffer address</p>

			<p>In tile-based type: The address is the start address of the line in the first tile used to generating output frame.</p> <p>In non-tile-based type: The address is the start address of the first line.</p>
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DEFE_BUF_ADDR1_REG

Offset: 0x24			Register Name: DEFE_BUF_ADDR1_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	<p>BUF_ADDR DEFE frame buffer address</p> <p>In tile-based type: The address is the start address of the line in the first tile used to generating output frame.</p> <p>In non-tile-based type: The address is the start address of the first line.</p>

DEFE_BUF_ADDR2_REG

Offset: 0x28			Register Name: DEFE_BUF_ADDR2_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	<p>BUF_ADDR DEFE frame buffer address</p> <p>In tile-based type: The address is the start address of the line in the first tile used</p>

			<p>to generating output frame.</p> <p>In non-tile-based type:</p> <p>The address is the start address of the first line.</p>
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DEFE_FIELD_CTRL_REG

Offset: 0x2C			Register Name: DEFE_FIELD_CTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31:3 0	/	/	/
29:2 4	R/W	0x20	FIR_OFFSET FIR compute initial value
23:1 3	/	/	/
12	R/W	0x0	FIELD_LOOP_MOD Field loop mode 0: the last field; 1: the full frame
11	/	/	/
10:8	R/W	0x0	VALID_FIELD_CNT Valid field counter bit the valid value = this value + 1;
7:0	R/W	0x0	FIELD_CNT Field counter each bit specify a field to display, 0: top field, 1: bottom field

DEFE_TB_OFF0_REG

Offset: 0x30			Register Name: DEFE_TB_OFF0_REG
Bit	Read/Writ e	Default/H ex	Description

31:2 1	/	/	/
20:1 6	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:1 3	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

DEFE_TB_OFF1_REG

Offset: 0x34			Register Name: DEFE_TB_OFF1_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 1	/	/	/
20:1 6	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:1 3	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

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DEFE_TB_OFF2_REG

Offset: 0x38			Register Name: DEFE_TB_OFF2_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 1	/	/	/
20:1 6	R/W	0x0	X_OFFSET1 The x offset of the bottom-right point in the end tile
15:1 3	/	/	/
12:8	R/W	0x0	Y_OFFSET0 The y offset of the top-left point in the first tile
7:5	/	/	/
4:0	R/W	0x0	X_OFFSET0 The x offset of the top-left point in the first tile

DEFE_LINESTRD0_REG

Offset: 0x40			Register Name: DEFE_LINESTRD0_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	LINE_STRIDE In tile-based type The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction) In non-tile-based type The stride length is the distance from the start of one line to the start of the next line.

DEFE_LINESTRD1_REG

Offset: 0x44			Register Name: DEFE_LINESTRD1_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	<p>LINE_STRIDE</p> <p>In tile-based type</p> <p>The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction)</p> <p>In non-tile-based type</p> <p>The stride length is the distance from the start of one line to the start of the next line.</p>

DEFE_LINESTRD2_REG

Offset: 0x48			Register Name: DEFE_LINESTRD2_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	<p>LINE_STRIDE</p> <p>In tile-based type</p> <p>The stride length is the distance from the start of the end line in one tile to the start of the first line in next tile(here next tile is in vertical direction)</p> <p>In non-tile-based type</p> <p>The stride length is the distance from the start of one line to the start of the next line.</p>

DEFE_INPUT_FMT_REG

Offset: 0x4C			Register Name: DEFE_INPUT_FMT_REG
Bit	Read/Writ	Default/H	Description

	e	ex	
31:1 7	/	/	/
16	R/W	0x0	<p>BYTE_SEQ</p> <p>Input data byte sequence selection</p> <p>0: P3P2P1P0(word)</p> <p>1: P0P1P2P3(word)</p>
15:1 3	/	/	/
12	R/W	0x0	<p>SCAN_MOD</p> <p>Scanning Mode selection</p> <p>0: non-interlace</p> <p>1: interlace</p>
11	/	/	/
10:8	R/W	0x0	<p>DATA_MOD</p> <p>Input data mode selection</p> <p>000: non-tile-based planar data</p> <p>001: interleaved data</p> <p>010: non-tile-based UV combined data</p> <p>100: tile-based planar data</p> <p>110: tile-based UV combined data</p> <p>other: reserved</p>
7	/	/	/
6:4	R/W	0x0	<p>DATA_FMT</p> <p>Input component data format</p> <p>In non-tile-based planar data mode:</p> <p>000: YUV 4:4:4</p> <p>001: YUV 4:2:2</p> <p>010: YUV 4:2:0</p> <p>011: YUV 4:1:1</p>

			<p>101: RGB888</p> <p>Other: Reserved</p> <p>In interleaved data mode:</p> <p>000: YUV 4:4:4</p> <p>001: YUV 4:2:2</p> <p>101: ARGB8888</p> <p>Other: reserved</p> <p>In non-tile-based UV combined data mode:</p> <p>001: YUV 4:2:2</p> <p>010: YUV 4:2:0</p> <p>011: YUV 4:1:1</p> <p>Other: reserved</p> <p>In tile-based planar data mode:</p> <p>001: YUV 4:2:2</p> <p>010: YUV 4:2:0</p> <p>011: YUV 4:1:1</p> <p>Other: Reserved</p> <p>In tile-based UV combined data mode:</p> <p>001: YUV 4:2:2</p> <p>010: YUV 4:2:0</p> <p>011: YUV 4:1:1</p> <p>Other: reserved</p>
3:2	/	/	/
1:0	R/W	0x0	<p>DATA_PS</p> <p>Pixel sequence</p>

			<p>In interleaved YUV422 data mode:</p> <p>00: Y1V0Y0U0</p> <p>01: V0Y1U0Y0</p> <p>10: Y1U0Y0V0</p> <p>11: U0Y1V0Y0</p> <p>In interleaved YUV444 data mode:</p> <p>00: VUYA</p> <p>01: AYUV</p> <p>Other: reserved</p> <p>In UV combined data mode: (UV component)</p> <p>00: V1U1V0U0</p> <p>01: U1V1U0V0</p> <p>Other: reserved</p> <p>In interleaved ARGB8888 data mode:</p> <p>00: BGRA</p> <p>01: ARGB</p> <p>Other: reserved</p>
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DEFE_WB_ADDR_REG

Offset: 0x50			Register Name: DEFE_WB_ADDR_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0x0	WB_ADDR Write-back address setting for output data.

DEFE_OUTPUT_FMT_REG

Offset: 0x5C			Register Name: DEFE_OUTPUT_FMT_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 8	/	/	/
17:1 6	R/W	0	<p>WB_Ch_Sel</p> <p>Write back channel select(chsel)</p> <p>0/1: Ch3</p> <p>2: Ch4</p> <p>3: Ch5</p> <p>Other: reserved</p>
15:9	/	/	/
8	R/W	0x0	<p>BYTE_SEQ</p> <p>Output data byte sequence selection</p> <p>0: P3P2P1P0(word)</p> <p>1: P0P1P2P3(word)</p> <p>For ARGB, when this bit is 0, the byte sequence is BGRA, and when this bit is 1, the byte sequence is ARGB;</p>
7:5	/	/	/
4	R/W	0x0	<p>SCAN_MOD</p> <p>Output interlace enable</p> <p>0: disable</p> <p>1: enable</p> <p>When output interlace enable, scaler selects YUV initial phase according to LCD field signal</p>
3	/	/	/
2:0	R/W	0x0	<p>DATA_FMT</p> <p>Data format</p> <p>000: planar RGB888 conversion data format</p> <p>001: interleaved BGRA8888 conversion data format (Alpha</p>

			<p>always 0xff)</p> <p>010: interleaved ARGB8888 conversion data format (Alpha always 0xff)</p> <p>100: planar YUV 444</p> <p>101: planar YUV 420(only support YUV input and not interleaved mode)</p> <p>110: planar YUV 422(only support YUV input)</p> <p>111: planar YUV 411(only support YUV input)</p> <p>Other: reserved</p>
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DEFE_INT_EN_REG

Offset: 0x60			Register Name: DEFE_INT_EN_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 1	/	/	/
10	R/W	0x0	<p>REG_LOAD_EN</p> <p>Register ready load interrupt enable</p>
9	R/W	0x0	<p>LINE_EN</p> <p>Line interrupt enable</p>
8	/	/	/
7	R/W	0x0	<p>WB_EN</p> <p>Write-back end interrupt enable</p> <p>0: Disable</p> <p>1: Enable</p>
6:0	/	/	/

DEFE_INT_STATUS_REG

Offset: 0x64	Register Name: DEFE_INT_STATUS_REG
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Bit	Read/Writ e	Default/H ex	Description
31:1 1	/	/	/
10	R/W	0x0	REG_LOAD_STATUS Register ready load interrupt status
9	R/W	0x0	LINE_STATUS Line interrupt status
8	/	/	/
7	R/W	0x0	WB_STATUS Write-back end interrupt status
6:0	/	/	/

DEFE_STATUS_REG

Offset: 0x68			Register Name: DEFE_STATUS_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28:1 6	R	0x0	LINE_ON_SYNC Line number(when sync reached)
15	R/W	0x0	WB_ERR_SYNC Sync reach flag when capture in process
14	R/W	0x0	WB_ERR_LOSEDATA Lose data flag when capture in process
13	/	/	/
12	R	0x0	WB_ERR_STATUS write-back error status 0: valid write back 1: un-valid write back

			This bit is cleared through write 0 to reset/start bit in frame control register
11	R	0x0	<p>COEF_ACCESS_STATUS</p> <p>Fir coef access status</p> <p>0: scaler module can access fir coef ram</p> <p>1: CPU can access fir coef ram</p> <p>This bit must be 1 before CPU access fir coef ram. When this bit is 1, scaler module will fetch 0x00004000 from ram.</p>
10:6	/	/	/
5	R	0x0	<p>LCD_FIELD</p> <p>LCD field status</p> <p>0: top field</p> <p>1: bottom field</p>
4	R	0x0	<p>DRAM_STATUS</p> <p>Access dram status</p> <p>0: idle</p> <p>1: busy</p> <p>This flag indicates whether DEFE is accessing dram</p>
3	/	/	/
2	R	0x0	<p>CFG_PENDING</p> <p>Register configuration pending</p> <p>0: no pending</p> <p>1: configuration pending</p> <p>This bit indicates the registers for the next frame has been configured. This bit will be set when configuration ready bit is set and this bit will be cleared when a new frame process begin.</p>
1	R	0x0	<p>WB_STATUS</p> <p>Write-back process status</p> <p>0: write-back end or write-back disable</p>

			1: write-back in process This flag indicates that a full frame has not been written back to memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process end.
0	R	0x0	FRM_BUSY Frame busy. This flag indicates that the frame is being processed. The bit will be set when frame process reset & start is set, and be cleared when frame process reset or disabled.

DEFE_CSC_COEF00_REG

Offset: 0x70			Register Name: DEFE_CSC_COEF00_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient* 2^{10}

DEFE_CSC_COEF01_REG

Offset: 0x74			Register Name: DEFE_CSC_COEF01_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient* 2^{10}

DEFE_CSC_COEF02_REG

Offset: 0x78			Register Name: DEFE_CSC_COEF02_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the Y/G coefficient the value equals to coefficient* 2^{10}

DEFE_CSC_COEF03_REG

Offset: 0x7C			Register Name: DEFE_CSC_COEF03_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 4	/	/	/
13:0	R/W	0x0	CONT the Y/G constant the value equals to coefficient* 2^4

DEFE_CSC_COEF10_REG

Offset: 0x80			Register Name: DEFE_CSC_COEF10_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient* 2^{10}

DEFE_CSC_COEF11_REG

Offset: 0x84			Register Name: DEFE_CSC_COEF11_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient* 2^{10}

DEFE_CSC_COEF12_REG

Offset: 0x88			Register Name: DEFE_CSC_COEF12_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the U/R coefficient the value equals to coefficient* 2^{10}

DEFE_CSC_COEF13_REG

Offset: 0x8C			Register Name: DEFE_CSC_COEF13_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 4	/	/	/
13:0 0	R/W	0x0	CONT the U/R constant the value equals to coefficient* 2^4

DEFE_CSC_COEF20_REG

Offset: 0x90			Register Name: DEFE_CSC_COEF20_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient* 2^{10}

DEFE_CSC_COEF21_REG

Offset: 0x94			Register Name: DEFE_CSC_COEF21_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient* 2^{10}

DEFE_CSC_COEF22_REG

Offset: 0x98			Register Name: DEFE_CSC_COEF22_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient* 2^{10}

DEFE_CSC_COEF23_REG

Offset: 0x9C			Register Name: DEFE_CSC_COEF23_REG
Bit	Read/Writ e	Default/H ex	Description
31:4	/	/	/
13:0	R/W	0x0	CONT the V/B constant the value equals to coefficient*2 ⁴

DEFE_WB_LINESTRD_EN_REG

Offset: 0xD0			Register Name: DEFE_WB_LINESTRD_EN_REG
Bit	Read/Writ e	Default/H ex	Description
31:1	/	/	/
0	R/W	0x0	EN Write back line-stride enable 0: disable 1: enable

DEFE_WB_LINESTRD_REG

Offset: 0xD4			Register Name: DEFE_WB_LINESTRD_REG
Bit	Read/Writ e	Default/H ex	Description
31:1	/	/	/
0	R/W	0x0	LINE_STRD Ch3 write back line-stride

DEFE_CHO_INSIZE_REG

Offset: 0x100			Register Name: DEFE_CHO_INSIZE_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28:1 6	R/W	0x0	<p>IN_HEIGHT</p> <p>Input image Y/G component height</p> <p>Input image height = The value of these bits add 1</p>
15:1 3	/	/	/
12:0	R/W	0x0	<p>IN_WIDTH</p> <p>Input image Y/G component width</p> <p>The image width = The value of these bits add 1</p> <p>When line buffer result selection is original data, the maximum width is 1366.</p>

DEFE_CHO_OUTSIZE_REG

Offset: 0x104			Register Name: DEFE_CHO_OUTSIZE_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28:1 6	R/W	0x0	<p>OUT_HEIGHT</p> <p>Output layer Y/G component height</p> <p>The output layer height = The value of these bits add 1</p>
15:1 3	/	/	/

12:0	R/W	0x0	<p>OUT_WIDTH</p> <p>Output layer Y/G component width</p> <p>The output layer width = The value of these bits add 1</p> <p>When line buffer result selection is horizontal filtered result, the maximum width is 1366.</p>
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DEFE_CH0_HORZFACT_REG

Offset: 0x108			Register Name: DEFE_CH0_HORZFACT_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:1 6	R/W	0x0	<p>FACTOR_INT</p> <p>The integer part of the horizontal scaling ratio</p> <p>the horizontal scaling ratio = input width/output width</p>
15:0	R/W	0x0	<p>FACTOR_FRAC</p> <p>The fractional part of the horizontal scaling ratio</p> <p>the horizontal scaling ratio = input width/output width</p>

DEFE_CH0_VERTFACT_REG

Offset: 0x10C			Register Name: DEFE_CH0_VERTFACT_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:1 6	R/W	0x0	<p>FACTOR_INT</p> <p>The integer part of the vertical scaling ratio</p>

			the vertical scaling ratio = input height/output height
15:0	R/W	0x0	<p>FACTOR_FRAC</p> <p>The fractional part of the vertical scaling ratio</p> <p>the vertical scaling ratio = input height /output height</p>

DEFE_CHO_HORZPHASE_REG

Offset: 0x110			Register Name: DEFE_CHO_HORZPHASE_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 0	/	/	/
19:0	R/W	0x0	<p>PHASE</p> <p>Y/G component initial phase in horizontal (complement)</p> <p>This value equals to initial phase * 2^{16}</p>

DEFE_CHO_VERTPHASE0_REG

Offset: 0x114			Register Name: DEFE_CHO_VERTPHASE0_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 0	/	/	/
19:0	R/W	0x0	<p>PHASE</p> <p>Y/G component initial phase in vertical for top field (complement)</p> <p>This value equals to initial phase * 2^{16}</p>

DEFE_CHO_VERTPHASE1_REG

Offset: 0x118	Register Name: DEFE_CHO_VERTPHASE1_REG
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Bit	Read/Writ e	Default/H ex	Description
31:2 0	/	/	/
19:0	R/W	0x0	<p>PHASE</p> <p>Y/G component initial phase in vertical for bottom field (complement)</p> <p>This value equals to initial phase * 2^{16}</p>

DEFE_CH0_HORZTAP_REG

Offset: 0x120			Register Name: DEFE_CH0_HORZTAP_REG
Bit	Read/Writ e	Default/H ex	Description
31	/	/	/
30:2 4	R/W	0x1	<p>TAP3</p> <p>Tap 3 offset in horizontal</p>
23	/	/	/
22:1 6	R/W	0x1	<p>TAP2</p> <p>Tap 2 offset in horizontal</p>
15	/	/	/
14:8	R/W	0x1	<p>TAP1</p> <p>Tap 1 offset in horizontal</p>
7	/	/	/
6:0	R/W	0x7D	<p>TAP0</p> <p>Tap 0 offset in horizontal</p>

DEFE_CH0_VERTTAP_REG

Offset: 0x128			Register Name: DEFE_CH0_VERTTAP_REG
Bit	Read/Writ e	Default/H ex	Description

31	/	/	/
30:2 4	R/W	0x1	TAP3 Tap 3 offset in vertical
23	/	/	/
22:1 6	R/W	0x1	TAP2 Tap 2 offset in vertical
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in vertical
7	/	/	/
6:0	R/W	0x7F	TAPO Tap 0 offset in vertical

DEFE_CH1_INSIZE_REG

Offset: 0x200			Register Name: DEFE_CH1_INSIZE_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28:1 6	R/W	0x0	IN_HEIGHT Input image U/R component height Input image height = The value of these bits add 1
15:1 3	/	/	/
12:0	R/W	0x0	IN_WIDTH Input image U/R component width The image width = The value of these bits add 1 When line buffer result selection is original data, the

			maximum width is 1366.
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DEFE_CH1_OUTSIZE_REG

Offset: 0x204			Register Name: DEFE_CH1_OUTSIZE_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28:1 6	R/W	0x0	<p>OUT_HEIGHT Output layer U/R component height The output layer height = The value of these bits add 1</p>
15:1 3	/	/	/
12:0	R/W	0x0	<p>OUT_WIDTH Output layer U/R component width The output layer width = The value of these bits add 1</p> <p>When line buffer result selection is horizontal filtered result, the maximum width is 1366.</p>

DEFE_CH1_HORZFACT_REG

Offset: 0x208			Register Name: DEFE_CH1_HORZFACT_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:1 6	R/W	0x0	<p>FACTOR_INT The integer part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width</p>

15:0	R/W	0x0	FACTOR_FRAC The fractional part of the horizontal scaling ratio the horizontal scaling ratio = input width/output width
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DEFE_CH1_VERTFACT_REG

Offset: 0x20C			Register Name: DEFE_CH1_VERTFACT_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:1 6	R/W	0x0	FACTOR_INT The integer part of the vertical scaling ratio the vertical scaling ratio = input height/output height
15:0	R/W	0x0	FACTOR_FRAC The fractional part of the vertical scaling ratio the vertical scaling ratio = input height /output height

DEFE_CH1_HORZPHASE_REG

Offset: 0x210			Register Name: DEFE_CH1_HORZPHASE_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 0	/	/	/
19:0	R/W	0x0	PHASE U/R component initial phase in horizontal (complement) This value equals to initial phase * 2^{16}

DEFE_CH1_VERTPHASE0_REG

Offset: 0x214			Register Name: DEFE_CH1_VERTPHASE0_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 0	/	/	/
19:0	R/W	0x0	<p>PHASE</p> <p>U/R component initial phase in vertical for top field (complement)</p> <p>This value equals to initial phase * 2^{16}</p>

DEFE_CH1_VERTPHASE1_REG

Offset: 0x218			Register Name: DEFE_CH1_VERTPHASE1_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 0	/	/	/
19:0	R/W	0x0	<p>PHASE</p> <p>U/R component initial phase in vertical for bottom field (complement)</p> <p>This value equals to initial phase * 2^{16}</p>

DEFE_CH1_HORZTAP_REG

Offset: 0x220			Register Name: DEFE_CH1_HORZTAP_REG
Bit	Read/Writ e	Default/H ex	Description
31	/	/	/
30:2 4	R/W	0x1	<p>TAP3</p> <p>Tap 3 offset in horizontal</p>
23	/	/	/
22:1	R/W	0x1	TAP2

6			Tap 2 offset in horizontal
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in horizontal
7	/	/	/
6:0	R/W	0x7D	TAP0 Tap 0 offset in horizontal

DEFE_CH1_VERTTAP_REG

Offset: 0x228			Register Name: DEFE_CH1_VERTTAP_REG
Bit	Read/Writ e	Default/H ex	Description
31	/	/	/
30:2 4	R/W	0x1	TAP3 Tap 3 offset in vertical
23	/	/	/
22:1 6	R/W	0x1	TAP2 Tap 2 offset in vertical
15	/	/	/
14:8	R/W	0x1	TAP1 Tap 1 offset in vertical
7	/	/	/
6:0	R/W	0x7F	TAP0 Tap 0 offset in vertical

DEFE_CHO_HORZCOEF_REGN (N=0 :31)

Offsetn: 0x400+N*4			Register Name: DEFE_CHO_HORZCOEF_REGN
Bit	Read/Writ e	Default/H ex	Description

31:2 4	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient* 2^6
23:1 6	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient* 2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient* 2^6
7:0	R/W	0x0	TAPO Horizontal tap0 coefficient The value equals to coefficient* 2^6

DEFE_CHO_VERTCOEF_REGN (N=0 :31)

Offsetn: 0x500+N*4			Register Name: DEFE_CHO_VERTCOEF_REGN
Bit	Read/Writ e	Default/H ex	Description
31:2 4	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient* 2^6
23:1 6	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient* 2^6

15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient* 2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient* 2^6

DEFE_CH1_HORZCOEF_REGN (N=0 :31)

Offsetn: 0x600+N*4			Register Name: DEFE_CH1_HORZCOEF_REGN
Bit	Read/Writ e	Default/H ex	Description
31:2 4	R/W	0x0	TAP3 Horizontal tap3 coefficient The value equals to coefficient* 2^6
23:1 6	R/W	0x0	TAP2 Horizontal tap2 coefficient The value equals to coefficient* 2^6
15:8	R/W	0x0	TAP1 Horizontal tap1 coefficient The value equals to coefficient* 2^6
7:0	R/W	0x0	TAP0 Horizontal tap0 coefficient The value equals to coefficient* 2^6

DEFE_CH1_VERTCOEF_REGN (N=0 :31)

Offsetn: 0x700+N*4			Register Name: DEFE_CH1_VERTCOEF_REGN
Bit	Read/Writ e	Default/H ex	Description
31:2 4	R/W	0x0	TAP3 Vertical tap3 coefficient The value equals to coefficient* 2^6
23:1 6	R/W	0x0	TAP2 Vertical tap2 coefficient The value equals to coefficient* 2^6
15:8	R/W	0x0	TAP1 Vertical tap1 coefficient The value equals to coefficient* 2^6
7:0	R/W	0x0	TAP0 Vertical tap0 coefficient The value equals to coefficient* 2^6

5.4 Display Engine Back-End

5.4.1 Overview

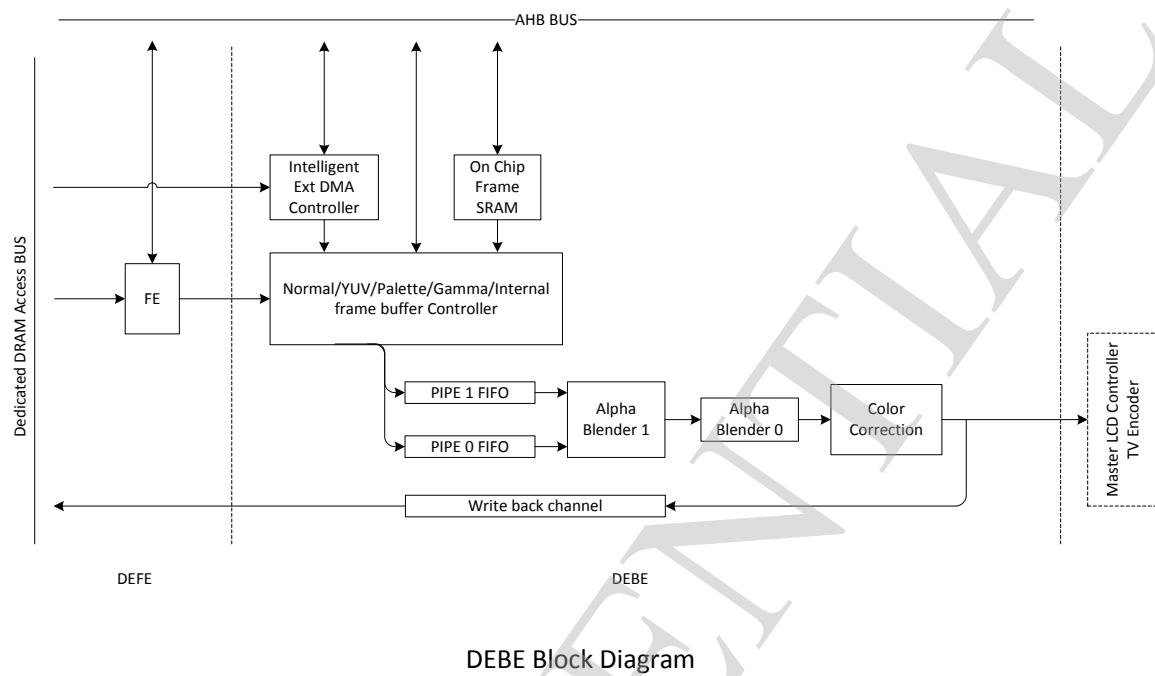
The display engine back-end (DEBE) provides overlay and alpha blending functions after receiving data from DEFE or SDRAM. After alpha blended, the data will either be delivered to Color Correction for image enhancement, or bypassed to flowing part LCD, etc.

The DEFE has two pipes data path.

The DEFE features:

- Support layer size up to 8192x8192 pixels
- Support four layers overlay in one pipe
- Support alpha blending
- Support color key
- Support pre-multiply alpha image data
- Support internal frame buffer scaling(1x/2x/4x)
- Support gamma correction
- Support output color correction
- Supported input formats: 1/2/4/8bpp / RGB655 / RGB565 / RGB556 / RGB888 / ARGB1555 / ARGB4444 / RGB8888 / iYUV422 / iYUV444 / YUV422 / YUV420 / YUV411

5.4.2 DEBE Block Diagram



5.4.3 Display Engine Memory Mapping

Offset	
0x0000	Reserved
0x07FF	Registers
0x0800	Reserved
0x0DFF	Reserved
0x0E00	Reserved
0x43FF	Gamma Table
0x4400	Reserved
0x47FF	Reserved
0x4800	Reserved
0x4BFF	Reserved
0x4C00	Reserved
0x4FFF	Reserved
0x5000	Pipe0 Palette
0x53FF	Pipe1 Palette
0x5400	Pipe1 Palette
0x57FF	Reserved
0x5800	Reserved
0xFFFF	Reserved

Display Engine Memory Mapping

5.4.4 DEBE Register List

Module name	Base address
DEBE	0x01E6 0000

Register name	Offset	Description
DEBE_MODCTL_REG	0x800	DE back-end mode control register
DEBE_BACKCOLOR_REG	0x804	DE-back color control register
DEBE_DISSIZE_REG	0x808	DE-back display size setting register
DEBE_LAYSIZE_REG	0x810 – 0x81C	DE-layer size register
DEBE_LAYCOOR_REG	0x820 – 0x82C	DE-layer coordinate control register
DEBE_LAYLINEWIDTH_REG	0x840 – 0x84C	DE-layer frame buffer line width register
DEBE_LAYFB_L32ADD_REG	0x850 – 0x85C	DE-layer frame buffer low 32 bit address register
DEBE_LAYFB_H4ADD_REG	0x860	DE-layer frame buffer high 4 bit address register
DEBE_REGBUFFCTL_REG	0x870	DE-Register buffer control register
DEBE_CKMAX_REG	0x880	DE-color key MAX register
DEBE_CKMIN_REG	0x884	DE-color key MIN register
DEBE_CKCFG_REG	0x888	DE-color key configuration register
DEBE_ATTCTL_REG0	0x890 – 0x89C	DE-layer attribute control register0
DEBE_ATTCTL_REG1	0x8A0 – 0x8AC	DE-layer attribute control register1
DEBE_IYUVCTL_REG	0x920	DE backend input YUV channel control register
DEBE_IYUVADD_REG	0x930 – 0x938	DE backend YUV channel frame buffer address register
DEBE_IYUVLINewidth_REG	0x940 – 0x948	DE backend YUV channel buffer line width register
DEBE_YGCOEF_REG	0x950 – 0x958	DE backend Y/G coefficient register
DEBE_YGCONS_REG	0x95C	DE backend Y/G constant register

DEBE_URCOEF_REG	0x960 – 0x968	DE backend U/R coefficient register
DEBE_URCONS_REG	0x96C	DE backend U/R constant register
DEBE_VBCOEF_REG	0x970 – 0x978	DE backend V/B coefficient register
DEBE_VBCONS_REG	0x97C	DE backend V/B constant register
DEBE_OCCTL_REG	0x9C0	DE backend output color control register
DEBE_OCRCOEF_REG	0x9D0-0x9D8	DE backend output color R coefficient register
DEBE_OCRCONS_REG	0x9DC	DE backend output color R constant register
DEBE_OCGCOEF_REG	0x9E0-0x9E8	DE backend output color G coefficient register
DEBE_OCGCONS_REG	0x9EC	DE backend output color G constant register
DEBE_OCBCOEF_REG	0x9F0-0x9F8	DE backend output color B coefficient register
DEBE_OCBCONS_REG	0x9FC	DE backend output color B constant register
	Memories	
	0x4400-0x47FF	Gamma table
	0x5000-0x53FF	Pipe0 palette table
	0x5400-0x57FF	Pipe1 palette table

5.4.5 DEBE Register Description

DE BACK-END MODE CONTROL REGISTER

Offset: 0x800			Register Name: DEBE_MODCTL_REG
Bit	Read/Writ e	Default/H ex	Description
31:30	/	/	/
29	R/W	0	<p>LINE_SEL</p> <p>Start top/bottom line selection in interlace mode</p>
28	R/W	0	<p>ITLMOD_EN</p> <p>Interlace mode enable</p> <p>0:disable</p> <p>1:enable</p>
27	/	/	/
22:20	R/W	0	<p>OUT_SEL</p> <p>Output selection</p> <p>000:LCD</p> <p>110:FEO only</p> <p>Other: reserved</p>
19:18	/	/	/
17	R/W	0	<p>OSCA_EN</p> <p>Output scaling function enable</p> <p>0:disable</p> <p>1:enable</p>
16:12	/	/	/
11	R/W	0	<p>LAY3_EN</p> <p>Layer3 Enable/Disable</p> <p>0: Disabled</p>

			1: Enabled
10	R/W	0	LAY2_EN Layer2 Enable/Disable 0: Disabled 1: Enabled
9	R/W	0	LAY1_EN Layer1 Enable/Disable 0: Disabled 1: Enabled
8	R/W	0	LAY0_EN Layer0 Enable/Disable 0: Disabled 1: Enabled
7:2	/	/	/
1	R/W	0	START_CTL Normal output channel Start & Reset control 0: reset 1: start
0	R/W	0	DEBE_EN DE back-end enable/disable 0: disable 1: enable

DE-BACK COLOR CONTROL REGISTER

Offset: 0x804			Register Name: DEBE_BACKCOLOR_REG
Bit	Read/Writ e	Default/H ex	Description
31:2	/	/	/
4			

23:16	R/W	UDF	BK_RED Red Red screen background color value
15:8	R/W	UDF	BK_GREEN Green Green screen background color value
7:0	R/W	UDF	BK_BLUE Blue Blue screen background color value

DE-BACK DISPLAY SIZE SETTING REGISTER

Offset: 0x808			Register Name: DEBE_DISSIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:16	R/W	UDF	DIS_HEIGHT Display height The real display height = The value of these bits add 1
15:0	R/W	UDF	DIS_WIDTH Display width The real display width = The value of these bits add 1

DE-LAYER SIZE REGISTER

Offset: Layer 0: 0x810 Layer 1: 0x814 Layer 2: 0x818 Layer 3: 0x81C			Register Name: DEBE_LAYSIZE_REG
Bit	Read/Writ e	Default/H ex	Description

31:2 9	/	/	/
28:1 6	R/W	UDF	LAY_HEIGHT Layer Height The Layer Height = The value of these bits add 1
15:1 3	/	/	/
12:0	R/W	UDF	LAY_WIDTH Layer Width The Layer Width = The value of these bits add 1

DE-LAYER COORDINATE CONTROL REGISTER

Offset: Layer 0: 0x820 Layer 1: 0x824 Layer 2: 0x828 Layer 3: 0x82C			Register Name: DEBE_LAYCOOR_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R/W	UDF	LAY_YCOOR Y coordinate Y is the left-top y coordinate of layer on screen in pixels The Y represent the two's complement
15:0	R/W	UDF	LAY_XCOOR X coordinate X is left-top x coordinate of the layer on screen in pixels The X represent the two's complement

Note: Setting the layer0-layer3 the coordinate (left-top) on screen control information

DE-LAYER FRAME BUFFER LINE WIDTH REGISTER

Offset:			Register Name: DEBE_LAYLINEWIDTH_REG
Layer 0: 0x840			
Layer 1: 0x844			
Layer 2: 0x848			
Layer 3: 0x84C			
Bit	Read/W rite	Default /Hex	Description
31:0	R/W	UDF	LAY_LINEWIDTH Layer frame buffer line width in bits

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

DE-LAYER FRAME BUFFER LOW 32 BIT ADDRESS REGISTER

Offset:			Register Name: DEBE_LAYFB_L32ADD_REG
Layer 0: 0x850			
Layer 1: 0x854			
Layer 2: 0x858			
Layer 3: 0x85C			
Bit	Read/W rite	Default /Hex	Description
31:0	R/W	UDF	LAYFB_L32ADD Buffer start Address Layer Frame start Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

DE-LAYER FRAME BUFFER HIGH 4 BIT ADDRESS REGISTER

Offset: 0x860			Register Name: DEBE_LAYFB_H4ADD_REG
Bit	Read/W rite	Default /Hex	Description

31:28	/	/	/
27:24	R/W	UDF	LAY3FB_H4ADD Layer3 Layer Frame Buffer Address in bit
23:20	/	/	/
19:16	R/W	UDF	LAY2FB_H4ADD Layer2 Layer Frame Buffer Address in bit
15:12	/	/	/
11:8	R/W	UDF	LAY1FB_H4ADD Layer1 Layer Frame Buffer Address in bit
7:4	/	/	/
3:0	R/W	UDF	LAY0FB_H4ADD Layer0 Layer Frame Buffer Address in bit

Note: If the layer is selected by video channel or YUV channel, the setting of this register will be ignored.

DE-REGISTER BUFFER CONTROL REGISTER

Offset: 0x870			Register Name: DEBE_REGBUFFCTL_REG
Bit	Read/Writ e	Default/H ex	Description
31: 2	/	/	/
1	R/W	0X00	REGAUTOLOAD_DIS Module registers loading auto mode disable control 0: registers auto loading mode 1: disable registers auto loading mode, the registers will be loaded by write 1 to bit0 of this register
0	R/W	0X00	REGLOADCTL

			<p>Register load control</p> <p>When the Module registers loading auto mode disable control bit is set, the registers will be loaded by write 1 to the bit, and the bit will self clean when the registers is loading done.</p>
--	--	--	---

DE-COLOR KEY MAX REGISTER

Offset: 0x880			Register Name: DEBE_CKMAX_REG
Bit	Read/Writ e	Default/H ex	Description
31:24	/	/	/
23:16	R/W	UDF	<p>CKMAX_R</p> <p>Red</p> <p>Red color key max</p>
15:8	R/W	UDF	<p>CKMAX_G</p> <p>Green</p> <p>Green color key max</p>
7:0	R/W	UDF	<p>CKMAX_B</p> <p>Blue</p> <p>Blue color key max</p>

DE-COLOR KEY MIN REGISTER

Offset: 0x884			Register Name: DEBE_CKMIN_REG
Bit	Read/Writ e	Default/H ex	Description
31:24	/	/	/
23:16	R/W	UDF	<p>CKMIN_R</p> <p>Red</p> <p>Red color key min</p>
15:8	R/W	UDF	CKMIN_G

			Green Green color key min
7:0	R/W	UDF	CKMIN_B Blue Blue color key min

DE-COLOR KEY CONFIGURATION REGISTER

Offset: 0x888			Register Name: DEBE_CKCFG_REG
Bit	Read/W rite	Default /Hex	Description
31:6	/	/	/
5:4	R/W	UDF	CKR_MATCH Red Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
3:2	R/W	UDF	CKG_MATCH Green Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)
1:0	R/W	UDF	CKB_MATCH Blue Match Rule 00: always match 01: always match 10: match if (Color Min=<Color<=Color Max) 11: match if (Color>Color Max or Color<Color Min)

DE-LAYER ATTRIBUTE CONTROL REGISTER0

Offset:			Register Name: DEBE_ATTCTL_REG0
Layer0: 0x890			
Layer1: 0x894			
Layer2: 0x898			
Layer3: 0x89C			
Bit	Read/Writ e	Default/H ex	Description
31:2 4	R/W	UDF	<p>LAY_GLBALPHA</p> <p>Alpha value</p> <p>Alpha value is used for this layer</p>
23:2 2	R/W	UDF	<p>LAY_WORKMOD</p> <p>Layer working mode selection</p> <p>00: normal mode (Non-Index mode)</p> <p>01: palette mode (Index mode)</p> <p>10: internal frame buffer mode</p> <p>11: gamma correction</p> <p>Except the normal mode, if the other working mode is selected, the on chip SRAM will be enabled.</p>
21:2 0	R/W	UDF	<p>PREMUL</p> <p>0: normal input layer</p> <p>1: pre-multiply input layer</p> <p>Other: reserved</p>
19:1 8	R/W	UDF	<p>CKEN</p> <p>Color key Mode</p> <p>00: disabled color key</p> <p>01: The layer color key match another channel pixel data in Alpha Blender1.</p> <p>1x: Reserved</p>

			Only 2 channels pixel data can get to Alpha Blender1 at the same screen coordinate.
17:1 6	/	/	/
15	R/W	UDF	<p>LAY_PIPESEL</p> <p>Pipe Select</p> <p>0: select Pipe 0</p> <p>1: select Pipe 1</p>
14:1 2	/	/	/
11:1 0	R/W	UDF	<p>LAY_PRISEL</p> <p>Priority</p> <p>The rule is: 11>10>01>00</p> <p>When more than 2 layers are enabled, the priority value of each layer must be different, soft designer must keep the condition.</p> <p>If more than 1 layer selects the same pipe, in the overlapping area, only the pixel of highest priority layer can pass the pipe to blender1.</p> <p>If both 2 pipes are selected by layers, in the overlapping area, the alpha value will use the alpha value of higher priority layer in the blender1.</p>
9:5	/	/	/
4	R/W	UDF	<p>LAY_VDOSEL</p> <p>Video channel selection control</p> <p>0:select video channel 0 (FE0)</p> <p>1: Reserved</p> <p>The selection setting is only valid when Layer video channel</p>

			selection is enabled.
3	/	/	/
2	R/W	UDF	<p>LAY_YUVEN</p> <p>YUV channel selection</p> <p>0: disable</p> <p>1: enable</p> <p>Setting 2 or more layers YUV channel mode is illegal, programmer should confirm it.</p>
1	R/W	UDF	<p>LAY_VDOEN</p> <p>Layer video channel selection enable control</p> <p>0: disable</p> <p>1: enable</p> <p>Normally, one layer can not be set both video channel and YUV channel mode, if both 2 mode is set, the layer will work in video channel mode, YUV channel mode will be ignored, programmer should confirm it.</p> <p>Setting 2 or more layers video channel mode is illegal, programmer should confirm it.</p>
0	R/W	UDF	<p>LAY_GLBALPHAEN</p> <p>Alpha Enable</p> <p>0: Disabled the alpha value of this register</p> <p>1: Enabled the alpha value of this register for the layer</p>

DE-LAYER ATTRIBUTE CONTROL REGISTER1

Offset: Layer0: 0x8A0 Layer1: 0x8A4 Layer2: 0x8A8	Register Name: DEBE_ATTCTL_REG1
--	---------------------------------

Layer3: 0x8AC			
Bit	Read/W rite	Default /Hex	Description
31:16	/	/	/
15:14	R/W	UDF	<p>LAY_HSCAFCT</p> <p>Setting the internal frame buffer scaling factor, only valid in internal frame buffer mode</p> <p>SH</p> <p>Height scale factor</p> <p>00: no scaling</p> <p>01: *2</p> <p>10: *4</p> <p>11: Reserved</p>
13:12	R/W	UDF	<p>LAY_WSCAFCT</p> <p>Setting the internal frame buffer scaling factor, only valid in internal frame buffer mode</p> <p>SW</p> <p>Width scale factor</p> <p>00: no scaling</p> <p>01: *2</p> <p>10: *4</p> <p>11: Reserved</p>
11:8	R/W	UDF	<p>LAY_FBFMT</p> <p>Frame buffer format</p> <p>Normal mode data format</p> <p>0000: mono 1-bpp</p> <p>0001: mono 2-bpp</p> <p>0010: mono 4-bpp</p> <p>0011: mono 8-bpp</p> <p>0100: color 16-bpp (R:6/G:5/B:5)</p>

			<p>0101: color 16-bpp (R:5/G:6/B:5)</p> <p>0110: color 16-bpp (R:5/G:5/B:6)</p> <p>0111: color 16-bpp (Alpha:1/R:5/G:5/B:5)</p> <p>1000: color 16-bpp (R:5/G:5/B:5/Alpha:1)</p> <p>1001: color 24-bpp (Padding:8/R:8/G:8/B:8)</p> <p>1010: color 32-bpp (Alpha:8/R:8/G:8/B:8)</p> <p>1011: color 24-bpp (R:8/G:8/B:8)</p> <p>1100: color 16-bpp (Alpha:4/R:4/G:4/B:4)</p> <p>1101: color 16-bpp (R:4/G:4/B:4/Alpha:4)</p> <p>Other: Reserved</p> <p> Palette Mode data format</p> <p>In palette mode, the data of external frame buffer is regarded as pattern.</p> <p>0000: 1-bpp</p> <p>0001: 2-bpp</p> <p>0010: 4-bpp</p> <p>0011: 8-bpp</p> <p>other: Reserved</p> <p> Internal Frame buffer mode data format</p> <p>0000: 1-bpp</p> <p>0001: 2-bpp</p> <p>0010: 4-bpp</p> <p>0011: 8-bpp</p> <p>Other: Reserved</p>
7:3	/	/	/
2	R/W	UDF	LAY_BRSWAPEN B R channel swap

			0: RGB. Follow the bit[11:8]----RGB 1: BGR. Swap the B R channel in the data format.
1:0	R/W	UDF	LAY_FBPS PS Pixels Sequence See the follow table "Pixels Sequence"

DE BACKEND INPUT YUV CHANNEL CONTROL REGISTER

Offset: 0x920			Register Name: DEBE_IYUVCTL_REG
Bit	Read/W rite	Default /Hex	Description
31:15	/	/	/
14:12	R/W	UDF	IYUV_FBFMT Input data format 000: planar YUV 411 001: planar YUV 422 010: planar YUV 444 011: interleaved YUV 422 100: interleaved YUV 444 Other: illegal
11:10	/	/	/
9:8	R/W	UDF	IYUV_FBPS Pixel sequence In planar data format mode: 00: Y3Y2Y1Y0 01: Y0Y1Y2Y3 (the other 2 components are same) Other: illegal In interleaved YUV 422 data format mode: 00: UYVY

			01: YUYV 10: VYUY 11: YVYU In interleaved YUV 444 data format mode: 00: AYUV 01: VUYA Other: illegal
7:5	/	/	/
4	R/W	UDF	IYUV_LINNEREN 0: linner 1:
3:1	/	/	/
0	R/W	UDF	IYUV_EN YUV channel enable control 0: disable 1: enable

Source data input data ports:

Input buffer channel	Planar YUV	Interleaved YUV
Channel0	Y	YUV
Channel1	U	-
Channel2	V	-

DE BACKEND YUV CHANNEL FRAME BUFFER ADDRESS REGISTER

Offset: Channel 0 : 0x930 Channel 1 : 0x934	Register Name: DEBE_IYUVADD_REG
---	---------------------------------

Channel 2 : 0x938			
Bit	Read/W rite	Default /Hex	Description
31:0	R/W	UDF	IYUV_ADD Buffer Address Frame buffer address in BYTE

DE BACKEND YUV CHANNEL BUFFER LINE WIDTH REGISTER

Offset:	Register Name: DEBE_IYUVLINewidth_REG		
Channel 0 : 0x940			
Channel 1 : 0x944			
Channel 2 : 0x948			
Bit	Read/W rite	Default /Hex	Description
31:0	R/W	UDF	IYUV_LINEWIDTH Line width The width is the distance from the start of one line to the start of the next line. Description in bits

YUV to RGB conversion algorithm formula:

R =
(R Y component coefficient * Y) +
(R U component coefficient * U) +
(R V component coefficient * V) +
R constant
G =
(G Y component coefficient * Y) +
(G U component coefficient * U) +

(G V component coefficient * V) +

G constant

B =

(B Y component coefficient * Y) +

(B U component coefficient * U) +

(B V component coefficient * V) +

B constant

DE BACKEND Y/G COEFFICIENT REGISTER

Offset: G/Y component: 0x950 R/U component: 0x954 B/V component: 0x958			Register Name: DEBE_YGCOEF_REG
Bit	Read/W rite	Default /Hex	Description
31:13	/	/	/
12:0	R/W	UDF	IYUV_YGCOEF the Y/G coefficient the value equals to coefficient* 2^{10}

DE BACKEND Y/G CONSTANT REGISTER

Offset: 0x95C			Register Name: DEBE_YGCONS_REG
Bit	Read/W rite	Default /Hex	Description
31:14	/	/	/
13:0	R/W	UDF	IYUV_YGCONS the Y/G constant the value equals to coefficient* 2^4

DE BACKEND U/R COEFFICIENT REGISTER

Offset: G/Y component: 0x960 R/U component: 0x964 B/V component: 0x968			Register Name: DEBE_URCOEF_REG
Bit	Read/W rite	Default /Hex	Description
31:13	/	/	/
12:0	R/W	UDF	IYUV_URCOEF the U/R coefficient the value equals to coefficient* 2^{10}

DE BACKEND U/R CONSTANT REGISTER

Offset: 0x96C			Register Name: DEBE_URCONS_REG
Bit	Read/W rite	Default /Hex	Description
31:14	/	/	/
13:0	R/W	UDF	IYUV_URCONS the U/R constant the value equals to coefficient* 2^4

DE BACKEND V/B COEFFICIENT REGISTER

Offset: G/Y component: 0x970 R/U component: 0x974 B/V component: 0x978			Register Name: DEBE_VBCOEF_REG
Bit	Read/W rite	Default /Hex	Description
31:13	/	/	/
12:0	R/W	UDF	IYUV_VBCOEF

			the V/B coefficient the value equals to coefficient*2 ¹⁰
--	--	--	--

DE BACKEND V/B CONSTANT REGISTER

Offset: 0x97C			Register Name: DEBE_VBCONS_REG
Bit	Read/W rite	Default /Hex	Description
31:14	/	/	/
13:0	R/W	UDF	IYUV_VBCONS the V/B constant the value equals to coefficient*2 ⁴

DE BACKEND OUTPUT COLOR CONTROL REGISTER

Offset: 0x9C0			Register Name: DEBE_OCCTL_REG
Bit	Read/W rite	Default /Hex	Description
31:1	/	/	/
0	R/W	UDF	OC_EN Color control module enable control 0: disable 1: enable

Color correction conversion algorithm formula:

R =
(R R component coefficient * R) +
(R G component coefficient * G) +
(R B component coefficient * B) +
R constant

G =
 (G R component coefficient * R) +
 (G G component coefficient * G) +
 (G B component coefficient * B) +
 G constant

B =
 (B R component coefficient * R) +
 (B G component coefficient * G) +
 (B B component coefficient * B) +
 B constant

DE BACKEND OUTPUT COLOR R COEFFICIENT REGISTER

Offset: R component: 0x9D0 G component: 0x9D4 B component: 0x9D8			Register Name: DEBE_OCRCOEF_REG
Bit	Read/W rite	Default /Hex	Description
31:14	/	/	/
13:0	R/W	UDF	OC_RCOEF the R coefficient the value equals to coefficient* 2^{10}

DE BACKEND OUTPUT COLOR R CONSTANT REGISTER

Offset: 0x9DC			Register Name: DEBE_OCRCONS_REG
Bit	Read/W rite	Default /Hex	Description
31:15	/	/	/
14:0	R/W	UDF	OC_RCONS

			the R constant the value equals to coefficient* 2^4
--	--	--	--

DE BACKEND OUTPUT COLOR G COEFFICIENT REGISTER

Offset: R component: 0x9E0 G component: 0x9E4 B component: 0x9E8			Register Name: DEBE_OCGCOEF_REG
Bit	Read/W rite	Default /Hex	Description
31:14	/	/	/
13:0	R/W	UDF	OC_GCOEF the G coefficient the value equals to coefficient* 2^{10}

DE BACKEND OUTPUT COLOR G CONSTANT REGISTER

Offset: 0x9EC			Register Name: DEBE_OCGCONS_REG
Bit	Read/W rite	Default /Hex	Description
31:15	/	/	/
14:0	R/W	UDF	OC_GCONS the G constant the value equals to coefficient* 2^4

DE BACKEND OUTPUT COLOR B COEFFICIENT REGISTER

Offset: G/Y component: 0x9F0 R/U component: 0x9F4 B/V component: 0x9F8	Register Name: DEBE_OCBCOEF_REG
---	---------------------------------

Bit	Read/W rite	Default /Hex	Description
31:14	/	/	/
13:0	R/W	UDF	OC_BCOEF the B coefficient the value equals to coefficient* 2^{10}

DE BACKEND OUTPUT COLOR B CONSTANT REGISTER

Offset: 0x9FC			Register Name: DEBE_OCBCONS_REG
Bit	Read/W rite	Default /Hex	Description
31:15	/	/	/
14:0	R/W	UDF	OC_BCONS the B constant the value equals to coefficient* 2^4

PALETTE MODE

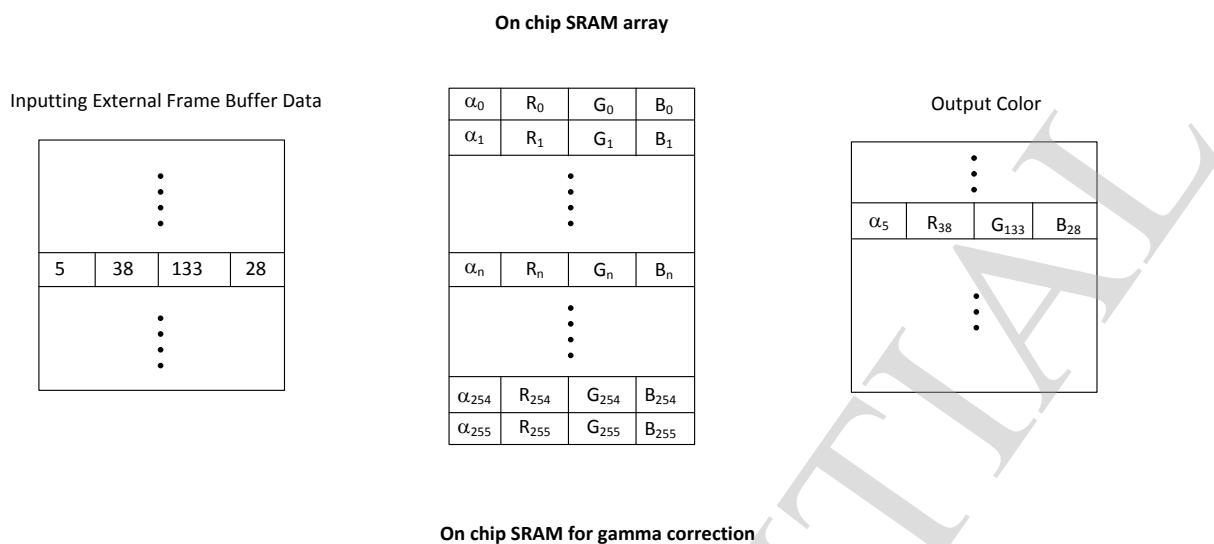
Offset: Pipe0:0x5000-0x53FF Pipe1:0x5400-0x57FF			Pipe palette color table SRAM block
Bit	Read/W rite	Default /Hex	Description
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	

			Blue value
--	--	--	------------

In this mode, RAM array is used for palette lookup table, each pixel in the layer frame buffer is treated as an index into the RAM array to select the actual color.

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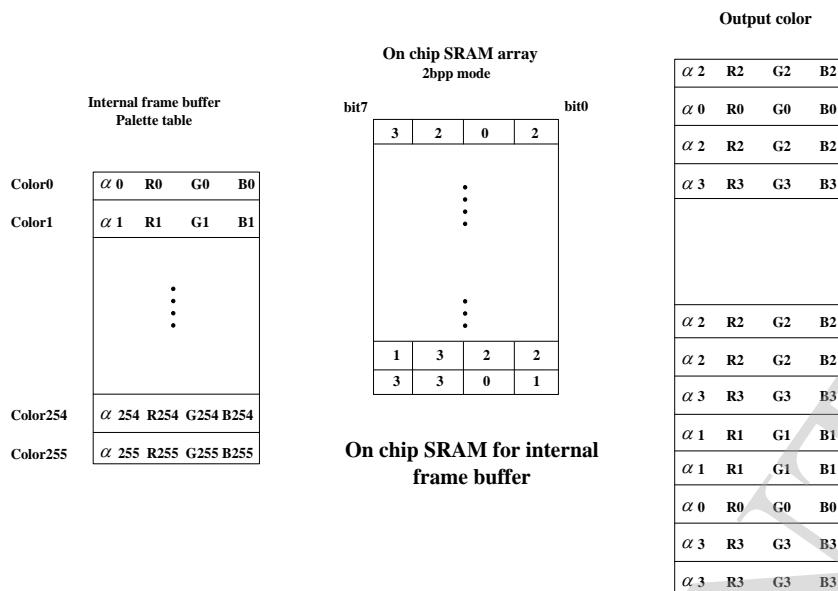
The following figure shows the RAM array used for palette lookup and the corresponding colors output.



INTERNAL FRAME BUFFER MODE PALETTE TABLE

Address:			Pipe palette table
Pipe0:0x5000-0x53FF			
Pipe1:0x5400-0x57FF			
Bit	Read/W rite	Default /Hex	Description
31:24	R/W	UDF	Alpha value
23:16	R/W	UDF	Red value
15:8	R/W	UDF	Green value
7:0	R/W	UDF	Blue value

The following figure shows the RAM array used for internal frame buffer mode and the corresponding colors output.



GAMMA CORRECTION MODE

Offset: 0x4400-0x47FF			DE-on chip SRAM block
Bit	Read/W rite	Default /Hex	Description
31:24	R/W	UDF	Alpha channel intensity
23:16	R/W	UDF	Red channel intensity
15:8	R/W	UDF	Green channel intensity
7:0	R/W	UDF	Blue channel intensity

In gamma correction mode, the RAM array is used for gamma correction, each pixel's alpha, red, green, and blue color component is treated as an index into the SRAM array. The corresponding alpha, red, green, or blue channel intensity value at that index is used in the actual color.

The following figure shows the RAM array used for gamma correction and the corresponding colors output.

On chip SRAM array

Inputting external
frame buffer data

5	38	133	28

Output color

α_0	R0	G0	B0
α_1	R1	G1	B1
α_n	Rn	Gn	Bn
α_{254}	R254	G254	B254
α_{255}	R255	G255	B255

On chip SRAM for gamma correction

5.5 MIPI DSI

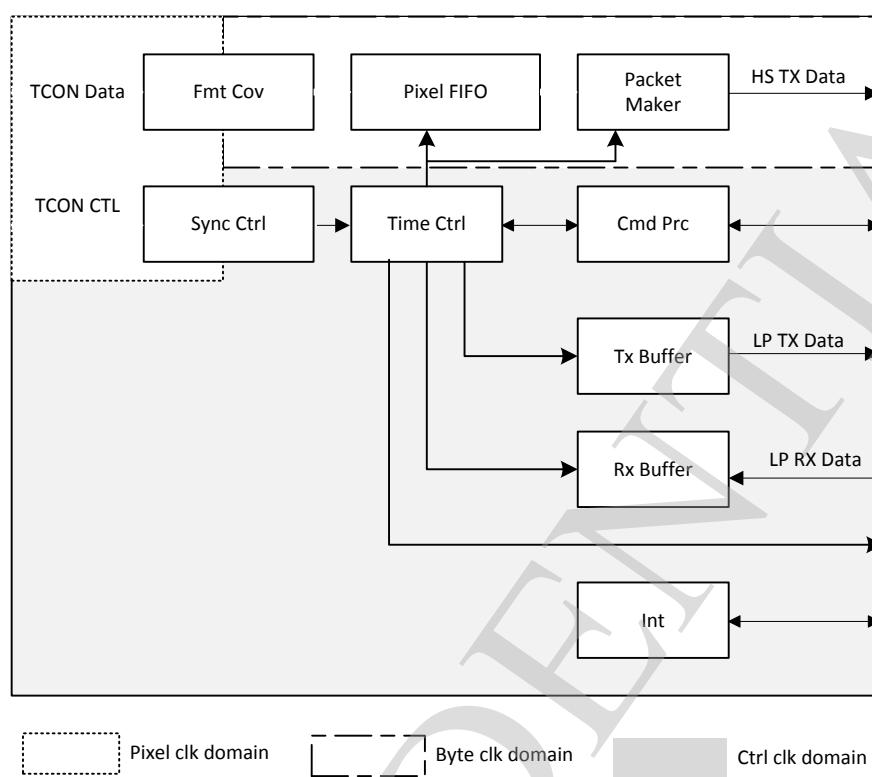
5.5.1 Overview

The Display Serial Interface (DSI) specifies the interface between a host processor and peripheral such as a display module. It builds on existing specs by adopting pixel formats and command set defined in MIPI alliance specs for Display Pixel Interface 2 (DPI-2) and Display Command Set (DCS).

The MIPI DSI of A23 processor features:

- Comply with MIPI DSI v1.01 and MIPI D-PHY v1.00
- 1 / 2 / 3 / 4 data lane configuration and up to 1Gbps per lane
- Support ECC, CRC generation and EOT package
- Support up to 1280x800@60fps with 4 data lanes
- Support command mode
- Support video mode
 - Non-burst mode with sync pulses
 - Non-burst mode with sync event
 - Burst mode
- Supported pixel formats: RGB888, RGB666, RGB666 packed, and RGB565
- Support MIPI DCS, bidirectional configuration in LP

5.5.2 Block Diagram



MIPI DSI Block Diagram

5.5.3 DSI Register List

Module Name	Base Address
DSI	0x01CA0000

Register Name	Offset	Description
DSI_CTL_REG	0x000	DSI Control Register
DSI_GINT0_REG	0x004	
DSI_GINT1_REG	0x008	
DSI_BASIC_CTL_REG	0x010	
DSI_BASIC_SIZE0_REG	0x014	
DSI_BASIC_SIZE1_REG	0x018	
DSI_PIXEL_CTL0_REG	0x080	
DSI_PIXEL_CTL1_REG	0x084	
DSI_PIXEL_PH_REG	0x090	
DSI_PIXEL_PD_REG	0x094	
DSI_PIXEL_PFO_REG	0x098	
DSI_PIXEL_PF1_REG	0x09C	
DSI_SYNC_HSS_REG	0x0B0	
DSI_SYNC_HSE_REG	0x0B4	
DSI_SYNC_VSS_REG	0x0B8	
DSI_SYNC_VSE_REG	0x0BC	
DSI_BLK_HSA0_REG	0x0C0	
DSI_BLK_HSA1_REG	0x0C4	
DSI_BLK_HBP0_REG	0x0C8	
DSI_BLK_HBP1_REG	0x0CC	
DSI_BLK_HFPO_REG	0x0D0	

DSI_BLK_HFP1_REG	0x0D4	
DSI_BLK_HBLK0_REG	0x0E0	
DSI_BLK_HBLK1_REG	0x0E4	
DSI_BLK_VBLK0_REG	0x0E8	
DSI_BLK_VBLK1_REG	0x0EC	
DSI_CMD_CTL_REG	0x200	
DSI_CMD_RX_REG	0x240+N*0x04	(N=0,1,2,3,4,5,6,7)
DSI_CMD_TX_REG	0x300+N*0x04	(N=0,1,2,...,63)
/	0x2E0	/
/	0x2E4	/
/	0x2F0	/
/	0x2F4	/
/	0x2F8	/
/	0xFF8	/

5.5.4 DSI Register Description

DSI_CTL_REG

Offset: 0x000			Register Name: DSI_CTL_REG
Bit	Read/Writ e	Default/H ex	Description
31: 1	/	/	/
0	R/W	0	DSI_En 0: disable 1: enable When it's disabled, the module will be reset to idle state.

DSI_GINT0_REG

Offset: 0x004			Register Name: DSI_GINT0_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 0	/	/	/
19	R/W	0	Video_Line_Int_Flag
18	R/W	0	Video_Vb_Int_Flag
17	R/W	0	Instru_Step_Flag
16	R/W	0	Instru_End_Flag
15:4	/	/	/
3	R/W	0	Video_Line_Int_En 0: disable 1: enable
2	R/W	0	Video_Vb_Int_En

			0: disable 1: enable
1	R/W	0	Instru_Step_En 0: disable 1: enable
0	R/W	0	Instru_End_En 0: disable 1: enable

DSI_GINT1_REG

Offset: 0x008			Register Name: DSI_GINT1_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0	Video_Line_Int_Num

DSI_BASIC_CTL0_REG

Offset: 0x010			Register Name: DSI_BASIC_CTL0_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28	R/W	0	Vsync_Existence 0: exit 1: no exit
27:1 9	/	/	/
18	R/W	0	HS_Eotp_En 0: disable

			1: enable enable eotp packet at the end of every HS transmission format: "08h" "0fh" "0fh" "01h"
17	R/W	0	CRC_En 0: disable 1: enable
16	R/W	0	ECC_En 0: disable 1: enable
15:1 3	/	/	/
12	R/W	0	FIFO_Gating 0: disable 1: enable Gating data from TCON, note that TCON data is gating in frame unit.
11	/	/	/
10	R/W	0	FIFO_Manual_Reset write '1' to reset all correlation FIFO, write'0' has no effect.
9:6	/	/	/
5:4	R/W	0	Src_Sel 00: tcon data 01: test data 1x: reservd write '1' to reset all correlation FIFO, write'0' has no effect.
3:1	/	/	/
0	R/W	0	Instru_En 0: disable 1: enable When instruction enable, dsi process from instruction0.

DSI_BASIC_CTL1_REG

Offset: 0x014			Register Name: DSI_BASIC_CTL1_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 2	R/W	0	reserved
11:4	R/W	0	Video_Start_Delay delay by lines, only valid in video mode
3	/	/	/
2	R/W	0	Video_Precision_Mode_Align 0: cut mode 1: fill mode
1	R/W	0	Video_Frame_Start 0: normal mode 1: precision mode set '0' start new frame by inst, set '1' start new frame by cntr.
0	R/W	0	DSI_Mode 0: command mode 1: video mode in video mode, enable timing define in basic size

DSI_BASIC_SIZE0_REG

Offset: 0x018			Register Name: DSI_BASIC_SIZE0_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 8	/	/	/
27:1 6	R/W	0	Video_VBP

15:1 2	/	/	/
11:0	R/W	0	Video_VSA

DSI_BASIC_SIZE1_REG

Offset: 0x01C			Register Name: DSI_BASIC_SIZE1_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 9	/	/	/
28:1 6	R/W	0	Video_VT
15:1 2	/	/	/
11:0	R/W	0	Video_VACT

DSI_PIXEL_CTL0_REG

Offset: 0x080			Register Name: DSI_PIXEL_CTL0_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 7	/	/	/
16	R/W	0	PD_Plug_Dis disable PD plug before pixel bytes
15:5	/	/	/
4	R/W	0	Pixel_Endian 0: LSB first 1: MSB first
3:0	R/W	0	Pixel_Format

			<p>Command mode</p> <p>0: 24bit (rgb888)</p> <p>1: 18bit (rgb666)</p> <p>2: 16bit (rgb565)</p> <p>3: 12bit (rgb444)</p> <p>4: 8bit (rgb332)</p> <p>5: 3bit (rgb111)</p> <p>Video mode</p> <p>8: 24bit(rgb888)</p> <p>9: 18bit(rgb666L)</p> <p>10: 18bit (rgb666)</p> <p>11: 16bit(rgb565)</p> <p>others: reserved</p>
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DSI_PIXEL_CTL1_REG

Offset: 0x084			Register Name: DSI_PIXEL_CTL1_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	/	/	/

DSI_PIXEL_PH_REG

Offset: 0x090			Register Name: DSI_PIXEL_PH_REG
Bit	Read/Writ e	Default/H ex	Description
31: 24	R/W	0	ECC only valid when DSI ECC is disable
23: 8	R/W	0	WC WC is byte numbers of PD in a pixel packet
7: 6	R/W	0	VC

Virtual Channel			
5:0	R/W	0	<p>DT</p> <p>video mode 24bit, set as "3eh"</p> <p>video mode L18bit, set as "2eh"</p> <p>video mode 18bit, set as "1eh"</p> <p>video mode 16bit, set as "0eh"</p> <p>command mode, set as "39h"</p>

DSI_PIXEL_PD_REG

Offset: 0x094			Register Name: DSI_PIXEL_PD_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	/	/	/
23:1 6	R/W	0	<p>PD_TranN</p> <p>Used in transmissions except 1st one, set as "3Ch", only valid when PD_Plug_Dis is set to '0'</p>
15:8	/	/	/
7:0	R/W	0	<p>PD_Tran0</p> <p>Used in 1st transmission, set as "2Ch", only valid when PD_Plug_Dis is set to '0'</p>

DSI_PIXEL_PFO_REG

Offset: 0x098			Register Name: DSI_PIXEL_PFO_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	/	/	/
15:0	R/W	0	<p>CRC_Force</p> <p>CRC force to this value, this value is only valid when CRC is disable</p>

DSI_PIXEL_PF1_REG

Offset: 0x09C			Register Name: DSI_PIXEL_PF1_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R/W	0xffff	CRC_Init_LineN CRC initial to this value in transmission except 1 st one, only valid when CRC is enabled.
15:0	R/W	0xffff	CRC_Init_Line0 CRC initial to this value in 1 st transmission every frame, only valid when CRC is enabled.

DSI_SYNC_HSS_REG

Offset: 0x0B0			Register Name: DSI_SYNC_HSS_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	R/W	0	ECC set as "12h"
23:1 6	R/W	0	D1 set as "00h"
15:8	R/W	0	D0 set as "00h"
7:6	R/W	0	VC Virtual Channel
5:0	R/W	0	DT HSS, set as "21h"

DSI_SYNC_HSE_REG

Offset: 0x0B4			Register Name: DSI_SYNC_HSE_REG
Bit	Read/Writ e	Default/H ex	Description

	e	ex	
31:2 4	R/W	0	ECC set as “01h”
23:1 6	R/W	0	D1 set as “00h”
15:8	R/W	0	D0 set as “00h”
7:6	R/W	0	VC Virtual Channel
5:0	R/W	0	DT HSE, set as “31h”

DSI_SYNC_VSS_REG

Offset: 0x0B8			Register Name: DSI_SYNC_VSS_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	R/W	0	ECC set as “07h”
23:1 6	R/W	0	D1 set as “00h”
15:8	R/W	0	D0 set as “00h”
7:6	R/W	0	VC Virtual Channel
5:0	R/W	0	DT VSS, set as “01h”

DSI_SYNC_VSE_REG

Offset: 0x0BC	Register Name: DSI_SYNC_VSE_REG
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Bit	Read/Writ e	Default/H ex	Description
31:2 4	R/W	0	ECC set as "14h"
23:1 6	R/W	0	D1 set as "00h"
15:8	R/W	0	D0 set as "00h"
7:6	R/W	0	VC Virtual Channel
5:0	R/W	0	DT VSE, set as "11h"

DSI_BLK_HSA0_REG

Offset: 0x0C0			Register Name: DSI_BLK_HSA0_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0	HSA_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet

DSI_BLK_HSA1_REG

Offset: 0x0C4			Register Name: DSI_BLK_HSA1_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R/W	0	HSA_PF
15:8	/	/	/
7:0	R/W	0	HSA_PD

DSI_BLK_HBPO_REG

Offset: 0x0C8			Register Name: DSI_BLK_HBPO_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0	HBP_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet

DSI_BLK_HBP1_REG

Offset: 0x0CC			Register Name: DSI_BLK_HBP1_REG
Bit	Read/Writ e	Default/H ex	Description
31: 16	R/W	0	HBP_PF
15:8	/	/	/
7:0	R/W	0	HBP_PD

DSI_BLK_HFPO_REG

Offset: 0x0D0			Register Name: DSI_BLK_HFPO_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0	HFP_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet

DSI_BLK_HFP1_REG

Offset: 0x0D4			Register Name: DSI_BLK_HFP1_REG
Bit	Read/Writ e	Default/H ex	Description

31:1 6	R/W	0	HFP_PF
15:8	/	/	/
7:0	R/W	0	HFP_PD

DSI_BLK_HBLK0_REG

Offset: 0x0E0			Register Name: DSI_BLK_HBLK0_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0	HBLK_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet

DSI_BLK_HBLK1_REG

Offset: 0x0E4			Register Name: DSI_HBLK_BLK1_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R/W	0	HBLK_PF
15:8	/	/	/
7:0	R/W	0	HBLK_PD

DSI_BLK_VBLK0_REG

Offset: 0x0E8			Register Name: DSI_BLK_VBLK0_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0	VBLK_PH Note that bit23:8 is WC, define byte numbers of PD in a blank packet

DSI_BLK_VBLK1_REG

Offset: 0x0EC			Register Name: DSI_BLK_VBLK1_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 6	R/W	0	VBLK_PF
15:8	/	/	/
7:0	R/W	0	VBLK_PD

DSI_CMD_CTL_REG

Offset: 0x200			Register Name: DSI_CMD_CTL_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 5	/	/	/
26	R/W	0	RX_Overflow 1: rx data is overflow register buffer Note: Write'1' to clear this bit. Write'0' has no effect.
25	R/W	0	RX_Flag 1: rx has happened Note: Write'1' to clear this bit. Write'0' has no effect.
24	R	0	RX_Status 0: rx is finish 1: rx is pending
20:1 6	R	0	RX_Size (RX_Size+1) is number of bytes in the last rx.
15:9	/	/	/
9	R/W	0	TX_Flag 1: tx has happened Note: Write'1' to clear this bit. Write'0' has no effect.

8	R	0	TX_Status 0: tx is finish 1: tx is pending
7:0	R/W	0	TX_Size (TX_Size+1) is number of bytes ready to tx

DSI_CMD_RX_REG

Offset: 0x240+N*0x04 (N=0,1,2,3,4,5,6,7)			Register Name: DSI_CMD_RX_REG
Bit	Read/Writ e	Default/H ex	Description
31: 0	R/W	0	Data Bit: 31:24 23:16 15:8 7:0 N=0: Byte03 Byte02 Byte01 Byte00 N=1: Byte07 Byte06 Byte05 Byte04 N=2: Byte11 Byte10 Byte09 Byte08 N=3: Byte15 Byte14 Byte13 Byte12 N=4: Byte19 Byte18 Byte17 Byte16 N=5: Byte23 Byte22 Byte21 Byte20 N=6: Byte27 Byte26 Byte25 Byte24 N=7: Byte31 Byte30 Byte29 Byte28 Data from rx, only in LPDT Only read when RX_Flag is set. No way to clear this FIFO.

DSI_CMD_TX_REG

Offset: 0x300+N*0x04 (N=0,1,2,...255)			Register Name: DSI_CMD_TX_REG
Bit	Read/Writ e	Default/H ex	Description
31:	R/W	0	Data

0		Bit: 31:24 23:16 15:8 7:0 N=0: Byte03 Byte02 Byte01 Byte00 N=1: Byte07 Byte06 Byte05 Byte04 N=2: Byte11 Byte10 Byte09 Byte08 N=3: Byte15 Byte14 Byte13 Byte12 N=4: Byte19 Byte18 Byte17 Byte16 N=5: Byte23 Byte22 Byte21 Byte20 N=6: Byte27 Byte26 Byte25 Byte24 N=7: Byte31 Byte30 Byte29 Byte28 Data for tx, transmission in HS and LPDT, defined by INST_REG
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5.6 IEP

The IEP (Image Enhancement Processor) of A23 processor includes CMU, DRC, and write back controller, which can be used to adjust the dynamic range of images.

5.6.1 CMU

Color Management Unit (CMU) is introduced in A23 platform to adjust colors from DEFE so that a better vivid vision effect can be achieved, and it is also capable of flesh tones enhancement.

It features:

- Support RGB888 input and output format
- Support window clipping up to 8192x8192 pixels
- Support global and local adjustment for hue/ saturation/ brightness in HSV space
- Support red/green/blue/cyan/magenta/yellow/flesh areas modifying in local adjustment mode

5.6.2 DRC

DRC (Dynamic Range Controller) adjusts the image mapping curve according to the histogram frame by frame. The control function can be defined by the software driver according to the application. A typical application is content-based backlight control.

It features:

- Support 1280x800 input/output
- Support HISTOGRAM and DRC in YUV or HSV color space

5.6.3 Write-Back Controller

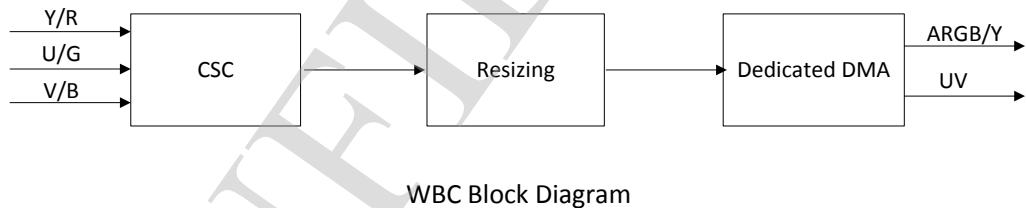
OVERVIEW

Write-back Controller is a circuit for capturing data between display engine and LCD controller. Data will be written back to SDRAM.

The Write-back controller includes following features:

- Support 1280x800 pixels write-back
- Support source cropping
- Support RGB888 and YUV444 format input
- Support write-back linestride setting
- Support interleaved ARGB8888 and NV12/NV21 output
- Support down sample to 1/2X, 1/4X
- Color space converter included

WBC BLOCK DIAGRAM



WBC Block Diagram

WRITE-BACK CONTROLLER REGISTER LIST

Module name	Base address
Write-back Controller	0x01E7 0200

Register name	Offset	Description
WBC_GCTRL_REG	0x000	Module General Control Register
WBC_SIZE_REG	0x004	Input Size Register
WBC_CROP_COORD_REG	0x008	Cropping Coordinate Register
WBC_CROP_SIZE_REG	0x00c	Cropping Size Register
WBC_CH0_ADDR_REG	0x010	Write-Back Channel 0 Address Register
WBC_CH1_ADDR_REG	0x014	Write-Back Channel 1 Address Register
WBC_CH0_LSTRD_REG	0x020	Write-Back Channel 0 Linestride Register
WBC_CH1_LSTRD_REG	0x024	Write-Back Channel 1 Linestride Register
WBC_RESIZER_REG	0x030	Resizer Setting Register
WBC_FORMAT_REG	0x034	Output Format Register
WBC_INT_REG	0x038	Interrupt Control Register
WBC_STATUS_REG	0x03c	Module Status Register
WBC_BURST_REG	0x040	DMA Burst Setting
WBC_CSC_COEF00_REG	0x050	CSC Coefficient 00 Register
WBC_CSC_COEF01_REG	0x054	CSC Coefficient 01 Register
WBC_CSC_COEF02_REG	0x058	CSC Coefficient 02 Register
WBC_CSC_COEF03_REG	0x05c	CSC Coefficient 03 Register
WBC_CSC_COEF10_REG	0x060	CSC Coefficient 10 Register
WBC_CSC_COEF11_REG	0x064	CSC Coefficient 11 Register
WBC_CSC_COEF12_REG	0x068	CSC Coefficient 12 Register
WBC_CSC_COEF13_REG	0x06c	CSC Coefficient 13 Register
WBC_CSC_COEF20_REG	0x070	CSC Coefficient 20 Register

WBC_CSC_COEF21_REG	0x074	CSC Coefficient 21 Register
WBC_CSC_COEF22_REG	0x078	CSC Coefficient 22 Register
WBC_CSC_COEF23_REG	0x07c	CSC Coefficient 23 Register

CONFIDENTIAL

WRITE-BACK CONTROLLER REGISTER DESCRIPTION

MODULE GENERAL CONTROL REGISTER

Offset: 0X000			Register name: WBC_GCTRL_REG
Bit	Read/Writ e	Default/H ex	Description
31	R/W	0	<p>BIST_EN</p> <p>BIST enable</p> <p>0: disable</p> <p>1: enable</p>
30:21	/	/	/
20	R/W	0	<p>WB_STOP_TIMING</p> <p>When error occurs, module stop accessing dram or not.</p> <p>0: Write-back DONOT stop.</p> <p>1: Write-back stops.</p>
19:17	/	/	/
16	R/W	0	<p>WB_EN</p> <p>Start write-back process.</p> <p>0: Enable</p> <p>1: Disable</p> <p>If WB_MODE set to 0, the write back process will start when WB_EN is set and a new frame processing begins. Otherwise, if WB_MODE set to 1, write back process will start immediately. The bit will be self-cleared when writing-back frame process starts.</p>
15:13	/	/	/

12	R/W	0	IN_PORT_SEL Input port selection 0: port 0 (DRC input) 1: port 1 (DRC output)
11:09	/	/	/
08	R/W	0	WB_MODE Write-back mode setting 0: Capture mode: Write-back and display simultaneously.(support port 0 and port 1) 1: Write-back only mode: Write-back to dram only, display will disable.(support port 1 only)
07:05	/	/	/
04	R/W	0	REG_RDY_EN Buffered registers configuration ready switch 0: Not ready 1: Registers configuration ready Note: When the new frame start, the bit will also be self-cleared.
03:01	/	/	/
00	R/W	0	EN Module enable 0: Disable 1: Enable

INPUT SIZE REGISTER

Offset: 0X004			Register name: WBC_SIZE_REG
Bit	Read/Writ e	Default/H ex	Description
31:27	/	/	/
26:16	R/W	0	<p>HEIGHT</p> <p>Input height</p> <p>The real input height = The value of these bits + 1.</p>
15:11	/	/	/
10:00	R/W	0	<p>WIDTH</p> <p>Input width</p> <p>The real input width = The value of these bits + 1.</p>

CROPPING COORDINATE REGISTER

Offset: 0X008			Register name: WBC_CROP_COORD_REG
Bit	Read/Writ e	Default/H ex	Description
31:27	/	/	/
26:16	R/W	0	<p>CROP_TOP</p> <p>Cropping top position</p> <p>Top position is the left-top y coordinate of input window in pixels</p>
15:11	/	/	/
10:00	R/W	0	CROP_LEFT

			Cropping left position Left position is left-top x coordinate of input window in pixels
--	--	--	--

CROPPING SIZE REGISTER

Offset: 0X00c			Register name: WBC_CROP_SIZE_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 7	/	/	/
26:1 6	R/W	0	<p>CROP_HEIGHT</p> <p>Cropping region height</p> <p>The real cropping region height = the value of these bits + 1.</p>
15:1 1	/	/	/
10:0 0	R/W	0	<p>CROP_WIDTH</p> <p>Cropping region width</p> <p>The real cropping region width = the value of these bits + 1.</p>

WRITE-BACK CHANNEL 0 ADDRESS REGISTER

Offset: 0X010			Register name: WBC_CH0_ADDR_REG
Bit	Read/Writ e	Default/H ex	Description
31:0 0	R/W	0	<p>ADDR</p> <p>Write-back channel 0 address in BYTE.</p> <p>When output format is ARGB, ADDR must 4 bytes aligning.</p>

WRITE-BACK CHANNEL 1 ADDRESS REGISTER

Offset: 0X014	Register name: WBC_CH1_ADDR_REG
---------------	---------------------------------

Bit	Read/Writ e	Default/H ex	Description
31:0 0	R/W	0	<p>ADDR</p> <p>Write-back channel 1 address in BYTE.</p> <p>When output format is ARGB, ADDR must 4 bytes aligning.</p>

WRITE-BACK CHANNEL 0 LINESTRIDE REGISTER

Offset: 0X020			Register name: WBC_CH0_LSTRD_REG
Bit	Read/Writ e	Default/H ex	Description
31:0 0	R/W	0	<p>LSTRD</p> <p>Write-back channel 0 linestride in BYTE.</p> <p>When output format is ARGB, LSTRD must 4 bytes aligning.</p>

WRITE-BACK CHANNEL 1 LINESTRIDE REGISTER

Offset: 0X024			Register name: WBC_CH1_LSTRD_REG
Bit	Read/Writ e	Default/H ex	Description
31:0 0	R/W	0	<p>LSTRD</p> <p>Write-back channel 1 linestride in BYTE.</p> <p>When output format is ARGB, LSTRD must 4 bytes aligning.</p>

RESIZER SETTING REGISTER

Offset: 0X030			Register name: WBC_RESIZER_REG
Bit	Read/Writ e	Default/H ex	Description
31:0 2	/	/	/
01:0 0	R/W	0	FACTOR

			Output down sample factor. 0: 1X 1: 1/2X 2: 1/4X 3: reserved
--	--	--	--

OUTPUT FORMAT REGISTER

Offset: 0X034			Register name: WBC_FORMAT_REG
Bit	Read/Writ e	Default/H ex	Description
31:0	/	/	/
04	R/W	0	<p>PS</p> <p>Output format pixel sequence</p> <p>In ARGB8888 data mode:</p> <p>0: BGRA(bit31 to bit0)</p> <p>1: ARGB</p> <p>In UV combined data mode: (UV component)</p> <p>00: V1U1V0U0</p> <p>01: U1V1U0V0</p>
03:0	/	/	/
00	R/W	0	<p>FORMAT</p> <p>Output format selection</p> <p>0: Interleaved ARGB8888 (alpha is always 0xff)</p> <p>1: Non tile-based UV combined YUV420.</p>

INTERRUPT CONTROL REGISTER

Offset: 0X038			Register name: WBC_INT_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 7	/	/	/
16	R/W	0	<p>WB_END_INT_TIMING</p> <p>Timing when write-back end interrupt sends</p> <p>0: last data writing to SDRAM</p> <p>1: last command sending to mbus</p>
15:0 7	/	/	/
06	R/W	0	<p>WB_UNFINISH_INT_EN</p> <p>Write-back unfinish error interrupt enable</p> <p>0: Enable</p> <p>1: Disable</p>
05	R/W	0	<p>WB_FIFO_OVF_INT_EN</p> <p>Write-back FIFO overflow error interrupt enable</p> <p>0: Enable</p> <p>1: Disable</p>
04	R/W	0	<p>WB_FIFO_EMPTY_INT_EN</p> <p>Write-back FIFO empty error interrupt enable</p> <p>0: Enable</p> <p>1: Disable</p>
03:0 1	/	/	/
00	R/W	0	WB_END_INT_EN

			Write-back end interrupt enable 0: Enable 1: Disable
--	--	--	--

MODULE STATUS REGISTER

Offset: 0X03c			Register name: WBC_STATUS_REG
Bit	Read/Writ e	Default/H ex	Description
31:0 9	/	/	/
08	R	0	<p>WB_BUSY</p> <p>Write-back process status 0: write-back end or write-back disable 1: write-back in process</p> <p>This flag indicates that a full frame has not been written back to the memory. The bit will be set when write-back enable bit is set, and be cleared when write-back process end. When module restarts, this bit will be also cleared. When error occur</p>
07	/	/	/
06	R/W	0	<p>WB_UNFINISH_ERR</p> <p>Write-back unfinish error status 0: No error 1: Error</p> <p>Write 1 to clear. Module restarts, this bit will be also cleared.</p>
05	R/W	0	WB_FIFO_OVF_ERR
			Write-back FIFO overflow error status

			<p>0: No error 1: Error</p> <p>Write 1 to clear. Module restarts, this bit will be also cleared.</p>
04	R/W	0	<p>WB_FIFO_EMPTY_ERR</p> <p>Write-back FIFO empty error status 0: No error 1: Error</p> <p>Write 1 to clear. Module restarts, this bit will be also cleared.</p>
03:0 1	/	/	/
00	R/W	0	<p>WB_END_FLAG</p> <p>Write-back process finish flag 0: write-back unfinished 1: write-back finished</p> <p>This flag indicates that a full frame has not been written back to the memory. The bit will be set when write-back process end. Write 1 to clear. Module restarts, this bit will be also cleared.</p>

DMA BURST SETTING

Offset: 0x040			Register Name: WBC_DMA_REG
Bit	Read/Writ e	Default/H ex	Description
31:0 2	/	/	/
01:0 0	R/W	0x0	BURST_LEN

			DMA burst length 0: 16 words 1: 32 words 2: 64 words 3: 128 words
--	--	--	---

CSC COEFFICIENT 00 REGISTER

Offset: 0x050			Register Name: WBC_CSC_COEF00_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0 0	R/W	0x0	COEF the Y/R coefficient the value equals to coefficient* 2^{10}

CSC COEFFICIENT 01 REGISTER

Offset: 0x054			Register Name: WBC_CSC_COEF01_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0 0	R/W	0x0	COEF the Y/R coefficient the value equals to coefficient* 2^{10}

CSC COEFFICIENT 02 REGISTER

Offset: 0x058			Register Name: WBC_CSC_COEF02_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the Y/R coefficient the value equals to coefficient* 2^{10}

CSC COEFFICIENT 03 REGISTER

Offset: 0x05c			Register Name: WBC_CSC_COEF03_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 4	/	/	/
13:0	R/W	0x0	CONT the Y/R constant the value equals to coefficient* 2^4

CSC COEFFICIENT 10 REGISTER

Offset: 0x060			Register Name: WBC_CSC_COEF10_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the U/G coefficient

			the value equals to coefficient*2 ¹⁰
--	--	--	---

CSC COEFFICIENT 11 REGISTER

Offset: 0x064			Register Name: WBC_CSC_COEF11_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the U/G coefficient the value equals to coefficient*2 ¹⁰

CSC COEFFICIENT 12 REGISTER

Offset: 0x068			Register Name: WBC_CSC_COEF12_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the U/G coefficient the value equals to coefficient*2 ¹⁰

CSC COEFFICIENT 13 REGISTER

Offset: 0x06c			Register Name: WBC_CSC_COEF13_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 4	/	/	/
13:0	R/W	0x0	CONT

0			the U/G constant the value equals to coefficient* 2^4
---	--	--	--

CSC COEFFICIENT 20 REGISTER

Offset: 0x070			Register Name: WBC_CSC_COEF20_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient* 2^{10}

CSC COEFFICIENT 22 REGISTER

Offset: 0x074			Register Name: WBC_CSC_COEF21_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 3	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient* 2^{10}

CSC COEFFICIENT 22 REGISTER

Offset: 0x078			Register Name: WBC_CSC_COEF22_REG
Bit	Read/Writ e	Default/H ex	Description

31:1 3	/	/	/
12:0	R/W	0x0	COEF the V/B coefficient the value equals to coefficient* 2^{10}

CSC COEFFICIENT 23 REGISTER

Offset: 0x07c			Register Name: WBC_CSC_COEF23_REG
Bit	Read/Writ e	Default/H ex	Description
31:1 4	/	/	/
13:0 0	R/W	0x0	CONT the V/B constant the value equals to coefficient* 2^4

Chapter 6

Video Input

This chapter details the video input system of A23 processor from following perspectives:

- CSI

CONFIDENTIAL

6.1 CSI

The A23 processor comes with one parallel CMOS sensor interface that supports up to 5M pixels. It also supports dual-channel output for display and encoding.

6.1.1 Features

- Support 8-bit YUV422 CMOS sensor interface
- Support CCIR656 protocol for NTSC and PAL
- Support multi-channel ITU-R BT656 time-multiplexed format
- Support still capture resolution up to 4Kx4K
- Support video capture resolution up to 1080p@60fps
- Support dual-channel buffer output for display and encoding
- Parsing interleaved YCbCr 422 data into planar or special tile-based Y, Cb, Cr output to memory
- Parsing YCbCr 420 data into planar or special tile-based Y, Cb, Cr output to memory
- Parsing interlaced data into field or frame output to memory
- Support received data double buffer
- Support crop and scale
- Support H/V-flip and rotation
- Frame rate counter statistic

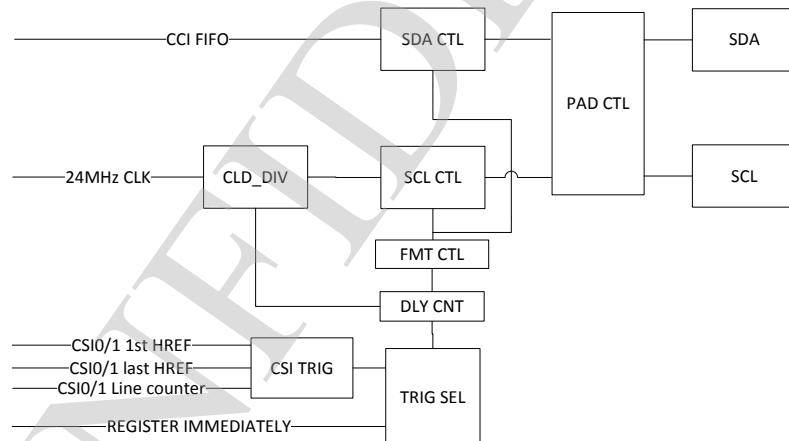
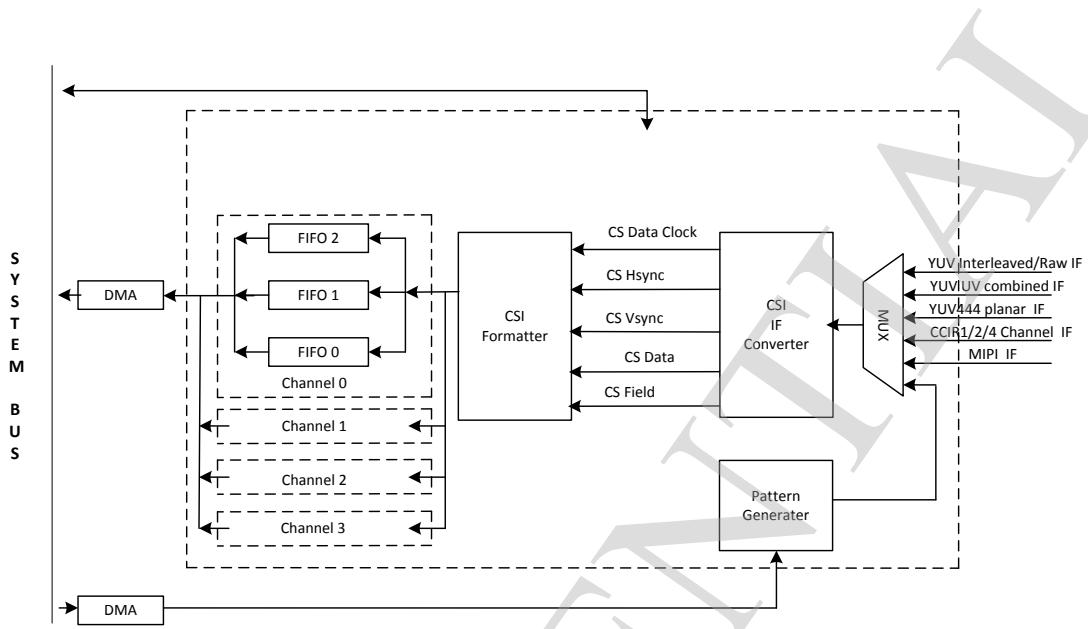
CCI

- Compatible with I2C transmission in 7-bit slave ID and 1-bit R/W
- Automatic transmission
- Support 0/8/16/32- bit register address
- Support 8/16/32- bit data
- Support 64-byte FIFO input CCI data

- Synchronized with CSI signal and delay trigger supported
- Support repeated transmission with sync signal

CONFIDENTIAL

6.1.2 Block Diagram



CCI Block Diagram

6.1.3 CSI Function Description

CSI FIFO DISTRIBUTION

Interface	YUYV422 Interleaved/RAW			YUV422 UV Combined	YUV444 Planar	YUV444 Planar to YUV422 UV Combined
Input format	YUV422		Raw	Raw	Raw	Raw
Output format	Planar	UV combined / MB	Raw/RGB /PRGB	Raw	Raw	Raw
CH0_FIFO0	Y pixel data	Y pixel data	All pixels data	Y pixel data	Y pixel data	Y pixel data
CH0_FIFO1	Cb (U) pixel data	Cb (U) Cr (V) pixel data	-	-	-	-
CH0_FIFO2	Cr (V) pixel data	-	-	-	-	-
CH1_FIFO0	-	-	-	Cb (U) Cr (V) pixel data	Cb (U) pixel data	Cb (U) Cr (V) pixel data
CH2_FIFO0	-	-	-	-	Cr(V) pixel data	-

Interface	BT656 Interface			Channels
Input format	YUV422			

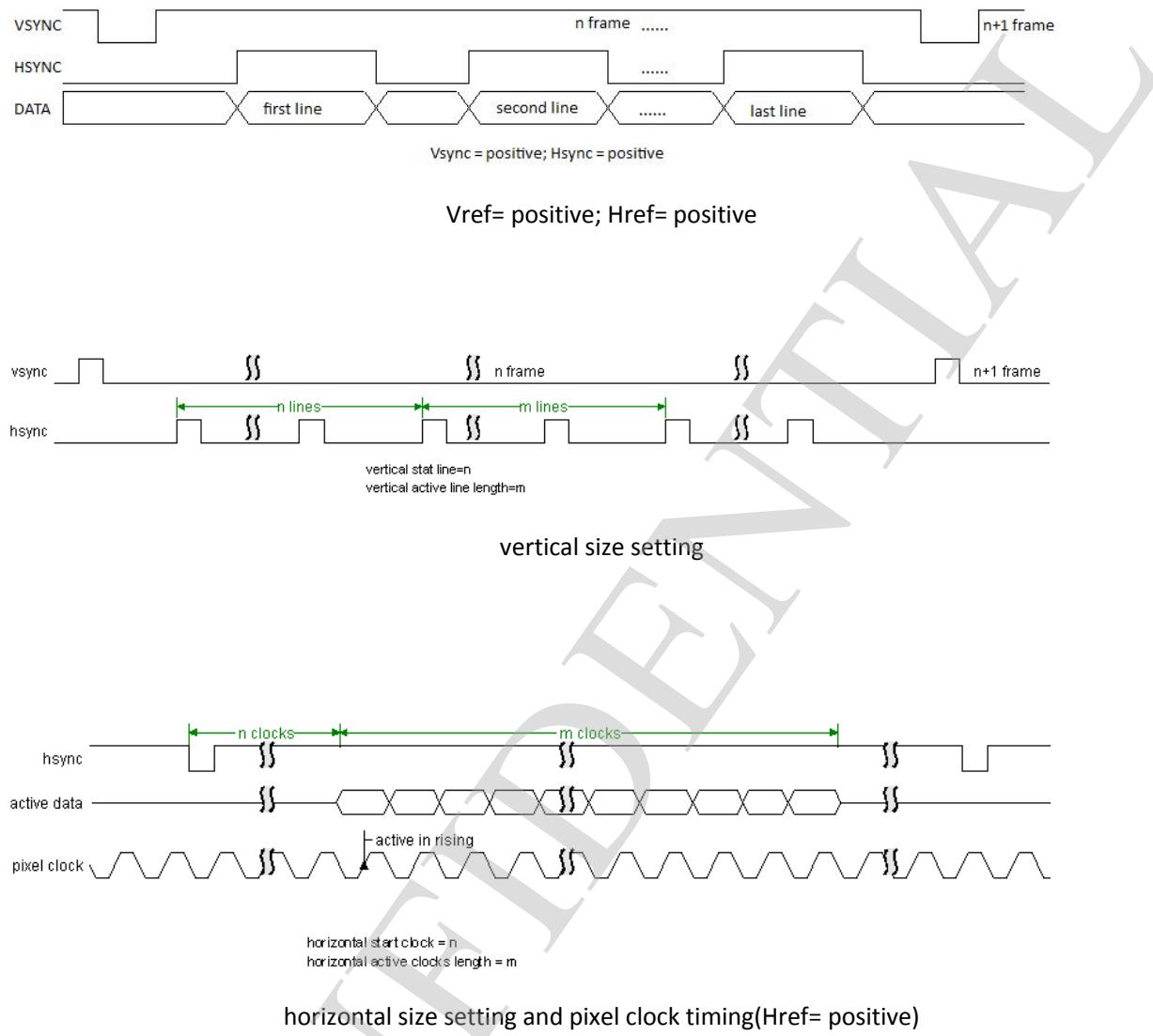
Output format	Planar	UV combined/ MB			
CH0_FIFO0	Y	Y	1	2	4
CH0_FIFO1	Cb (U)	CbCr (UV)			
CH0_FIFO2	Cr (V)	-			
CH1_FIFO0	Y	Y	-		
CH1_FIFO1	Cb (U)	CbCr (UV)			
CH1_FIFO2	Cr (V)	-			
CH2_FIFO0	Y	Y	-		
CH2_FIFO1	Cb (U)	CbCr (UV)			
CH2_FIFO2	Cr (V)	-			
CH3_FIFO0	Y	Y			
CH3_FIFO1	Cb (U)	CbCr (UV)			
CH3_FIFO2	Cr (V)	-			

Interface	MIPI Interface			Channels			
Input format	YUV422/YUV420		Raw				
Output format	Planar	UV combined/ MB	Pass-Through /Padding				
CH0_FIFO0	Y	Y	All pixels data	1	2	3	4
CH0_FIFO1	Cb (U)	CbCr	-				

		(UV)					
CH0_FIFO2	Cr (V)	-	-				
CH1_FIFO0	Y	Y	All pixels data	-			
CH1_FIFO1	Cb (U)	CbCr (UV)	-				
CH1_FIFO2	Cr (V)	-	-				
CH2_FIFO0	Y	Y	All pixels data	-			
CH2_FIFO1	Cb (U)	CbCr (UV)	-				
CH2_FIFO2	Cr (V)	-	-				
CH3_FIFO0	Y	Y	All pixels data	-			
CH3_FIFO1	Cb (U)	CbCr (UV)	-				
CH3_FIFO2	Cr (V)	-	-				

TIMING

CSI timing



CCIR656 HEADER CODE

CCIR656 Header Data Bit Definition

Data Bit	First Word(0xFF)	Second Word(0x00)	Third Word(0x00)	Fourth Word
CS D[9] (MSB)	1	0	0	1
CS D[8]	1	0	0	F
CS D[7]	1	0	0	V
CS D[6]	1	0	0	H
CS D[5]	1	0	0	P3
CS D[4]	1	0	0	P2
CS D[3]	1	0	0	P1
CS D[2]	1	0	0	P0
CS D[1]	x	x	x	x
CS D[0]	x	x	x	x

For compatibility with an 8-bit interface, CS D[1] and CS D[0] are not defined.

Decode	F	V	H	P3	P2	P1	P0
Field 1 start of active video (SAV)	0	0	0	0	0	0	0
Field 1 end of active video (EAV)	0	0	1	1	1	0	1
Field 1 SAV (digital blanking)	0	1	0	1	0	1	1
Field 1 EAV (digital blanking)	0	1	1	0	1	1	0
Field 2 SAV	1	0	0	0	1	1	1
Field 2 EAV	1	0	1	1	0	1	0
Field 2 SAV (digital blanking)	1	1	0	1	1	0	0
Field 2 EAV (digital blanking)	1	1	1	0	0	0	1

OFFSET DEFINITION

Offset in horizontal and vertical can be added when receiving image. Unit is pixel.

For YUV422 format, pixel unit is a YU/YV combination.

For YUV420 format, pixel unit is a YU/YV combination in YC line, and only a Y in Y line.

For Bayer_raw format, pixel unit is a R/G/B single component.

For RGB565, pixel unit is two bytes of RGB565 package.

For RGB888, pixel unit is three bytes of RGB combination.

SCALE DEFINITION

All channel input image can be decimated to its quarter size if **QUART_EN** is set to 1.

When using this function, horizontal input components should be multiples of the components in a unit, and vertical lines should be multiples of the height of a unit.

Specific components and lines will be dropped except the blue ones as follows.

Component sequence in a unit may changed, but unit dropping position will not changed.

BAYER_RAW(raw_8/raw_10/raw_12):

GRGRGRGR...

BGBGBGBG...

GRGRGRGR...

BGBGBGBG...

GRGRGRGR...

BGBGBGBG...

GRGRGRGR...

BGBGBGBG...

RGB888:

RGBRGB...

RGBRGB...

RGB565:

565565...

565565...

YUV422(8bit/10bit in field mode):

YUYVYUYV...

YUYVYUYV...

YUYVYUYV...

YUYVYUYV...

YUV422(8bit/10bit in frame mode):

YUYVYUYV... → odd field

YUYVYUYV... → even field

YUYVYUYV...

YUYVYUYV...

YUV420(8bit/10bit):

YC line: YUYVYUYV...

Y line: YYYY...

YC line: YUYVYUYV...

Y line: YYYY...

FLIP DEFINITION

Both horizontal and vertical flip are supported at the same time. This function is implemented in the process of each FIFO writing data to memory, only flipping the data of separate FIFO, not changing component to FIFO distribution.

If horizontal flip is enabled, one or more pixels will be took as a unit:

For YUV format, a unit of $Y_0U_0Y_1V_1$ will parser and flip the Y component in one channel, and UV will be treated as a whole. In planar output mode, U and V will be flipped separately. In UV combined output mode, UV will be flipped as a whole. So, a sequence of $Y_1U_0Y_0V_1$ will be.

For Bayer_raw format, situation is much like. A GR/BG sequence will be changed to BG/RG. A unit of square has four pixels.

For RGB565/RGB888, one unit of two/three bytes of component will be flipped with original sequence.

CAMERA COMMUNICATION INTERFACE

The CCI module support master mode i2c-compatible single read and write access to camera and related devices.

It reads a series of packet from FIFO(accessed by registers) and transmit with the format defined in specific register(or packet data).

In compact mode, format register define the slave ID, R/W flag, register address width (0/8/16/32...bit), data width (8/16/32...bit) and access counter.

In complete mode, all data and format will be loaded from memory packet.

The access counter should be set to N(N> 0), and it will read N packets from FIFO. The total bytes should not exceed 64 for FIFO input mode.

COMPACT MODE

	MEM START						MEM END	
	BYTE0	BYTE1	BYTE2	BYTE3	BYTEn		
8_8 RD	Reg0	Data0_rd	Reg1	Data1_rd		
8_8 WR	Reg0	Data0	Reg1	Data1		
16_8 RD	Reg0_high	Reg0_low	Data0_rd	Reg1_high		
16_8 WR	Reg0_high	Reg0_low	Data0	Reg1_high		

← Total bytes = Packet size * Counter of packet →

A packet

COMPLETE MODE

	BYTE0	BYTE1	BYTE2	BYTE3	BYTEn		
8_8 RD	Slave_id	Reg_w/Dat_w	Reg0	Data0		
8_8 WR	Slave_id	Reg_w/Dat_w	Reg0	Data0		
16_8 RD	Slave_id	Reg_w/Dat_w	Reg0_high	Reg0_low	Data0	...		
16_8 WR	Slave_id	Reg_w/Dat_w	Reg0_high	Reg0_low	Data0	...		

← Total bytes = Packet size * Counter of packet →

A packet

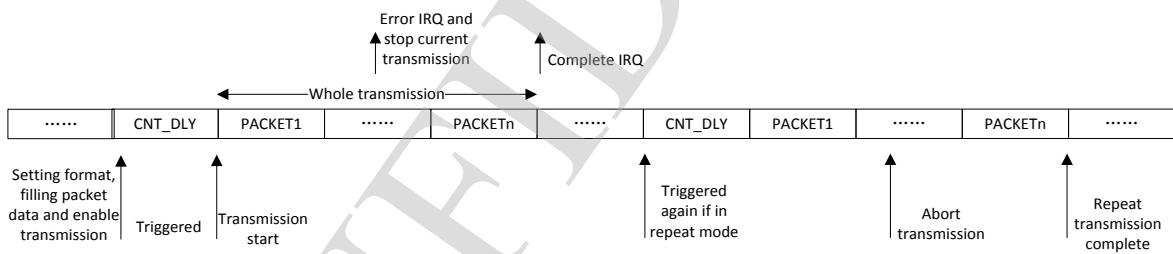
A packet is several bytes filled with register address and data(if in complete mode, slave id and width should

be filled too) as the i2c access sequence defined. That is, the low address byte will be transmitted/received first. Bytes will be sent in write access, while some address will be written back with the data received in read access.

Single Access protocol supported by CCI

	RS	or	P+S	is optional	X	is driven by CCI	X	is driven by slave
8_8 RD	S	ID+W	ACK	Reg0	RS	ID+R	ACK	Data0_rd NA CK
8_8 WR	S	ID+W	ACK	Reg0	ACK	Data0_wr	NA CK	
16_8 RD	S	ID+W	ACK	Reg0_high	ACK	Reg0_low	RS	ID+R ACK Data0_rd NA CK
16_8 WR	S	ID+W	ACK	Reg0_high	ACK	Reg0_low	ACK	Data0_w r NA CK
0_16 RD	S	ID+R	ACK	Data0_rd_high	ACK	Data0_rd_low	NA CK	
0_16 WR	S	ID+W	ACK	Data0_w r_high	ACK	Data0_w r_low	NA CK	

After set the execution bit, the module will do the transmission automatically and return the result - success or fail. If any access fail, the whole transmission will be stopped and returns the number when it fail in the access counter.



6.1.4 CSI Register List

Module Name	Base Address
CSI	0x01CB0000

Register Name	Offset	Register name
CSI_EN_REG	0X0000	CSI Enable register
CSI_IF_CFG_REG	0X0004	CSI Interface Configuration Register
CSI_CAP_REG	0X0008	CSI Capture Register
CSI_SYNC_CNT_REG	0X000C	CSI Synchronization Counter Register
CSI_FIFO_THRS_REG	0X0010	CSI FIFO Threshold Register
CSI_FIFO_STAT_REG	0X0014	CSI FIFO Statistic Register
CSI_PCLK_STAT_REG	0X0018	CSI PCLK Statistic Register
CSI_PTN_LEN_REG	0X0030	CSI Pattern Generation Length register
CSI_PTN_ADDR_REG	0X0034	CSI Pattern Generation Address register
CSI_VER_REG	0X003C	CSI Version Register
CSI_CO_CFG_REG	0X0044	CSI Channel_0 configuration register
CSI_CO_SCALE_REG	0X004C	CSI Channel_0 scale register
CSI_CO_F0_BUFA_REG	0X0050	CSI Channel_0 FIFO 0 output buffer-A address register
CSI_CO_F1_BUFA_REG	0X0058	CSI Channel_0 FIFO 1 output buffer-A address register
CSI_CO_F2_BUFA_REG	0X0060	CSI Channel_0 FIFO 2 output buffer-A address register
CSI_CO_CAP_STA_REG	0X006C	CSI Channel_0 status register
CSI_CO_INT_EN_REG	0X0070	CSI Channel_0 interrupt enable register
CSI_CO_INT_STA_REG	0X0074	CSI Channel_0 interrupt status register

CSI_CO_HSIZE_REG	0X0080	CSI Channel_0 horizontal size register
CSI_CO_VSIZE_REG	0X0084	CSI Channel_0 vertical size register
CSI_CO_BUF_LEN_REG	0X0088	CSI Channel_0 line buffer length register
CSI_CO_FLIP_SIZE_REG	0X008C	CSI Channel_0 flip size register
CSI_CO_FRM_CLK_CNT_REG	0X0090	CSI Channel_0 frame clock counter register
CSI_CO_ACC_ITNL_CLK_CNT_REG	0X0094	CSI Channel_0 accumulated and internal clock counter register
CSI_C1_CFG_REG	0X0144	CSI Channel_1 configuration register
CSI_C1_SCALE_REG	0X014C	CSI Channel_1 scale register
CSI_C1_F0_BUFA_REG	0X0150	CSI Channel_1 FIFO 0 output buffer-A address register
CSI_C1_F1_BUFA_REG	0X0158	CSI Channel_1 FIFO 1 output buffer-A address register
CSI_C1_F2_BUFA_REG	0X0160	CSI Channel_1 FIFO 2 output buffer-A address register
CSI_C1_CAP_STA_REG	0X016C	CSI Channel_1 status register
CSI_C1_INT_EN_REG	0X0170	CSI Channel_1 interrupt enable register
CSI_C1_INT_STA_REG	0X0174	CSI Channel_1 interrupt status register
CSI_C1_HSIZE_REG	0X0180	CSI Channel_1 horizontal size register
CSI_C1_VSIZE_REG	0X0184	CSI Channel_1 vertical size register
CSI_C1_BUF_LEN_REG	0X0188	CSI Channel_1 line buffer length register
CSI_C1_FLIP_SIZE_REG	0X018C	CSI Channel_1 flip size register
CSI_C1_FRM_CLK_CNT_REG	0X0190	CSI Channel_1 frame clock counter register
CSI_C1_ACC_ITNL_CLK_CNT_REG	0X0194	CSI Channel_1 accumulated and internal clock counter register
CSI_C2_CFG_REG	0X0244	CSI Channel_2 configuration register
CSI_C2_SCALE_REG	0X024C	CSI Channel_2 scale register
CSI_C2_F0_BUFA_REG	0X0250	CSI Channel_2 FIFO 0 output buffer-A address register
CSI_C2_F1_BUFA_REG	0X0258	CSI Channel_2 FIFO 1 output buffer-A address register

CSI_C2_F2_BUFA_REG	0X0260	CSI Channel_2 FIFO 2 output buffer-A address register
CSI_C2_CAP_STA_REG	0X26C	CSI Channel_2 status register
CSI_C2_INT_EN_REG	0X0270	CSI Channel_2 interrupt enable register
CSI_C2_INT_STA_REG	0X0274	CSI Channel_2 interrupt status register
CSI_C2_HSIZE_REG	0X0280	CSI Channel_2 horizontal size register
CSI_C2_VSIZE_REG	0X0284	CSI Channel_2 vertical size register
CSI_C2_BUF_LEN_REG	0X0288	CSI Channel_2 line buffer length register
CSI_C2_FLIP_SIZE_REG	0X028C	CSI Channel_2 flip size register
CSI_C2_FRM_CLK_CNT_REG	0X0290	CSI Channel_2 frame clock counter register
CSI_C2_ACC_ITNL_CLK_CNT_REG	0X0294	CSI Channel_2 accumulated and internal clock counter register
CSI_C3_CFG_REG	0X0344	CSI Channel_3 configuration register
CSI_C3_SCALE_REG	0X034C	CSI Channel_3 scale register
CSI_C3_F0_BUFA_REG	0X0350	CSI Channel_3 FIFO 0 output buffer-A address register
CSI_C3_F1_BUFA_REG	0X0358	CSI Channel_3 FIFO 1 output buffer-A address register
CSI_C3_F2_BUFA_REG	0X0360	CSI Channel_3 FIFO 2 output buffer-A address register
CSI_C3_CAP_STA_REG	0X036C	CSI Channel_3 status register
CSI_C3_INT_EN_REG	0X0370	CSI Channel_3 interrupt enable register
CSI_C3_INT_STA_REG	0X0374	CSI Channel_3 interrupt status register
CSI_C3_HSIZE_REG	0X0380	CSI Channel_3 horizontal size register
CSI_C3_VSIZE_REG	0X0384	CSI Channel_3 vertical size register
CSI_C3_BUF_LEN_REG	0X0388	CSI Channel_3 line buffer length register
CSI_C3_FLIP_SIZE_REG	0X038C	CSI Channel_3 flip size register
CSI_C3_FRM_CLK_CNT_REG	0X0390	CSI Channel_3 frame clock counter register
CSI_C3_ACC_ITNL_CLK_CNT_REG	0X0394	CSI Channel_3 accumulated and internal clock counter register
CCI_CTRL	0x3000	CCI control register

CCI_CFG	0x3004	CCI transmission config register
CCI_FMT	0x3008	CCI packet format register
CCI_BUS_CTRL	0x300C	CCI bus control register
CCI_INT_CTRL	0x3014	CCI interrupt control register
CCI_LC_TRIG	0x3018	CCI line counter trigger register
CCI_FIFO_ACC	0x3100	CCI FIFO access register
CCI_RSV_REG	0x3200	CCI reserved register

6.1.5 CSI Register Description

CSI ENABLE REGISTER

Offset Address: 0x0000			Register Name: CSIO_EN_REG
Bit	Read/ Write	Default/Hex	Description
31	/	/	/
30	R/W	0x0	<p>VER_EN</p> <p>CSI Version Register Read Enable:</p> <p>0: Disable</p> <p>1: Enable</p>
29:24	/	/	/
23:16	R/W	0x00	<p>PTN_CYCLE</p> <p>Pattern generating cycle counter.</p> <p>The pattern in dram will be generated in cycles of PTN_CYCLE+1.</p>
15:5	/	/	/
4	R/W	0x0	<p>PTN_START</p> <p>CSI Pattern Generating Start</p> <p>0: Finish</p> <p>other: Start</p> <p>Software write this bit to "1" to start pattern generating from DRAM. When finished, the hardware will clear this bit to "0" automatically. Generating cycles depends on PTN_CYCLE.</p>
3	R/W	0	<p>CLK_CNT_SPL</p> <p>Sampling time for clk counter per frame</p> <p>0: Sampling clock counter every frame done</p> <p>1: Sampling clock counter every vsync</p>

2	R/W	0	CLK_CNT clk count per frame
1	R/W	0	PTN_GEN_EN Pattern Generation Enable
0	R/W	0	CSI_EN Enable 0: Reset and disable the CSI module 1: Enable the CSI module

CSI INTERFACE CONFIGURATION REGISTER

Offset Address: 0x0004			Register Name: CSIO_IF_CFG_REG
Bit	Read/ Write	Default/H ex	Description
31:2 4	/	/	/
23	R/W	0	CSI_SRC_SWAP 0: normal 1: swap src Normally, Csi0/1 parser the h/v and data to Csi0/1 interface; Enable this bit will swap the signals after Csi1/0 parser to Csi0/1 interface.
22	/	/	/
21	R/W	0	SRC_TYPE Source type 0: Progressed 1: Interlaced
20	R/W	0	FPS_DS Fps down sample 0: no down sample 1: 1/2 fps, only receives the first frame every 2 frames

19	R/W	0	<p>FIELD</p> <p>For YUV HV timing, Field polarity</p> <p>0: negative(field=0 indicate odd, field=1 indicate even)</p> <p>1: positive(field=1 indicate odd, field=0 indicate even)</p> <p>For BT656 timing, Field sequence</p> <p>0: Normal sequence (field 0 first)</p> <p>1: Inverse sequence (field 1 first)</p>
18	R/W	1	<p>VREF_POL</p> <p>Vref polarity</p> <p>0: negative</p> <p>1: positive</p> <p>This register is not apply to CCIR656 interface.</p>
17	R/W	0	<p>HERF_POL</p> <p>Href polarity</p> <p>0: negative</p> <p>1: positive</p> <p>This register is not apply to CCIR656 interface.</p>
16	R/W	1	<p>CLK_POL</p> <p>Data clock type</p> <p>0: active in falling edge</p> <p>1: active in rising edge</p>
15:1 2	/	/	/
11:1 0	R/W	0	<p>SEQ_8PLUS2</p> <p>When select IF_DATA_WIDTH to be 8+2bit, odd/even pixel byte at CSI-D[11:4] will be rearranged to D[11:2]+2'b0 at the actual csi data bus according to these sequences:</p> <p>00: 6'bx+D[9:8], D[7:0]</p> <p>01: D[9:2], 6'bx+D[1:0]</p> <p>10: D[7:0], D[9:8]+6'bx</p>

			11: D[7:0], 6'bx+D[9:8]
9:8	R/W	0	<p>IF_DATA_WIDTH</p> <p>00: 8 bit data bus</p> <p>01: 10 bit data bus</p> <p>10: 12 bit data bus</p> <p>11: 8+2bit data bus</p>
7	R/W	0	<p>MIPI_IF</p> <p>MIPI Interface Enable:</p> <p>0: CSI</p> <p>1: MIPI</p>
6:5	/	/	/
4:0	R/W	0	<p>CSI_IF</p> <p>YUV:</p> <p>00000: YUYV422 Interleaved or RAW (All data in one data bus)</p> <p>00001: YUV422 UV Combined (Y in one data bus and UV in another)</p> <p>00010: YUV444 Planar (Y/U/V in separated data bus)</p> <p>00011: YUV444 Planar to YUV422 UV Combined</p> <p>CCIR656:</p> <p>00100: YUYV422 Interleaved or RAW (All data in one data bus)</p> <p>00101: YUV422 UV Combined (Y in one data bus and UV in another)</p> <p>00110: YUV444 Planar (Y/U/V in separated data bus)</p> <p>00111: YUV444 Planar to YUV422 UV Combined</p> <p>01100: CCIR656 2 channels (All data interleaved in one data bus)</p> <p>01101: CCIR656 4 channels (All data interleaved in one data bus)</p> <p>Others: Reserved</p>

CSI CAPTURE REGISTER

Offset: 0x0008			Register Name: CSIO_CAP_REG
Bit	Read/ Write	Default/Het erogeneous	Description
31:30	/	/	/
29:26	R/W	0x00	CH3_CAP_MASK Vsync number masked before capture.
25	R/W	0	CH3_VCAP_ON Video capture control: Capture the video image data stream on channel 3. 0: Disable video capture If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO. 1: Enable video capture The CSI starts capturing image data at the start of the next frame.
24	R/W	0	CH3_SCAP_ON Still capture control: Capture a single still image frame on channel 3. 0: Disable still capture. 1: Enable still capture The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.
23:22	/	/	/
21:18	R/W	0x00	CH2_CAP_MASK Vsync number masked before capture.
17	R/W	0	CH2_VCAP_ON

			<p>Video capture control: Capture the video image data stream on channel 2.</p> <p>0: Disable video capture</p> <p>If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO.</p> <p>1: Enable video capture</p> <p>The CSI starts capturing image data at the start of the next frame.</p>
16	R/W	0	<p>CH2_SCAP_ON</p> <p>Still capture control: Capture a single still image frame on channel 2.</p> <p>0: Disable still capture.</p> <p>1: Enable still capture</p> <p>The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.</p>
15:1 4	/	/	/
13:1 0	R/W	0x00	<p>CH1_CAP_MASK</p> <p>Vsync number masked before capture.</p>
09	R/W	0	<p>CH1_VCAP_ON</p> <p>Video capture control: Capture the video image data stream on channel 1.</p> <p>0: Disable video capture</p> <p>If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO.</p> <p>1: Enable video capture</p> <p>The CSI starts capturing image data at the start of the next frame.</p>
08	R/W	0	<p>CH1_SCAP_ON</p> <p>Still capture control: Capture a single still image frame on</p>

			<p>channel 1.</p> <p>0: Disable still capture.</p> <p>1: Enable still capture</p> <p>The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.</p>
07:0 6	/	/	/
05:0 2	R/W	0x00	<p>CHO_CAP_MASK</p> <p>Vsync number masked before capture.</p>
01	R/W	0	<p>CHO_VCAP_ON</p> <p>Video capture control: Capture the video image data stream on channel 0.</p> <p>0: Disable video capture</p> <p>If video capture is in progress, the CSI stops capturing image data at the end of the current frame, and all of the current frame data is written to output FIFO.</p> <p>1: Enable video capture</p> <p>The CSI starts capturing image data at the start of the next frame.</p>
00	R/W	0	<p>CHO_SCAP_ON</p> <p>Still capture control: Capture a single still image frame on channel 0.</p> <p>0: Disable still capture.</p> <p>1: Enable still capture</p> <p>The CSI module starts capturing image data at the start of the next frame. The CSI module captures only one frame of image data. This bit is self clearing and always reads as a 0.</p>

CSI SYNCHRONIZATION COUNTER REGISTER

Offset Address: 0x000c			Register Name: CSIO_SYNC_CNT_REG
Bit	Read/Hex	Default/Hex	Description

	Write		
31:24	/	/	/
23:00	R	0	SYNC_CNT The counter value between vsync of Csi0 channel 0 and vsync of Csi1 channel 0 , using 24MHz.

CSI FIFO THRESHOLD REGISTER

Offset Address: 0x0010			Register Name: CSIO_FIFO_THRS_REG
Bit	Read/ Write	Default/H ex	Description
31:24	/	/	/
23:16	R/W	0x0f	PTN_GEN_DLY Clocks delayed before pattern generating start.
15:12	/	/	/
11:00	R/W	0x400	FIFO_THRS When CSIO FIFO occupied memory exceed the threshold, dram frequency can not change.

CSI FIFO STATISTIC REGISTER

Offset Address: 0x0014			Register Name: CSIO_FIFO_STAT_REG
Bit	Read/ Write	Default/H ex	Description
31:12	/	/	/
11:00	R	/	FIFO_FRM_MAX Indicates the maximum depth of FIFO being occupied for whole frame. Update at every vsync or framedone.

CSI PCLK STATISTIC REGISTER

Offset Address: 0x0018			Register Name: CSIO_PCLK_STAT_REG
Bit	Read/	Default/H	Description

	Write	ex	
31	/	/	/
30:16	R	/	PCLK_CNT_LINE_MAX Indicates maximum pixel clock counter value for each line. Update at every vsync or framedone.
15	/	/	/
14:00	R	/	PCLK_CNT_LINE_MIN Indicates minimum pixel clock counter value for each line. Update at every vsync or framedone.

CSI PATTERN GENERATION LENGTH REGISTER

Offset: 0x0030			Register Name: CSIO_PTN_LEN_REG
Bit	Read/ Write	Default/Hex	Description
31:0	R/W	0x0	PTN_LEN The pattern length in byte when generating pattern.

CSI PATTERN GENERATION ADDRESS REGISTER

Offset: 0x0034			Register Name: CSIO_PTN_ADDR_REG
Bit	Read/ Write	Default/He x	Description
31:0	R/W	0x0	PTN_ADDR The pattern DRAM address when generating pattern.

CSI VERSION REGISTER

Offset: 0x003C			Register Name: CSIO_VER_REG
Bit	Read/ Write	Default/He x	Description
31:0	R/W	/	VER

			Version of hardware circuit. Only can be read when version register read enable is on.
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CSI CHANNEL_0 CONFIGURATION REGISTER

Offset Address: 0X0044			Register Name: CSI0_C0_CFG_REG
Bit	Read/W rite	Default /Hex	Description
31:24	R/W	0	<p>PAD_VAL</p> <p>Padding value when OUTPUT_FMT is prgb888</p> <p>0x00~0xff</p>
23:20	R/W	3	<p>INPUT_FMT</p> <p>Input data format</p> <p>0000: RAW stream</p> <p>0001: reserved</p> <p>0010: reserved</p> <p>0011: YUV422</p> <p>0100: YUV420</p> <p>Others: reserved</p>
19:16	R/W	0	<p>OUTPUT_FMT</p> <p>Output data format</p> <p>When the input format is set RAW stream</p> <p>0000: field-raw-8</p> <p>0001: field-raw-10</p> <p>0010: field-raw-12</p> <p>0011: reserved</p> <p>0100: field-rgb565</p> <p>0101: field-rgb888</p> <p>0110: field-prgb888</p> <p>0111: field-uv-combined</p>

		1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: frame-uv-combined When the input format is set Bayer RGB242 0000: planar RGB242 When the input format is set YUV422 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved
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			<p>When the input format is set YUV420</p> <p>0000: Reserved</p> <p>0001: field planar YCbCr 420</p> <p>0010: frame planar YCbCr 420</p> <p>0011: Reserved</p> <p>0100: Reserved</p> <p>0101: field planar YCbCr 420 UV combined</p> <p>0110: frame planar YCbCr 420 UV combined</p> <p>0111: Reserved</p> <p>1000: Reserved</p> <p>1001: field MB YCbCr 420</p> <p>1010: frame MB YCbCr 420</p> <p>1011: Reserved</p> <p>1100: Reserved</p> <p>1101: field planar YCbCr 420 10bit UV combined</p> <p>1110: Reserved</p> <p>1111: Reserved</p> <p>Others: reserved</p>
15:14	/	/	/
13	R/W	0	<p>VFLIP_EN</p> <p>Vertical flip enable</p> <p>When enabled, the received data will be arranged in vertical flip.</p> <p>0:Disable</p> <p>1:Enable</p>
12	R/W	0	<p>HFLIP_EN</p> <p>Horizontal flip enable</p> <p>When enabled, the received data will be arranged in horizontal</p>

			flip. 0:Disable 1:Enable
11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU 10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU
07:00	/	/	/

CSI CHANNEL_0 SCALE REGISTER

Offset Address: 0X004C			Register Name: CSIO_C0_SCALE_REG
Bit	Read/W rite	Default /Hex	Description
31:01	/	/	/

00	R/W	0	QUART_EN
When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.			

CSI CHANNEL_0 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0050			Register Name: CSIO_CO_F0_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	COFO_BUFA FIFO 0 output buffer-A address

CSI CHANNEL_0 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0058			Register Name: CSIO_CO_F1_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C0F1_BUFA FIFO 1 output buffer-A address

CSI CHANNEL_0 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0060			Register Name: CSIO_CO_F2_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C0F2_BUFA FIFO 2 output buffer-A address

CSI CHANNEL_0 STATUS REGISTER

Offset Address: 0X006C	Register Name: CSIO_CO_CAP_STA_REG
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Bit	Read/W rite	Default /Hex	Description
31:03	/	/	/
02	R	0	<p>FIELD_STA</p> <p>The status of the received field</p> <p>0: Field 0</p> <p>1: Field 1</p>
01	R	0	<p>VCAP_STA</p> <p>Video capture in progress</p> <p>Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.</p>
00	R	0	<p>SCAP_STA</p> <p>Still capture in progress</p> <p>Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.</p>

CSI CHANNEL_0 INTERRUPT ENABLE REGISTER

Offset Address: 0X0070			Register Name: CSI0_C0_INT_EN_REG
Bit	Read/W rite	Default /Hex	Description
31:08	/	/	/
07	R/W	0	<p>VS_INT_EN</p> <p>vsync flag</p> <p>The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame</p>

06	R/W	0	<p>HB_OF_INT_EN</p> <p>Hblank FIFO overflow</p> <p>The bit is set when 3 FIFOs still overflow after the hblank.</p>
05	R/W	0	<p>MUL_ERR_INT_EN</p> <p>Multi-channel writing error</p> <p>Indicates error has been detected for writing data to a wrong channel.</p>
04	R/W	0	<p>FIFO2_OF_INT_EN</p> <p>FIFO 2 overflow</p> <p>The bit is set when the FIFO 2 become overflow.</p>
03	R/W	0	<p>FIFO1_OF_INT_EN</p> <p>FIFO 1 overflow</p> <p>The bit is set when the FIFO 1 become overflow.</p>
02	R/W	0	<p>FIFO0_OF_INT_EN</p> <p>FIFO 0 overflow</p> <p>The bit is set when the FIFO 0 become overflow.</p>
01	R/W	0	<p>FD_INT_EN</p> <p>Frame done</p> <p>Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.</p>
00	R/W	0	<p>CD_INT_EN</p> <p>Capture done</p> <p>Indicates the CSI has completed capturing the image data.</p> <p>For still capture, the bit is set when one frame data has been written to buffer.</p> <p>For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame</p>

			end means field end.
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CSI CHANNEL_0 INTERRUPT STATUS REGISTER

Offset Address: 0X0074			Register Name: CSIO_CO_INT_STA_REG
Bit	Read/W rite	Default /Hex	Description
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

CSI CHANNEL_0 HORIZONTAL SIZE REGISTER

Offset Address: 0X0080			Register Name: CSIO_C0_HSIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel unit start. Pixel is valid from this unit.

CSI CHANNEL_0 VERTICAL SIZE REGISTER

Offset Address: 0X0084			Register Name: CSIO_C0_VSIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

CSI CHANNEL_0 BUFFER LENGTH REGISTER

Offset Address: 0X0088			Register Name: CSIO_C0_BUF_LEN_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.

15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

CSI CHANNEL_0 FLIP SIZE REGISTER

Offset Address: 0X008C			Register Name: CSIO_CO_FLIP_SIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

CSI CHANNEL_0 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0090			Register Name: CSIO_CO_FRM_CLK_CNT_REG
Bit	Read/ Write	Default/H ex	Description
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0.

CSI CHANNEL_0 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0094	Register Name: CSIO_CO_ACC_ITNL_CLK_CNT_REG
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Bit	Read/ Write	Default/H ex	Description
31:24	R/W	0	<p>ACC_CLK_CNT</p> <p>The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame.</p> <p>When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.</p>
23:00	R	0	<p>ITNL_CLK_CNT</p> <p>The instant value of internal frame clock counter.</p> <p>When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.</p>

CSI CHANNEL_1 CONFIGURATION REGISTER

Offset Address: 0X0144			Register Name: CSI0_C1_CFG_REG
Bit	Read/Writ e	Default/He x	Description
31:2 4	R/W	0	<p>PAD_VAL</p> <p>Padding value when OUTPUT_FMT is prgb888</p> <p>0x00~0xff</p>
23:2 0	R/W	3	<p>INPUT_FMT</p> <p>Input data format</p> <p>0000: RAW stream</p> <p>0001: reserved</p> <p>0010: reserved</p> <p>0011: YUV422</p> <p>0100: YUV420</p>

			Others: reserved
19:1 6	R/W	0	<p>OUTPUT_FMT</p> <p>Output data format</p> <p>When the input format is set RAW stream</p> <ul style="list-style-type: none"> 0000: field-raw-8 0001: field-raw-10 0010: field-raw-12 0011: reserved 0100: field-rgb565 0101: field-rgb888 0110: field-prgb888 0111: field-uv-combined 1000: frame-raw-8 1001: frame-raw-10 1010: frame-raw-12 1011: reserved 1100: frame-rgb565 1101: frame-rgb888 1110: frame-prgb888 1111: frame-uv-combined <p>When the input format is set Bayer RGB242</p> <ul style="list-style-type: none"> 0000: planar RGB242 <p>When the input format is set YUV422</p> <ul style="list-style-type: none"> 0000: field planar YCbCr 422 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: frame planar YCbCr 422

	<p>0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved</p> <p>When the input format is set YUV420</p> <p>0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved</p>
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			1111: Reserved Others: reserved
15:1 4	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:1 0	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
09:0 8	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU

07:0 0	/	/	10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU /
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CSI CHANNEL_1 SCALE REGISTER

Offset Address: 0X014C			Register Name: CSI0_C1_SCALE_REG
Bit	Read/W rite	Default /Hex	Description
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

CSI CHANNEL_1 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0150			Register Name: CSI0_C1_F0_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C1F0_BUFA FIFO 0 output buffer-A address

CSI CHANNEL_1 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0158			Register Name: CSI0_C1_F1_BUFA_REG
Bit	Read/W rite	Default /Hex	Description

31:00	R/W	0	C1F1_BUFA FIFO 1 output buffer-A address
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CSI CHANNEL_1 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0160			Register Name: CSI0_C1_F2_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C1F2_BUFA FIFO 2 output buffer-A address

CSI CHANNEL_1 STATUS REGISTER

Offset Address: 0X016C			Register Name: CSI0_C1_CAP_STA_REG
Bit	Read/W rite	Default /Hex	Description
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame

			<p>capture. It clears itself after the last pixel of the first frame is captured.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.</p>
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CSI CHANNEL_1 INTERRUPT ENABLE REGISTER

Offset Address: 0X0170			Register Name: CSI0_C1_INT_EN_REG
Bit	Read/W rite	Default /Hex	Description
31:08	/	/	/
07	R/W	0	<p>VS_INT_EN</p> <p>vsync flag</p> <p>The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame</p>
06	R/W	0	<p>HB_OF_INT_EN</p> <p>Hblank FIFO overflow</p> <p>The bit is set when 3 FIFOs still overflow after the hblank.</p>
05	R/W	0	<p>MUL_ERR_INT_EN</p> <p>Multi-channel writing error</p> <p>Indicates error has been detected for writing data to a wrong channel.</p>
04	R/W	0	<p>FIFO2_OF_INT_EN</p> <p>FIFO 2 overflow</p> <p>The bit is set when the FIFO 2 become overflow.</p>
03	R/W	0	<p>FIFO1_OF_INT_EN</p> <p>FIFO 1 overflow</p> <p>The bit is set when the FIFO 1 become overflow.</p>
02	R/W	0	<p>FIFO0_OF_INT_EN</p> <p>FIFO 0 overflow</p>

			The bit is set when the FIFO 0 become overflow.
01	R/W	0	<p>FD_INT_EN</p> <p>Frame done</p> <p>Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.</p>
00	R/W	0	<p>CD_INT_EN</p> <p>Capture done</p> <p>Indicates the CSI has completed capturing the image data.</p> <p>For still capture, the bit is set when one frame data has been written to buffer.</p> <p>For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.</p>

CSI CHANNEL_1 INTERRUPT STATUS REGISTER

Offset Address: 0X0174			Register Name: CSIO_C1_INT_STA_REG
Bit	Read/W rite	Default /Hex	Description
31:08	/	/	/
07	R/W	0	<p>VS_PD</p> <p>vsync flag</p>
06	R/W	0	<p>HB_OF_PD</p> <p>Hblank FIFO overflow</p>
05	R/W	0	<p>MUL_ERR_PD</p> <p>Multi-channel writing error</p>
04	R/W	0	<p>FIFO2_OF_PD</p> <p>FIFO 2 overflow</p>

03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

CSI CHANNEL_1 HORIZONTAL SIZE REGISTER

Offset Address: 0X0180			Register Name: CSI0_C1_HSIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start. Pixel data is valid from this clock.

CSI CHANNEL_1 VERTICAL SIZE REGISTER

Offset Address: 0X0184			Register Name: CSI0_C1_VSIZE_REG
Bit	Read/W rite	Default /Hex	Description

31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

CSI CHANNEL_1 BUFFER LENGTH REGISTER

Offset Address: 0X0188			Register Name: CSI0_C1_BUF_LEN_REG
Bit	Read/W/ rite	Default/ Hex	Description
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

CSI CHANNEL_1 FLIP SIZE REGISTER

Offset Address: 0X018C			Register Name: CSI0_C1_FLIP_SIZE_REG
Bit	Read/Writ e	Default/H ex	Description
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

CSI CHANNEL_1 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0190			Register Name: CSI0_C1_FRM_CLK_CNT_REG
Bit	Read/ Write	Default/H ex	Description
31:24	/	/	/
23:00	R	0	<p>FRM_CLK_CNT</p> <p>Counter value between every frame. For instant hardware frame rate statics.</p> <p>The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. Then the FRM_CLK_CNT is added to ACC_CLK_CNT.</p>

CSI CHANNEL_1 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0194			Register Name: CSI0_C1_ACC_ITNL_CLK_CNT_REG
Bit	Read/ Write	Default/H ex	Description
31:24	R/W	0	<p>ACC_CLK_CNT</p> <p>The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame.</p> <p>When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.</p>
23:00	R	0	<p>ITNL_CLK_CNT</p> <p>The instant value of internal frame clock counter.</p> <p>When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.</p>

CSI CHANNEL_2 CONFIGURATION REGISTER

Offset Address: 0X0244			Register Name: CSI0_C2_CFG_REG
Bit	Read/Writ e	Default/H ex	Description
31:2 4	R/W	0	<p>PAD_VAL</p> <p>Padding value when OUTPUT_FMT is prgb888</p> <p>0x00~0xff</p>
23:2 0	R/W	3	<p>INPUT_FMT</p> <p>Input data format</p> <p>0000: RAW stream</p> <p>0001: reserved</p> <p>0010: reserved</p> <p>0011: YUV422</p> <p>0100: YUV420</p> <p>Others: reserved</p>
19:1 6	R/W	0	<p>OUTPUT_FMT</p> <p>Output data format</p> <p>When the input format is set RAW stream</p> <p>0000: field-raw-8</p> <p>0001: field-raw-10</p> <p>0010: field-raw-12</p> <p>0011: reserved</p> <p>0100: field-rgb565</p> <p>0101: field-rgb888</p> <p>0110: field-prgb888</p> <p>0111: field-uv-combined</p> <p>1000: frame-raw-8</p> <p>1001: frame-raw-10</p>

	<p>1010: frame-raw-12</p> <p>1011: reserved</p> <p>1100: frame-rgb565</p> <p>1101: frame-rgb888</p> <p>1110: frame-prgb888</p> <p>1111: frame-uv-combined</p> <p>When the input format is set Bayer RGB242</p> <p>0000: planar RGB242</p> <p>When the input format is set YUV422</p> <p>0000: field planar YCbCr 422</p> <p>0001: field planar YCbCr 420</p> <p>0010: frame planar YCbCr 420</p> <p>0011: frame planar YCbCr 422</p> <p>0100: field planar YCbCr 422 UV combined</p> <p>0101: field planar YCbCr 420 UV combined</p> <p>0110: frame planar YCbCr 420 UV combined</p> <p>0111: frame planar YCbCr 422 UV combined</p> <p>1000: field MB YCbCr 422</p> <p>1001: field MB YCbCr 420</p> <p>1010: frame MB YCbCr 420</p> <p>1011: frame MB YCbCr 422</p> <p>1100: field planar YCbCr 422 10bit UV combined</p> <p>1101: field planar YCbCr 420 10bit UV combined</p> <p>1110: Reserved</p> <p>1111: Reserved</p> <p>When the input format is set YUV420</p>
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			0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved
15:1 4	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip.

			0:Disable 1:Enable
11:1 0	R/W	0	<p>FIELD_SEL Field selection.</p> <p>00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved</p>
09:0 8	R/W	2	<p>INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format.</p> <p>All data interleaved in one channel:</p> <p>00: YUYV 01: YVYU 10: UYVY 11: VYUY</p> <p>Y and UV in separated channel:</p> <p>x0: UV x1: VU</p>
07:0 0	/	/	/

CSI CHANNEL_2 SCALE REGISTER

Offset Address: 0X024C			Register Name: CSI0_C2_SCALE_REG
Bit	Read/W rite	Default /Hex	Description
31:01	/	/	/
00	R/W	0	QUART_EN

			When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.
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CSI CHANNEL_2 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0250			Register Name: CSI0_C2_F0_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C2F0_BUFA FIFO 0 output buffer-A address

CSI CHANNEL_2 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0258			Register Name: CSI0_C2_F1_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C2F1_BUFA FIFO 1 output buffer-A address

CSI CHANNEL_2 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0260			Register Name: CSI0_C2_F2_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C2F2_BUFA FIFO 2 output buffer-A address

CSI CHANNEL_2 STATUS REGISTER

Offset Address: 0X026C			Register Name: CSI0_C2_CAP_STA_REG
Bit	Read/W	Default	Description

	rite	/Hex	
31:03	/	/	/
02	R	0	<p>FIELD_STA</p> <p>The status of the received field</p> <p>0: Field 0</p> <p>1: Field 1</p>
01	R	0	<p>VCAP_STA</p> <p>Video capture in progress</p> <p>Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.</p>
00	R	0	<p>SCAP_STA</p> <p>Still capture in progress</p> <p>Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is captured.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.</p>

CSI CHANNEL_2 INTERRUPT ENABLE REGISTER

Offset Address: 0X0270			Register Name: CSI0_C2_INT_EN_REG
Bit	Read/W rite	Default /Hex	Description
31:08	/	/	/
07	R/W	0	<p>VS_INT_EN</p> <p>vsync flag</p> <p>The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame</p>

06	R/W	0	<p>HB_OF_INT_EN</p> <p>Hblank FIFO overflow</p> <p>The bit is set when 3 FIFOs still overflow after the hblank.</p>
05	R/W	0	<p>MUL_ERR_INT_EN</p> <p>Multi-channel writing error</p> <p>Indicates error has been detected for writing data to a wrong channel.</p>
04	R/W	0	<p>FIFO2_OF_INT_EN</p> <p>FIFO 2 overflow</p> <p>The bit is set when the FIFO 2 become overflow.</p>
03	R/W	0	<p>FIFO1_OF_INT_EN</p> <p>FIFO 1 overflow</p> <p>The bit is set when the FIFO 1 become overflow.</p>
02	R/W	0	<p>FIFO0_OF_INT_EN</p> <p>FIFO 0 overflow</p> <p>The bit is set when the FIFO 0 become overflow.</p>
01	R/W	0	<p>FD_INT_EN</p> <p>Frame done</p> <p>Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.</p>
00	R/W	0	<p>CD_INT_EN</p> <p>Capture done</p> <p>Indicates the CSI has completed capturing the image data.</p> <p>For still capture, the bit is set when one frame data has been written to buffer.</p> <p>For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame</p>

			end means field end.
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CSI CHANNEL_2 INTERRUPT STATUS REGISTER

Offset Address: 0X0274			Register Name: CSIO_C2_INT_STA_REG
Bit	Read/W rite	Default /Hex	Description
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow
03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

CSI CHANNEL_2 HORIZONTAL SIZE REGISTER

Offset Address: 0X0280			Register Name: CSI0_C2_HSIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start. Pixel data is valid from this clock.

CSI CHANNEL_2 VERTICAL SIZE REGISTER

Offset Address: 0X0284			Register Name: CSI0_C2_VSIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

CSI CHANNEL_2 BUFFER LENGTH REGISTER

Offset Address: 0X0288			Register Name: CSI0_C2_BUF_LEN_REG
Bit	Read/Writ e	Default/H ex	Description
31:29	/	/	/
28:1	R/W	140	BUF_LEN_C

6			Buffer length of chroma C in a line. Unit is byte.
15:1 3	/	/	/
12:0 0	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

CSI CHANNEL_2 FLIP SIZE REGISTER

Offset Address: 0X028C			Register Name: CSI0_C2_FLIP_SIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

CSI CHANNEL_2 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0290			Register Name: CSI0_C2_FRM_CLK_CNT_REG
Bit	Read/ Write	Default/H ex	Description
31:24	/	/	/
23:00	R	0	FRM_CLK_CNT Counter value between every frame. For instant hardware frame rate statics. The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. Then the FRM_CLK_CNT is added to ACC_CLK_CNT.

CSI CHANNEL_2 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0294			Register Name: CSI0_C2_ACC_ITNL_CLK_CNT_REG
Bit	Read/ Write	Default/H ex	Description
31:24	R/W	0	<p>ACC_CLK_CNT</p> <p>The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame.</p> <p>When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.</p>
23:00	R	0	<p>ITNL_CLK_CNT</p> <p>The instant value of internal frame clock counter.</p> <p>When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.</p>

CSI CHANNEL_3 CONFIGURATION REGISTER

Offset Address: 0X0344			Register Name: CSI0_C3_CFG_REG
Bit	Read/W rite	Default /Hex	Description
31:24	R/W	0	<p>PAD_VAL</p> <p>Padding value when OUTPUT_FMT is prgb888</p> <p>0x00~0xff</p>
23:20	R/W	3	<p>INPUT_FMT</p> <p>Input data format</p> <p>0000: RAW stream</p> <p>0001: reserved</p> <p>0010: reserved</p>

			0011: YUV422 0100: YUV420 Others: reserved
19:16	R/W	0	<p>OUTPUT_FMT</p> <p>Output data format</p> <p>When the input format is set RAW stream</p> <p>0000: field-raw-8</p> <p>0001: field-raw-10</p> <p>0010: field-raw-12</p> <p>0011: reserved</p> <p>0100: field-rgb565</p> <p>0101: field-rgb888</p> <p>0110: field-prgb888</p> <p>0111: field-uv-combined</p> <p>1000: frame-raw-8</p> <p>1001: frame-raw-10</p> <p>1010: frame-raw-12</p> <p>1011: reserved</p> <p>1100: frame-rgb565</p> <p>1101: frame-rgb888</p> <p>1110: frame-prgb888</p> <p>1111: frame-uv-combined</p> <p>When the input format is set Bayer RGB242</p> <p>0000: planar RGB242</p> <p>When the input format is set YUV422</p> <p>0000: field planar YCbCr 422</p> <p>0001: field planar YCbCr 420</p>

		0010: frame planar YCbCr 420 0011: frame planar YCbCr 422 0100: field planar YCbCr 422 UV combined 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: frame planar YCbCr 422 UV combined 1000: field MB YCbCr 422 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: frame MB YCbCr 422 1100: field planar YCbCr 422 10bit UV combined 1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved
		When the input format is set YUV420 0000: Reserved 0001: field planar YCbCr 420 0010: frame planar YCbCr 420 0011: Reserved 0100: Reserved 0101: field planar YCbCr 420 UV combined 0110: frame planar YCbCr 420 UV combined 0111: Reserved 1000: Reserved 1001: field MB YCbCr 420 1010: frame MB YCbCr 420 1011: Reserved 1100: Reserved

			1101: field planar YCbCr 420 10bit UV combined 1110: Reserved 1111: Reserved Others: reserved
15:14	/	/	/
13	R/W	0	VFLIP_EN Vertical flip enable When enabled, the received data will be arranged in vertical flip. 0:Disable 1:Enable
12	R/W	0	HFLIP_EN Horizontal flip enable When enabled, the received data will be arranged in horizontal flip. 0:Disable 1:Enable
11:10	R/W	0	FIELD_SEL Field selection. 00: capturing with field 1. 01: capturing with field 2. 10: capturing with either field. 11: reserved
09:08	R/W	2	INPUT_SEQ Input data sequence, only valid for YUV422 and YUV420 input format. All data interleaved in one channel: 00: YUYV 01: YVYU

07:00	/	/	10: UYVY 11: VYUY Y and UV in separated channel: x0: UV x1: VU /
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CSI CHANNEL_3 SCALE REGISTER

Offset Address: 0X034C			Register Name: CSI0_C3_SCALE_REG
Bit	Read/W rite	Default /Hex	Description
31:01	/	/	/
00	R/W	0	QUART_EN When this bit is set to 1, input image will be decimated to quarter size. All input format are supported.

CSI CHANNEL_3 FIFO 0 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0350			Register Name: CSI0_C3_F0_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C3F0_BUFA FIFO 0 output buffer-A address

CSI CHANNEL_3 FIFO 1 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0358			Register Name: CSI0_C3_F1_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C3F1_BUFA

			FIFO 1 output buffer-A address
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CSI CHANNEL_3 FIFO 2 OUTPUT BUFFER-A ADDRESS REGISTER

Offset Address: 0X0360			Register Name: CSI0_C3_F2_BUFA_REG
Bit	Read/W rite	Default /Hex	Description
31:00	R/W	0	C3F2_BUFA FIFO 2 output buffer-A address

CSI CHANNEL_3 STATUS REGISTER

Offset Address: 0X036C			Register Name: CSI0_C3_CAP_STA_REG
Bit	Read/W rite	Default /Hex	Description
31:03	/	/	/
02	R	0	FIELD_STA The status of the received field 0: Field 0 1: Field 1
01	R	0	VCAP_STA Video capture in progress Indicates the CSI is capturing video image data (multiple frames). The bit is set at the start of the first frame after enabling video capture. When software disables video capture, it clears itself after the last pixel of the current frame is captured.
00	R	0	SCAP_STA Still capture in progress Indicates the CSI is capturing still image data (single frame). The bit is set at the start of the first frame after enabling still frame capture. It clears itself after the last pixel of the first frame is

			<p>captured.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means filed end.</p>
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CSI CHANNEL_3 INTERRUPT ENABLE REGISTER

Offset Address: 0X0370			Register Name: CSI0_C3_INT_EN_REG
Bit	Read/W rite	Default /Hex	Description
31:08	/	/	/
07	R/W	0	<p>VS_INT_EN</p> <p>vsync flag</p> <p>The bit is set when vsync come. And at this time load the buffer address for the coming frame. So after this irq come, change the buffer address could only effect next frame</p>
06	R/W	0	<p>HB_OF_INT_EN</p> <p>Hblank FIFO overflow</p> <p>The bit is set when 3 FIFOs still overflow after the hblank.</p>
05	R/W	0	<p>MUL_ERR_INT_EN</p> <p>Multi-channel writing error</p> <p>Indicates error has been detected for writing data to a wrong channel.</p>
04	R/W	0	<p>FIFO2_OF_INT_EN</p> <p>FIFO 2 overflow</p> <p>The bit is set when the FIFO 2 become overflow.</p>
03	R/W	0	<p>FIFO1_OF_INT_EN</p> <p>FIFO 1 overflow</p> <p>The bit is set when the FIFO 1 become overflow.</p>
02	R/W	0	<p>FIFO0_OF_INT_EN</p> <p>FIFO 0 overflow</p> <p>The bit is set when the FIFO 0 become overflow.</p>

01	R/W	0	<p>FD_INT_EN</p> <p>Frame done</p> <p>Indicates the CSI has finished capturing an image frame. Applies to video capture mode. The bit is set after each completed frame capturing data is written to buffer as long as video capture remains enabled.</p>
00	R/W	0	<p>CD_INT_EN</p> <p>Capture done</p> <p>Indicates the CSI has completed capturing the image data.</p> <p>For still capture, the bit is set when one frame data has been written to buffer.</p> <p>For video capture, the bit is set when the last frame has been written to buffer after video capture has been disabled.</p> <p>For CCIR656 interface, if the output format is frame planar YCbCr 420 mode, the frame end means the field2 end, the other frame end means field end.</p>

CSI CHANNEL_3 INTERRUPT STATUS REGISTER

Offset Address: 0X0374			Register Name: CSI0_C3_INT_STA_REG
Bit	Read/W rite	Default /Hex	Description
31:08	/	/	/
07	R/W	0	VS_PD vsync flag
06	R/W	0	HB_OF_PD Hblank FIFO overflow
05	R/W	0	MUL_ERR_PD Multi-channel writing error
04	R/W	0	FIFO2_OF_PD FIFO 2 overflow

03	R/W	0	FIFO1_OF_PD FIFO 1 overflow
02	R/W	0	FIFO0_OF_PD FIFO 0 overflow
01	R/W	0	FD_PD Frame done
00	R/W	0	CD_PD Capture done

CSI CHANNEL_3 HORIZONTAL SIZE REGISTER

Offset Address: 0X0380			Register Name: CSI0_C3_HSIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	500	HOR_LEN Horizontal pixel clock length. Valid pixel clocks of a line.
15:13	/	/	/
12:00	R/W	0	HOR_START Horizontal pixel clock start. Pixel data is valid from this clock.

CSI CHANNEL_3 VERTICAL SIZE REGISTER

Offset Address: 0X0384			Register Name: CSI0_C3_VSIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/

28:16	R/W	1E0	VER_LEN Vertical line length. Valid line number of a frame.
15:13	/	/	/
12:00	R/W	0	VER_START Vertical line start. data is valid from this line.

CSI CHANNEL_3 BUFFER LENGTH REGISTER

Offset Address: 0X0388			Register Name: CSIO_C3_BUF_LEN_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	140	BUF_LEN_C Buffer length of chroma C in a line. Unit is byte.
15:13	/	/	/
12:00	R/W	280	BUF_LEN Buffer length of luminance Y in a line. Unit is byte.

CSI CHANNEL_3 FLIP SIZE REGISTER

Offset Address: 0X038C			Register Name: CSIO_C3_FLIP_SIZE_REG
Bit	Read/W rite	Default /Hex	Description
31:29	/	/	/
28:16	R/W	1E0	VER_LEN Vertical line number when in vflip mode.
15:13	/	/	/
12:00	R/W	280	VALID_LEN Valid components of a line when in flip mode.

CSI CHANNEL_3 FRAME CLOCK COUNTER REGISTER

Offset Address: 0x0390			Register Name: CSIO_C3_FRM_CLK_CNT_REG
Bit	Read/ Write	Default/H ex	Description
31:24	/	/	/
23:00	R	0	<p>FRM_CLK_CNT</p> <p>Counter value between every frame. For instant hardware frame rate statics.</p> <p>The internal counter is added by one every 24MHz clock cycle. When frame done or vsync comes, the internal counter value is sampled to FRM_CLK_CNT, and cleared to 0. Then the FRM_CLK_CNT is added to ACC_CLK_CNT.</p>

CSI CHANNEL_3 ACCUMULATED AND INTERNAL CLOCK COUNTER REGISTER

Offset Address: 0x0394			Register Name: CSIO_C3_ACC_ITNL_CLK_CNT_REG
Bit	Read/ Write	Default/H ex	Description
31:24	R/W	0	<p>ACC_CLK_CNT</p> <p>The accumulated value of FRM_CLK_CNT for software frame rate statics. Every interrupt of frame done, the software check this accumulated value and clear it to 0. If the ACC_CLK_CNT is larger than 1, the software has lost frame.</p> <p>When frame done or vsync comes, ACC_CLK_CNT = ACC_CLK_CNT + 1, and cleared to 0 when writing 0 to this register.</p>
23:00	R	0	<p>ITNL_CLK_CNT</p> <p>The instant value of internal frame clock counter.</p> <p>When frame done interrupt comes, the software can query this counter for judging whether it is the time for updating the double buffer address registers.</p>

CCI CONTROL REGISTER

Offset Address: 0x000			Register Name: CCI_CTRL
Bit	Read/ Write	Default/Hex	Description
31	R/W	0	<p>SINGLE_TRAN</p> <p>0: Transmission idle</p> <p>1: Start single transmission</p> <p>Automatically cleared to '0' when finished. Abort current transmission immediately if changing from '1' to '0'. If slave not respond for the expected status over the time defined by TIMEOUT, current transmission will stop. PACKET_CNT will return the sequence number when transmission fail. All format setting and data will be loaded from registers and FIFO when transmission start.</p>
30	R/W	0	<p>REPEAT_TRAN</p> <p>0: transmission idle</p> <p>1: repeated transmission</p> <p>When this bit is set to 1, transmission repeats when trigger signal (such as VSYNC/ VCAP done) repeats.</p> <p>If changing this bit from '1' to '0' during transmission, the current transmission will be guaranteed then stop.</p>
29	R/W	0	<p>RESTART_MODE</p> <p>0: RESTART</p> <p>1: STOP+START</p> <p>Define the CCI action after sending register address.</p>
28	R/W	0	<p>READ_TRAN_MODE</p> <p>0: send slave_id+W</p> <p>1: do not send slave_id+W</p> <p>Setting this bit to 1 if reading from a slave which register width is equal to 0.</p>
27:4	R	0	TRAN_RESULT 000: OK

			001: FAIL Other: Reserved
23:1 6	R	/	CCI_STA 0x00: bus error 0x08: START condition transmitted 0x10: Repeated START condition transmitted 0x18: Address + Write bit transmitted, ACK received 0x20: Address + Write bit transmitted, ACK not received 0x28: Data byte transmitted in master mode, ACK received 0x30: Data byte transmitted in master mode, ACK not received 0x38: Arbitration lost in address or data byte 0x40: Address + Read bit transmitted, ACK received 0x48: Address + Read bit transmitted, ACK not received 0x50: Data byte received in master mode, ACK received 0x58: Data byte received in master mode, ACK not received 0x01: Timeout when sending 9 th SCL clk Other: Reserved
15:2	/	/	/
1	R/W	0	SOFT_RESET 0: normal 1: reset
0	R/W	0	CCI_EN 0: Module disable 1: Module enable

CCI TRANSMISSION CONFIGURATION REGISTER

Offset Address: 0x004		Register Name: CCI_CFG	
Bit	Read/ Write	Default/Het x	Description

31:2 4	R/W	0x10	TIMEOUT_N When sending the 9 th clock, assert fail signal when slave device did not response after $N \cdot F_{SCL}$ cycles. And software must do a reset to CCI module and send a stop condition to slave.
23:1 6	R/W	0x00	INTERVAL Define the interval between each packet in $40 \cdot F_{SCL}$ cycles, 0~255
15	R/W	0	PACKET_MODE Select where to load slave id / data width 0: Compact mode 1: Complete mode In compact mode, slave id/register width / data width will be loaded from CCI_FMT register, only address and data read from memory. In complete mode, they will be loaded from packet memory.
14:8	/	/	/
7	R/W	0	SRC_SEL 0: From register CCI_FIFO_ACC 1: From dram address define by CCI_PARA_BASE Read packet data source select.
6:4	R/W	0	TRIG_MODE Transmit mode: 000: Immediately, no trigger 001: Reserved 010: CSI0 int trigger 011: CSI1 int trigger
3:0	R/W	0	CSI_TRIG CSI Int trig signal select: 0000: First HREF start 0001: Last HREF done 0010: Line counter trigger

			other: Reserved
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CCI PACKET FORMAT REGISTER

Offset Address: 0x008			Register Name: CCI_FMT
Bit	Read/ Write	Default/H ex	Description
31:2 5	R/W	0	SLV_ID 7bit address
24	R/W	0	CMD 0: write 1: read
23:2 0	R/W	1	ADDR_BYTEx How many bytes be sent as address 0~15
19:1 6	R/W	1	DATA_BYTEx How many bytes be sent/received as data 1~15 Normally use ADDR_DATA with 0_2, 1_1, 1_2, 2_1, 2_2 access mode. If DATA bytes is 0, transmission will not start. In complete mode, the ADDR_BYTEx and DATA_BYTEx is defined in a byte's high/low 4bit.
15:0	R/W	1	PACKET_CNT FIFO data be transmitted as PACKET_CNT packets in current format. Total bytes not exceed 32bytes.

CCI BUS CONTROL REGISTER

Offset Address: 0x00C			Register Name: CCI_BUS_CTRL
Bit	Read/ Write	Default/H ex	Description

31:1 6	R/W	0	DLY_CYC 0~65535 F_{SCL} cycles between each transmission
15	R/W	0	DLY_TRIG 0: disable 1: execute transmission after internal counter delay when triggered
14:1 2	R/W	0x2	CLK_N CCI bus sampling clock $F_0=24MHz/2^{\text{CLK_N}}$
11:8	R/W	0x5	CLK_M CCI output SCL frequency is $F_{SCL}=F_1/10=(F_0/(CLK_M+1))/10$
7	R	/	SCL_STA SCL current status
6	R	/	SDA_STA SDA current status
5	R/W	0	SCL_PEN SCL PAD enable
4	R/W	0	SDA_PEN SDA PAD enable
3	R/W	0	SCL_MOV SCL manual output value
2	R/W	0	SDA_MOV SDA manual output value
1	R/W	0	SCL_MOE SCL manual output en
0	R/W	0	SDA_MOE SDA manual output en

CCI DRAM INPUT BASE REGISTER

Offset Address: 0x010	Register Name: CCI_PARA_BASE
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Bit	Read/ Write	Default/H ex	Description
31:0	R/W	0	DRAM_BASE Dram address for CCI data, used in dram input mode. CCI transmission read/write data from/to dram in byte.

CCI INTERRUPT CONTROL REGISTER

Offset Address: 0x014			Register Name: CCI_INT_CTRL
Bit	Read/ Write	Default/H ex	Description
31:18	/	/	/
17	R/W	0	S_TRAN_ERR_INT_EN
16	R/W	0	S_TRAN_COM_INT_EN
15:2	/	/	/
1	R/W	0	S_TRAN_ERR_PD
0	R/W	0	S_TRAN_COM_PD

CCI LINE COUNTER TRIGGER CONTROL REGISTER

Offset Address: 0x018			Register Name: CCI_LC_TRIG
Bit	Read/ Write	Default/H ex	Description
31:13	/	/	/
12:0	R/W	0	LN_CNT 0~8191: line counter send trigger when 1 st ~8192 th line is received.

CCI FIFO ACCESS REGISTER

Offset Address: 0x100~0x13f			Register Name: CCI_FIFO_ACC
Bit	Read/ Write	Default/H	Description

	Write	ex	
31:0	R/W	0	DATA_FIFO From 0x100 to 0x13f, CCI data FIFO is 64bytes, used in FIFO input mode. CCI transmission read/write data from/to FIFO in byte.

CCI RESERVED REGISTER

Offset Address: 0x200~0x220			Register Name: CCI_RSV_REG
Bit	Read/ Write	Default/H ex	Description
31:0	R/W	/	From 0x200 to 0x220 address, normal TWI registers are copied here. All transmission will be act like hardware controlling these registers. And don't change them in transmission.

Chapter 7

Interfaces

This chapter describes the external peripherals of A23 processor, including:

- SD 3.0
- TWI
- SPI
- UART
- USB OTG
- USB Host
- Digital audio interface
- RSB

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7.1 SD/MMC

7.1.1 Overview

The A23 processor comes with three SD/MMC controllers.

The SD/MMC controller can be configured as a Secure Digital Multimedia Card controller, which simultaneously supports Secure Digital memory (SD Memo), UHS-1 Card, Secure Digital I/O (SDIO), Multimedia Cards (MMC), eMMC Card and Consumer Electronics Advanced Transport Architecture (CE-ATA).

The SD3.0 controller includes the following features:

- Support Secure Digital memory protocol commands (up to SD3.0)
- Support Secure Digital I/O protocol commands
- Support multimedia card protocol commands (up to MMC4.41)
- Support CE-ATA digital protocol commands
- Support eMMC boot operation and alternative boot operation
- Support Command Completion signal and interrupt to host processor and Command Completion Signal disable feature
- Support one SD (Version1.0 to 3.0) or MMC (Version3.3 to 4.41) or CE-ATA device
- Support hardware CRC generation and error detection
- Support programmable baud rate
- Support host pull-up control
- Support SDIO interrupts in 1-bit and 4-bit modes
- Support SDIO suspend and resume operation
- Support SDIO read wait
- Support block size of 1 to 65535 bytes
- Support descriptor-based internal DMA controller
- Internal 128 bytes FIFO for data transfer
- Support 3.3 V IO pad

7.1.2 SD3.0 Timing Diagram

Please refer to relative specification:

- Physical Layer Specification Ver3.00 Final, 2009.04.16
- SDIO Specification Ver2.00
- Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
- Multimedia Cards (MMC – version 4.2)
- JEDEC Standard – JESD84-44, Embedded Multimedia Card (eMMC) Card Product Standard

7.2 TWI

7.2.1 Overview

This TWI controller can be used as an interface between CPU host and the serial TWI bus. It can support all the standard TWI transfer, including Slave and Master. The communication to the TWI bus is carried out on a byte-wise basis using interrupt or polled handshaking. This TWI Controller can be operated in standard mode (100Kbps) or fast-mode, supporting data rate up to 400Kbps. Multiple Masters and 10-bit addressing Mode are supported for this specified application. General Call Addressing is also supported in Slave mode.

The TWI controller includes the following features:

- Software-programmable for Slave or Master
- Supports Repeated START signal
- Multi-master systems supported
- Allows 10-bit addressing with TWI bus
- Performs arbitration and clock synchronization
- Own address and General Call address detection
- Interrupt on address detection
- Supports speeds up to 400Kbits/s ('fast mode')
- Allows operation from a wide range of input clock frequencies

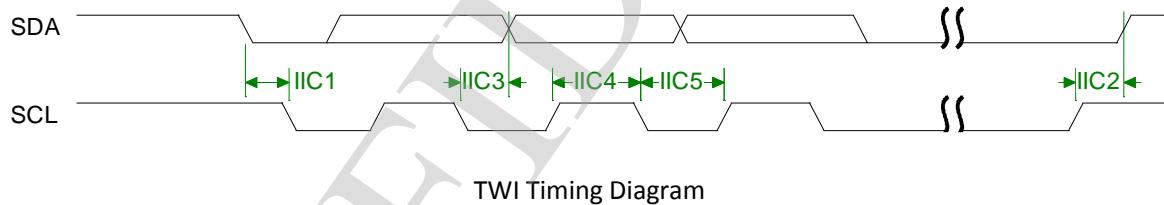
7.2.2 TWI Controller Timing Diagram

Data transferred are always in a unit of 8-bit (byte), followed by an acknowledge bit. The number of bytes that can be transmitted per transfer is unrestricted. Data is transferred in serial with the MSB first. Between each byte of data transfer, a receiver device will hold the clock line SCL low to force the transmitter into a wait state while waiting the response from microprocessor.

Data transfer with acknowledge is obligatory. The clock line is driven by the master all the time, including the acknowledge-related clock cycle, except for the SCL holding between each bytes. After sending each byte, the transmitter releases the SDA line to allow the receiver to pull down the SDA line and send an acknowledge signal (or leave it high to send a "not acknowledge") to the transmitter.

When a slave receiver doesn't acknowledge the slave address (unable to receive because of no resource available), the data line must be left high by the slave so that the master can then generate a STOP condition to abort the transfer. Slave receiver can also indicate not to want to send more data during a transfer by leave the acknowledge signal high. And the master should generate the STOP condition to abort the transfer.

Below diagram provides an illustration the relation of SDA signal line and SCL signal line on the TWI serial bus.



7.2.3 TWI Controller Register List

Module Name	Base Address
TWI0	0x01C2AC00
TWI1	0x01C2B000
TWI2	0x01C2B400

Register Name	Offset	Description
TWI_ADDR	0x0000	TWI Slave address
TWI_XADDR	0x0004	TWI Extended slave address
TWI_DATA	0x0008	TWI Data byte
TWI_CNTR	0x000C	TWI Control register
TWI_STAT	0x0010	TWI Status register
TWI_CCR	0x0014	TWI Clock control register
TWI_SRST	0x0018	TWI Software reset
TWI_EFR	0x001C	TWI Enhance Feature register
TWI_LCR	0x0020	TWI Line Control register

7.2.4 TWI Controller Register Description

TWI SLAVE ADDRESS REGISTER

Offset: 0x00			Register Name: TWI_ADDR Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
7:1	R/W	0	SLA Slave address 7-bit addressing SLA6, SLA5, SLA4, SLA3, SLA2, SLA1, SLA0 10-bit addressing 1, 1, 1, 1, 0, SLAX[9:8]
0	R/W	0	GCE General call address enable 0: Disable 1: Enable

Note:

For 7-bit addressing:

SLA6 – SLA0 is the 7-bit address of the TWI when in slave mode. When the TWI receives this address after a START condition, it will generate an interrupt and enter slave mode. (SLA6 corresponds to the first bit received from the TWI bus.) If GCE is set to '1', the TWI will also recognize the general call address (00h).

For 10-bit addressing:

When the address received starts with 11110b, the TWI recognizes this as the first part of a 10-bit address and if the next two bits match ADDR[2:1] (i.e. SLAX9 and SLAX8 of the device's extended address), it sends an ACK. (The device does not generate an interrupt at this point.) If the next byte of the address matches the XADDR register (SLAX7 – SLAX0), the TWI generates an interrupt and goes into slave mode.

TWI EXTEND ADDRESS REGISTER

Offset: 0x04			Register Name: TWI_XADDR
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0	SLAX Extend Slave Address SLAX[7:0]

TWI DATA REGISTER

Offset: 0x08			Register Name: TWI_DATA
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0	TWI_DATA Data byte for transmitting or received

TWI CONTROL REGISTER

Offset: 0x0C			Register Name: TWI_CNTR
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0	INT_EN Interrupt Enable 1'b0: The interrupt line always low 1'b1: The interrupt line will go high when INT_FLAG is set.
6	R/W	0	BUS_EN TWI Bus Enable 1'b0: The TWI bus inputs ISDA/ISCL are ignored and the TWI

			<p>Controller will not respond to any address on the bus</p> <p>1'b1: The TWI will respond to calls to its slave address – and to the general call address if the GCE bit in the ADDR register is set.</p> <p>Notes: In master operation mode, this bit should be set to '1'</p>
5	R/W	0	<p>M_STA</p> <p>Master Mode Start</p> <p>When M_STA is set to '1', TWI Controller enters master mode and will transmit a START condition on the bus when the bus is free. If the M_STA bit is set to '1' when the TWI Controller is already in master mode and one or more bytes have been transmitted, then a repeated START condition will be sent. If the M_STA bit is set to '1' when the TWI is being accessed in slave mode, the TWI will complete the data transfer in slave mode then enter master mode when the bus has been released.</p> <p>The M_STA bit is cleared automatically after a START condition has been sent: writing a '0' to this bit has no effect.</p>
4	R/W	0	<p>M_STP</p> <p>Master Mode Stop</p> <p>If M_STP is set to '1' in master mode, a STOP condition is transmitted on the TWI bus. If the M_STP bit is set to '1' in slave mode, the TWI will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the TWI bus. If both M_STA and M_STP bits are set, the TWI will first transmit the STOP condition (if in master mode) then transmit the START condition.</p> <p>The M_STP bit is cleared automatically: writing a '0' to this bit has no effect.</p>
3	R/W	0	<p>INT_FLAG</p> <p>Interrupt Flag</p> <p>INT_FLAG is automatically set to '1' when any of 28 (out of the possible 29) states is entered (see 'STAT Register' below). The only state that does not set INT_FLAG is state F8h. If the</p>

			INT_EN bit is set, the interrupt line goes high when IFLG is set to '1'. If the TWI is operating in slave mode, data transfer is suspended when INT_FLAG is set and the low period of the TWI bus clock line (SCL) is stretched until '1' is written to INT_FLAG. The TWI clock line is then released and the interrupt line goes low.
			<p>A_ACK</p> <p>Assert Acknowledge</p> <p>When A_ACK is set to '1', an Acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the TWI bus if:</p> <ol style="list-style-type: none"> 1. Either the whole of a matching 7-bit slave address or the first or the second byte of a matching 10-bit slave address has been received. 2. The general call address has been received and the GCE bit in the ADDR register is set to '1'. 3. A data byte has been received in master or slave mode. <p>When A_ACK is '0', a Not Acknowledge (high level on SDA) will be sent when a data byte is received in master or slave mode.</p> <p>If A_ACK is cleared to '0' in slave transmitter mode, the byte in the DATA register is assumed to be the 'last byte'. After this byte has been transmitted, the TWI will enter state C8h then return to the idle state (status code F8h) when INT_FLAG is cleared.</p>
2	R/W	0	The TWI will not respond as a slave unless A_ACK is set.
1:0	R/W	0	/

TWI STATUS REGISTER

Offset: 0x10	Register Name: TWI_STAT Default Value: 0x0000_00F8
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Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0xF8	<p>STA</p> <p>Status Information Byte</p> <p>Code Status</p> <p>0x00: Bus error</p> <p>0x08: START condition transmitted</p> <p>0x10: Repeated START condition transmitted</p> <p>0x18: Address + Write bit transmitted, ACK received</p> <p>0x20: Address + Write bit transmitted, ACK not received</p> <p>0x28: Data byte transmitted in master mode, ACK received</p> <p>0x30: Data byte transmitted in master mode, ACK not received</p> <p>0x38: Arbitration lost in address or data byte</p> <p>0x40: Address + Read bit transmitted, ACK received</p> <p>0x48: Address + Read bit transmitted, ACK not received</p> <p>0x50: Data byte received in master mode, ACK transmitted</p> <p>0x58: Data byte received in master mode, not ACK transmitted</p> <p>0x60: Slave address + Write bit received, ACK transmitted</p> <p>0x68: Arbitration lost in address as master, slave address + Write bit received, ACK transmitted</p> <p>0x70: General Call address received, ACK transmitted</p> <p>0x78: Arbitration lost in address as master, General Call address received, ACK transmitted</p> <p>0x80: Data byte received after slave address received, ACK transmitted</p> <p>0x88: Data byte received after slave address received, not ACK transmitted</p> <p>0x90: Data byte received after General Call received, ACK transmitted</p> <p>0x98: Data byte received after General Call received, not ACK transmitted</p>

		<p>0xA0: STOP or repeated START condition received in slave mode</p> <p>0xA8: Slave address + Read bit received, ACK transmitted</p> <p>0xB0: Arbitration lost in address as master, slave address + Read bit received, ACK transmitted</p> <p>0xB8: Data byte transmitted in slave mode, ACK received</p> <p>0xC0: Data byte transmitted in slave mode, ACK not received</p> <p>0xC8: Last byte transmitted in slave mode, ACK received</p> <p>0xD0: Second Address byte + Write bit transmitted, ACK received</p> <p>0xD8: Second Address byte + Write bit transmitted, ACK not received</p> <p>0xF8: No relevant status information, INT_FLAG=0</p> <p>Others: Reserved</p>
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TWI CLOCK REGISTER

Offset: 0x14			Register Name: TWI_CCR
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:7	/	/	/
6:3	R/W	0	CLK_M
2:0	R/W	0	<p>CLK_N</p> <p>The TWI bus is sampled by the TWI at the frequency defined by F0:</p> $F_{samp} = F_0 = F_{in} / 2^{CLK_N}$ <p>The TWI OSCL output frequency, in master mode, is F1 / 10:</p> $F_1 = F_0 / (CLK_M + 1)$ $F_{oscl} = F_1 / 10 = F_{in} / (2^{CLK_N} * (CLK_M + 1) * 10)$ <p>For Example:</p> $F_{in} = 48\text{Mhz} \text{ (APB clock input)}$

		For 400kHz full speed 2Wire, CLK_N = 2, CLK_M=2 $F_0 = 48M/2^2=12\text{Mhz}$, $F_1 = F_0/(10*(2+1)) = 0.4\text{Mhz}$ For 100Khz standard speed 2Wire, CLK_N=2, CLK_M=11 $F_0=48M/2^2=12\text{Mhz}$, $F_1=F_0/(10*(11+1)) = 0.1\text{Mhz}$	
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TWI SOFT RESET REGISTER

Offset: 0x18			Register Name: TWI_SRST Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:1	/	/	/
0	R/W	0	SOFT_RST Soft Reset Write '1' to this bit to reset the TWI and clear to '0' when completing Soft Reset operation.

TWI ENHANCE FEATURE REGISTER

Offset: 0x1C			Register Name: TWI_EFR Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:2	/	/	/
0:1	R/W	0	DBN Data Byte number follow Read Command Control No Data Byte to be written after read command Only 1 byte data to be written after read command 2 bytes data can be written after read command 3 bytes data can be written after read command

TWI LINE CONTROL REGISTER

Offset: 0x20			Register Name: TWI_LCR
Default Value: 0x0000_003a			
Bit	Read/Write	Default	Description
31:6	/	/	/
5	R	1	<p>SCL_STATE</p> <p>Current state of TWI_SCL</p> <p>0 – low</p> <p>1 - high</p>
4	R	1	<p>SDA_STATE</p> <p>Current state of TWI_SDA</p> <p>0 – low</p> <p>1 - high</p>
3	R/W	1	<p>SCL_CTL</p> <p>TWI_SCL line state control bit</p> <p>When line control mode is enabled (bit[2] set), value of this bit decide the output level of TWI_SCL</p> <p>0 – output low level</p> <p>1 – output high level</p>
2	R/W	0	<p>SCL_CTL_EN</p> <p>TWI_SCL line state control enable</p> <p>When this bit is set, the state of TWI_SCL is control by the value of bit[3].</p> <p>0-disable TWI_SCL line control mode</p> <p>1-enable TWI_SCL line control mode</p>
1	R/W	1	<p>SDA_CTL</p> <p>TWI_SDA line state control bit</p> <p>When line control mode is enabled (bit[0] set), value of this bit decide the output level of TWI_SDA</p> <p>0 – output low level</p>

			1 – output high level
0	R/W	0	<p>SDA_CTL_EN</p> <p>TWI_SDA line state control enable</p> <p>When this bit is set, the state of TWI_SDA is control by the value of bit[1].</p> <p>0-disable TWI_SDA line control mode</p> <p>1-enable TWI_SDA line control mode</p>

TWI DVFS CONTROL REGISTER

Offset: 0x24			Register Name: TWI_DVFSCR
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:2	/	/	/
2	R/W	0	<p>MS_PRIORITY</p> <p>CPU and DVFS BUSY set priority select</p> <p>0: CPU has higher priority</p> <p>1: DVFS has higher priority</p>
1	R/W	0	CPU_BUSY_SET
0	R/W	0	DVFC_BUSY_SET

Note: This register is only implemented in TWI0.

7.2.5 TWI Controller Special Requirement

TWI PIN LIST

Port Name	Width	Direction	Description
TWI_SCL	1	IN/OUT	TWI Clock line
TWI_SDA	1	IN/OUT	TWI Serial Data line

TWI CONTROLLER OPERATION

There are four operation modes on the TWI bus which dictates the communications method. They are Master Transmit, Master Receive, Slave Transmit and Slave Receive. In general, CPU host controls TWI by writing commands and data to its registers. The TWI interrupts the CPU host for the attention each time a byte transfer is done or a START/STOP conditions is detected. The CPU host can also poll the status register for current status if the interrupt mechanism is not disabled by the CPU host.

When the CPU host wants to start a bus transfer, it initiates a bus START to enter the master mode by setting IM_STA bit in the 2WIRE_CNTR register to high (before it must be low). The TWI will assert INT line and INT_FLAG to indicate a completion for the START condition and each consequent byte transfer. At each interrupt, the micro-processor needs to check the 2WIRE_STAT register for current status. A transfer has to be concluded with STOP condition by setting M_STP bit high.

In Slave Mode, the TWI also constantly samples the bus and look for its own slave address during addressing cycles. Once a match is found, it is addressed and interrupt the CPU host with the corresponding status. Upon request, the CPU host should read the status, read/write 2WIRE_DATA data register, and set the 2WIRE_CNTR control register. After each byte transfer, a slave device always halt the operation of remote master by holding the next low pulse on SCL line until the microprocessor responds to the status of previous byte transfer or START condition.

7.3 SPI

7.3.1 Overview

The SPI (Serial Peripheral Interface) allows rapid data communication with fewer software interrupts. The SPI module contains one 64x8 receiver buffer (RXFIFO) and one 64x8 transmit buffer (TXFIFO). It can work at two modes: Master mode and Slave mode.

It includes the following features:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- Four chip selects to support multiple peripherals for SPI0 and SPI1 has one chip select
- 8-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SPI_SS) and SPI Clock (SPI_SCLK) are configurable
- Support dedicated DMA

7.3.2 SPI Timing Diagram

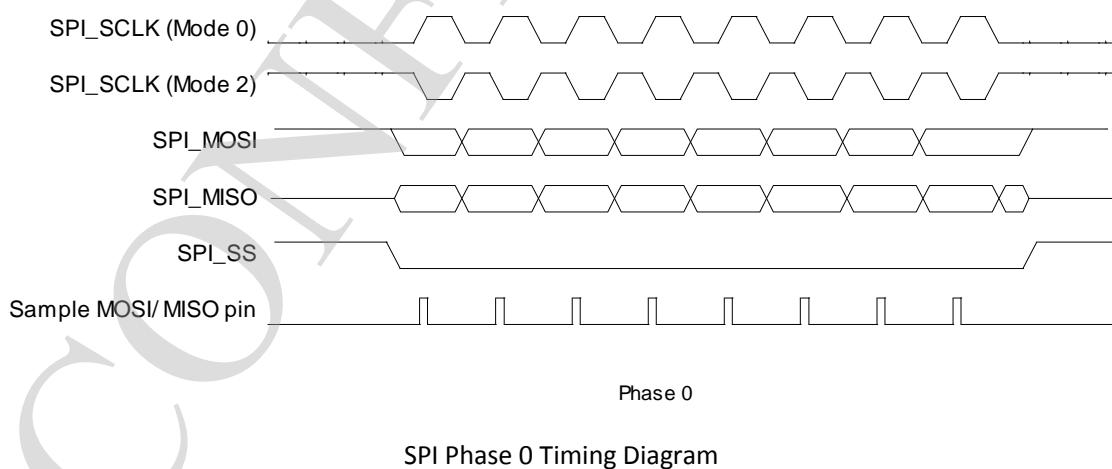
The serial peripheral interface master uses the SPI_SCLK signal to transfer data in and out of the shift register. Data is clocked using any one of four programmable clock phase and polarity combinations.

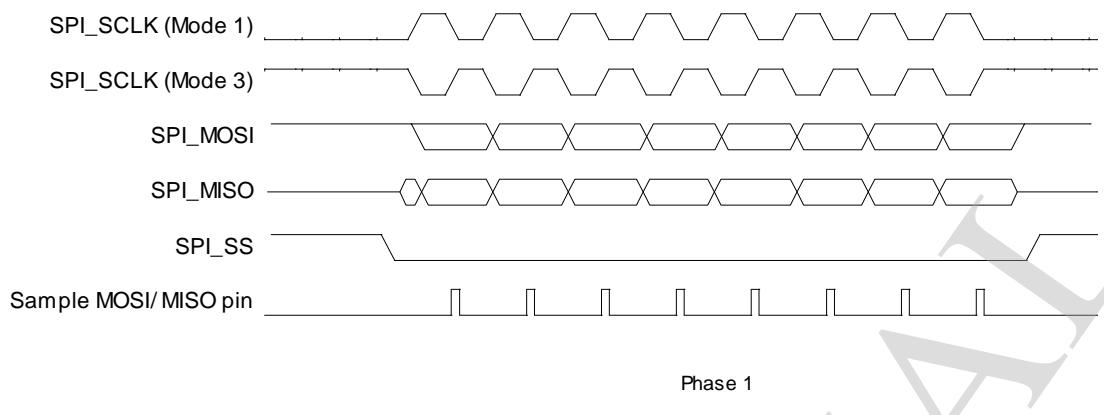
During Phase 0, Polarity 0 and Phase 1, Polarity 1 operations, output data changes on the falling clock edge and input data is shifted in on the rising edge.

During Phase 1, Polarity 0 and Phase 0, Polarity 1 operations, output data changes on the rising edges of the clock and is shifted in on falling edges.

The POL defines the signal polarity when SPI_SCLK is in idle state. The SPI_SCLK is high level when POL is '1' and it is low level when POL is '0'. The PHA decides whether the leading edge of SPI_SCLK is used for setup or sample data. The leading edge is used for setup data when PHA is '1' and for sample data when PHA is '0'. The four modes are listed below:

SPI Mode	POL	PHA	Leading Edge	Trailing Edge
0	0	0	Rising, Sample	Falling, Setup
1	0	1	Rising, Setup	Falling, Sample
2	1	0	Falling, Sample	Rising, Setup
3	1	1	Falling, Setup	Rising, Sample





7.3.3 SPI Register List

Module Name	Base Address
SPI0	0x01C68000
SPI1	0x01C69000

Register Name	Offset	Description
SPI_VER	0x00	SPI Version Number Register
SPI_GCR	0x04	SPI Global Control Register
SPI_TCR	0x08	SPI Transfer Control register
/	0x0c	reserved
SPI_IER	0x10	SPI Interrupt Control register
SPI_ISR	0x14	SPI Interrupt Status register
SPI_FCR	0x18	SPI FIFO Control register
SPI_FSR	0x1C	SPI FIFO Status register
SPI_WCR	0x20	SPI Wait Clock Counter register
SPI_CCR	0x24	SPI Clock Rate Control register
/	0x28	reserved
/	0x2c	reserved
SPI_MBC	0x30	SPI Burst Counter register
SPI_MTC	0x34	SPI Transmit Counter Register
SPI_BCC	0x38	SPI Burst Control register
SPI_TXD	0x200	SPI TX Data register
SPI_RXD	0x300	SPI RX Data register

7.3.4 SPI Register Description

SPI VERSION NUMBER REGISTER

Offset: 0x00			Register Name: SPI_VER
			Default Value: 0x0000_0080
Bit	Read/Write	Default	Description
31:16	R	0	VER_H
15:0	R	0	VER_L

SPI GLOBAL CONTROL REGISTER

Offset: 0x04			Register Name: SPI_CTL
			Default Value: 0x0000_0080
Bit	Read/Write	Default	Description
31	R/W	0	<p>SRST Soft reset Write '1' to this bit will clear the SPI controller, and auto clear to '0' when reset operation completes Write '0' has no effect.</p>
30:8	/	/	/
7	R/W	1	<p>TP_EN Transmit Pause Enable In master mode, it is used to control transmit state machine to stop smart burst sending when RX FIFO is full. 1 – stop transmit data when RXFIFO full 0 – normal operation, ignore RXFIFO status Note: Can't be written when XCH=1</p>
6:2	/	/	/
1	R/W	0	MODE

			SPI Function Mode Select 0: Slave Mode 1: Master Mode Note: Can't be written when XCH=1
0	R/W	0	EN SPI Module Enable Control 0: Disable 1: Enable

SPI TRANSFER CONTROL REGISTER

Offset: 0x08			Register Name: SPI_INTCTL
Default Value: 0x0000_2087			
Bit	Read/Write	Default	Description
31	R/W	0x0	XCH Exchange Burst In master mode it is used to start SPI burst 0: Idle 1: Initiates exchange. Write "1" to this bit will start the SPI burst, and will auto clear after finishing the bursts transfer specified by BC. Write "1" to SRST will also clear this bit. Write '0' to this bit has no effect. Note: Can't be written when XCH=1.
30:14	R	0x0	Reserved.
13	R/W	0x1	SDM Master Sample Data Mode 1-Normal Sample Mode 0-Delay Sample Mode In Normal Sample Mode,SPI Master samples the data at the correct edge for each SPI mode.

			In Delay Sample Mode,SPI master samples data at the edge that is half cycle delayed by the correct edge defined in respective SPI mode.
12	R/W	0x0	<p>FBS</p> <p>First Transmit Bit Select</p> <p>0: MSB first</p> <p>1: LSB first</p> <p>Note: Can't be written when XCH=1.</p>
11	R/W	0x0	<p>SDC</p> <p>Master Sample Data Control</p> <p>Set this bit to '1' to make the internal read sample point with a delay of half cycle of SPI_CLK. It is used in high speed read operation to reduce the error caused by the time delay of SPI_CLK propagating between master and slave.</p> <p>0 – normal operation, do not delay internal read sample point</p> <p>1 – delay internal read sample point</p> <p>Note: Can't be written when XCH=1.</p>
10	R/W	0x0	<p>RPSM</p> <p>Rapids mode select</p> <p>Select RapidS mode for high speed write.</p> <p>0: normal write mode</p> <p>1: rapids write mode</p> <p>Note: Can't be written when XCH=1.</p>
9	R/W	0x0	<p>DDB</p> <p>Dummy Burst Type</p> <p>0: The bit value of dummy SPI burst is zero</p> <p>1: The bit value of dummy SPI burst is one</p> <p>Note: Can't be written when XCH=1.</p>
8	R/W	0x0	<p>DHB</p> <p>Discard Hash Burst</p> <p>In master mode it controls whether discarding unused SPI</p>

			<p>bursts</p> <p>0: Receiving all SPI bursts in BC period</p> <p>1: Discard unused SPI bursts, only fetching the SPI bursts during dummy burst period. The bursts number is specified by TC.</p> <p>Note: Can't be written when XCH=1.</p>
7	R/W	0x1	<p>SS_LEVEL</p> <p>When control SS signal manually (SPI_CTRL_REG.SS_CTRL==1), set this bit to '1' or '0' to control the level of SS signal.</p> <p>0: set SS to low</p> <p>1: set SS to high</p> <p>Note: Can't be written when XCH=1.</p>
6	R/W	0x0	<p>SS_OWNER</p> <p>SS Output Owner Select</p> <p>Usually, controller sends SS signal automatically with data together. When this bit is set to 1, software must manually write SPI_CTRL_REG.SS_LEVEL to 1 or 0 to control the level of SS signal.</p> <p>0: SPI controller</p> <p>1: Software</p> <p>Note: Can't be written when XCH=1.</p>
5:4	R/W	0x0	<p>SS_SEL</p> <p>SPI Chip Select</p> <p>Select one of four external SPI Master/Slave Devices</p> <p>00: SPI_SS0 will be asserted</p> <p>01: SPI_SS1 will be asserted</p> <p>10: SPI_SS2 will be asserted</p> <p>11: SPI_SS3 will be asserted</p> <p>Note: Can't be written when XCH=1.</p>
3	R/W	0x0	<p>SSCTL</p> <p>In master mode, this bit selects the output wave form for the</p>

			SPI_SSx signal. Only valid when SS_OWNER = 0. 0: SPI_SSx remains asserted between SPI bursts 1: Negate SPI_SSx between SPI bursts Note: Can't be written when XCH=1.
2	R/W	0x1	SPOL SPI Chip Select Signal Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Note: Can't be written when XCH=1.
1	R/W	0x1	CPOL SPI Clock Polarity Control 0: Active high polarity (0 = Idle) 1: Active low polarity (1 = Idle) Note: Can't be written when XCH=1.
0	R/W	0x1	CPHA SPI Clock/Data Phase Control 0: Phase 0 (Leading edge for sample data) 1: Phase 1 (Leading edge for setup data) Note: Can't be written when XCH=1.

SPI INTERRUPT CONTROL REGISTER

Offset: 0x010			Register Name: SPI_IER
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:14	R	0x0	Reserved.
13	R/W	0x0	SS_INT_EN SSI Interrupt Enable Chip Select Signal (SSx) from valid state to invalid state 0: Disable

			1: Enable
12	R/W	0x0	<p>TC_INT_EN Transfer Completed Interrupt Enable</p> <p>0: Disable 1: Enable</p>
11	R/W	0x0	<p>TF_UDR_INT_EN TXFIFO under run Interrupt Enable</p> <p>0: Disable 1: Enable</p>
10	R/W	0x0	<p>TF_OVF_INT_EN TX FIFO Overflow Interrupt Enable</p> <p>0: Disable 1: Enable</p>
9	R/W	0x0	<p>RF_UDR_INT_EN RXFIFO under run Interrupt Enable</p> <p>0: Disable 1: Enable</p>
8	R/W	0x0	<p>RF_OVF_INT_EN RX FIFO Overflow Interrupt Enable</p> <p>0: Disable 1: Enable</p>
7	R	0x0	Reserved.
6	R/W	0x0	<p>TF_FUL_INT_EN TX FIFO Full Interrupt Enable</p> <p>0: Disable 1: Enable</p>
5	R/W	0x0	<p>TX_EMP_INT_EN TX FIFO Empty Interrupt Enable</p> <p>0: Disable</p>

			1: Enable
4	R/W	0x0	<p>TX_ERQ_INT_EN TX FIFO Empty Request Interrupt Enable</p> <p>0: Disable 1: Enable</p>
3	R	0x0	Reserved
2	R/W	0x0	<p>RF_FUL_INT_EN RX FIFO Full Interrupt Enable</p> <p>0: Disable 1: Enable</p>
1	R/W	0x0	<p>RX_EMP_INT_EN RX FIFO Empty Interrupt Enable</p> <p>0: Disable 1: Enable</p>
0	R/W	0x0	<p>RF_RDY_INT_EN RX FIFO Ready Request Interrupt Enable</p> <p>0: Disable 1: Enable</p>

SPI INTERRUPT STATUS REGISTER

Offset: 0x14			Register Name: SPI_INT_STA
			Default Value: 0x0000_0022
Bit	Read/Write	Default	Description
31:14	/	0	/
13	R/W	0	<p>SSI SS Invalid Interrupt</p> <p>When SSI is 1, it indicates that SS has changed from valid state to invalid state. Writing 1 to this bit clears it.</p>
12	R/W	0	TC

			<p>Transfer Completed</p> <p>In master mode, it indicates that all bursts specified by BC has been exchanged. In other condition, When set, this bit indicates that all the data in TXFIFO has been loaded in the Shift register, and the Shift register has shifted out all the bits. Writing 1 to this bit clears it.</p> <p>0: Busy</p> <p>1: Transfer Completed</p>
11	R/W	0	<p>TF_UDF</p> <p>TXFIFO under run</p> <p>This bit is set when if the TXFIFO is underrun. Writing 1 to this bit clears it.</p> <p>0: TXFIFO is not underrun</p> <p>1: TXFIFO is underrun</p>
10	R/W	0	<p>TF_OVF</p> <p>TXFIFO Overflow</p> <p>This bit is set when if the TXFIFO is overflow. Writing 1 to this bit clears it.</p> <p>0: TXFIFO is not overflow</p> <p>1: TXFIFO is overflowed</p>
9	R/W	0	<p>RX_UDF</p> <p>RXFIFO Underrun</p> <p>When set, this bit indicates that RXFIFO has underrun. Writing 1 to this bit clears it.</p>
8	R/W	0	<p>RX_OVF</p> <p>RXFIFO Overflow</p> <p>When set, this bit indicates that RXFIFO has overflowed. Writing 1 to this bit clears it.</p> <p>0: RXFIFO is available.</p> <p>1: RXFIFO has overflowed.</p>
7	/	/	/
6	R/W	0	TX_FULL

			<p>TXFIFO Full</p> <p>This bit is set when if the TXFIFO is full. Writing 1 to this bit clears it.</p> <p>0: TXFIFO is not Full 1: TXFIFO is Full</p>
5	R/W	1	<p>TX_EMP</p> <p>TXFIFO Empty</p> <p>This bit is set if the TXFIFO is empty. Writing 1 to this bit clears it.</p> <p>0: TXFIFO contains one or more words. 1: TXFIFO is empty</p>
4	R/W	0	<p>TX_READY</p> <p>TXFIFO Ready</p> <p>0: $\text{TX_WL} > \text{TX_TRIG_LEVEL}$ 1: $\text{TX_WL} \leq \text{TX_TRIG_LEVEL}$</p> <p>This bit is set any time if $\text{TX_WL} \leq \text{TX_TRIG_LEVEL}$. Writing "1" to this bit clears it. Where TX_WL is the water level of RXFIFO</p>
3	/	/	reserved
2	R/W	0	<p>RX_FULL</p> <p>RXFIFO Full</p> <p>This bit is set when the RXFIFO is full. Writing 1 to this bit clears it.</p> <p>0: Not Full 1: Full</p>
1	R/W	1	<p>RX_EMP</p> <p>RXFIFO Empty</p> <p>This bit is set when the RXFIFO is empty. Writing 1 to this bit clears it.</p> <p>0: Not empty 1: empty</p>
0	R/W	0	RX_RDY

			<p>RXFIFO Ready</p> <p>0: RX_WL < RX_TRIG_LEVEL</p> <p>1: RX_WL >= RX_TRIG_LEVEL</p> <p>This bit is set any time if RX_WL >= RX_TRIG_LEVEL. Writing "1" to this bit clears it. Where RX_WL is the water level of RXFIFO.</p>
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SPI FIFO CONTROL REGISTER

Offset: 0x18			Register Name: SPI_DMACTL
Default Value: 0x0040_0001			
Bit	Read/Write	Default	Description
31	R/W	0	<p>TX_FIFO_RST</p> <p>TX FIFO Reset</p> <p>Write '1' to this bit will reset the control portion of the TX FIFO and auto clear to '0' when completing reset operation, write to '0' has no effect.</p>
30	R/W	0	<p>TF_TEST_ENB</p> <p>TX Test Mode Enable</p> <p>0: disable</p> <p>1: enable</p> <p>Note: In normal mode, TX FIFO can only be read by SPI controller, write '1' to this bit will switch TX FIFO read and write function to AHB bus. This bit is used to test the TX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.</p>
29:25	/	/	/
24	R/W	0x0	<p>TF_DRQ_EN</p> <p>TX FIFO DMA Request Enable</p> <p>0: Disable</p> <p>1: Enable</p>
23:16	R/W	0x40	TX_TRIG_LEVEL

			TX FIFO Empty Request Trigger Level
15	W/R	0x0	<p>RF_RST</p> <p>RXFIFO Reset</p> <p>Write '1' to this bit will reset the control portion of the receiver FIFO, and auto clear to '0' when completing reset operation, write '0' to this bit has no effect.</p>
14	W/R	0x0	<p>RF_TEST</p> <p>RX Test Mode Enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>Note: In normal mode, RX FIFO can only be written by SPI controller, write '1' to this bit will switch RX FIFO read and write function to AHB bus. This bit is used to test the RX FIFO, don't set in normal operation and don't set RF_TEST and TF_TEST at the same time.</p>
13:10	R	0x0	Reserved
9	W/R	0x0	<p>RX_DMA_MODE</p> <p>SPI RX DMA Mode Control</p> <p>0: Normal DMA mode</p> <p>1: Dedicate DMA mode</p>
8	R/W	0x0	<p>RF_DRQ_EN</p> <p>RX FIFO DMA Request Enable</p> <p>0: Disable</p> <p>1: Enable</p>
7:0	R/W	0x1	<p>RX_TRIG_LEVEL</p> <p>RX FIFO Ready Request Trigger Level</p>

SPI FIFO STATUS REGISTER

Offset: 0x1c		Register Name: SPI_FSR	
		Default Value: 0x0000_0000	
Bit	Read/Write	Default	Description

31	R	0x0	TB_WR TX FIFO Write Buffer Write Enable
30:28	R	0x0	TB_CNT TX FIFO Write Buffer Counter These bits indicate the number of words in TX FIFO Write Buffer
27:24	R	0x0	Reserved
23:16	R	0x0	TF_CNT TX FIFO Counter These bits indicate the number of words in TX FIFO 0: 0 byte in TX FIFO 1: 1 byte in TX FIFO ... 127: 127 bytes in TX FIFO
15	R	0x0	RB_WR RX FIFO Read Buffer Write Enable
14:12	R	0x0	RB_CNT RX FIFO Read Buffer Counter These bits indicate the number of words in RX FIFO Read Buffer
11:8	R	0x0	Reserved
7:0	R	0x0	RF_CNT RX FIFO Counter These bits indicate the number of words in RX FIFO 0: 0 byte in RX FIFO 1: 1 byte in RX FIFO ... 127: 127 bytes in RX FIFO

SPI WAIT CLOCK REGISTER

Offset: 0x20			Register Name: SPI_WAIT
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
31:20	/	/	/
19:16	R/W	0x0	<p>SWC Dual mode direction switch wait clock counter (for master mode only). 0: No wait states inserted n: n SPI_SCLK wait states inserted Note: These bits control the number of wait states to be inserted before start dual data transfer in dual SPI mode. The SPI module counts SPI_SCLK by SWC for delaying next word data transfer. Note: Can't be written when XCH=1.</p>
15:0	R/W	0	<p>WCC Wait Clock Counter (In Master mode) These bits control the number of wait states to be inserted in data transfers. The SPI module counts SPI_SCLK by WCC for delaying next word data transfer. 0: No wait states inserted N: N SPI_SCLK wait states inserted</p>

SPI CLOCK CONTROL REGISTER

Offset: 0x24			Register Name: SPI_CCTL
Default Value: 0x0000_0002			
Bit	Read/Write	Default	Description
31:13	/	/	/
12	R/W	0	<p>DRS Divide Rate Select (Master Mode Only) 0: Select Clock Divide Rate 1</p>

			1: Select Clock Divide Rate 2
11:8	R/W	0	<p>CDR1</p> <p>Clock Divide Rate 1 (Master Mode Only)</p> <p>This field selects the baud rate of the SPI_SCLK based on a division of the AHB_CLK. These bits allow SPI to synchronize with different external SPI devices. The max frequency is one quarter of AHB_CLK. The divide ratio is determined according to the following table using the equation: 2^n. The SPI_SCLK is determined according to the following equation: $SPI_CLK = AHB_CLK / 2^n$.</p>
7:0	R/W	0x2	<p>CDR2</p> <p>Clock Divide Rate 2 (Master Mode Only)</p> <p>The SPI_SCLK is determined according to the following equation: $SPI_CLK = AHB_CLK / (2^{(n+1)})$.</p>

SPI MASTER BURST COUNTER REGISTER

Offset: 0x30			Register Name: SPI_BC
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:24	/	/	/
23:0	R/W	0	<p>MBC</p> <p>Master Burst Counter</p> <p>In master mode, this field specifies the total burst number when SMC is 1.</p> <p>0: 0 burst</p> <p>1: 1 burst</p> <p>...</p> <p>N: N bursts</p>

SPI MASTER TRANSMIT COUNTER REGISTER

Offset: 0x34		Register Name: SPI_TC
		Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:24	/	/	/
23:0	R/W	0	<p>MWTC Master Write Transmit Counter</p> <p>In master mode, this field specifies the burst number that should be sent to TXFIFO before automatically sending dummy burst when SMC is 1. For saving bus bandwidth, the dummy burst (all zero bits or all one bits) is sent by SPI Controller automatically.</p> <p>0: 0 burst 1: 1 burst ... N: N bursts</p>

SPI MASTER BURST CONTROL COUNTER REGISTER

Offset: 0x38			Register Name: SPI_BCC Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:29	R	0x0	Reserved
28	R/W	0x0	<p>DRM Master Dual Mode RX Enable</p> <p>0: RX use single-bit mode 1: RX use dual mode</p> <p>Note: Can't be written when XCH=1.</p>
27:24	R/W	0x0	<p>DBC Master Dummy Burst Counter</p> <p>In master mode, this field specifies the burst number that should be sent before receive in dual SPI mode. The data is don't care by the device.</p> <p>0: 0 burst 1: 1 burst</p>

			<p>...</p> <p>N: N bursts</p> <p>Note: Can't be written when XCH=1.</p>
23:0	R/W	0x0	<p>STC</p> <p>Master Single Mode Transmit Counter</p> <p>In master mode, this field specifies the burst number that should be sent in single mode before automatically sending dummy burst. This is the first transmit counter in all bursts.</p> <p>0: 0 burst</p> <p>1: 1 burst</p> <p>...</p> <p>N: N bursts</p> <p>Note: Can't be written when XCH=1.</p>

SPI TX DATA REGISTER

Offset: 0x200			Register Name: SPI_TXD
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	W/R	0x0	<p>TDATA</p> <p>Transmit Data</p> <p>This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are rooms in RXFIFO, one burst data is written to RXFIFO and the depth is increased by 1. In half-word accessing method, two SPI burst data are written and the TXFIFO depth is increase by 2. In word accessing method, four SPI burst data are written and the TXFIFO depth is increased by 4.</p> <p>Note: This address is writing-only if TF_TEST is '0', and if TF_TEST is set to '1', this address is readable and writable to test the TX FIFO through the AHB bus.</p>

SPI RX DATA REGISTER

			Register Name: SPI_RXD
Offset: 0x300			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	R	0	<p>RDATA Receive Data</p> <p>This register can be accessed in byte, half-word or word unit by AHB. In byte accessing method, if there are data in RXFIFO, the top word is returned and the RXFIFO depth is decreased by 1. In half-word accessing method, two SPI bursts are returned and the RXFIFO depth is decrease by 2. In word accessing method, the four SPI bursts are returned and the RXFIFO depth is decreased by 4.</p> <p>Note: This address is read-only if RF_TEST is '0', and if RF_TEST is set to '1', this address is readable and writable to test the RX FIFO through the AHB bus.</p>

7.3.5 SPI Special Requirement

SPI PIN LIST

The direction of SPI pin is different in two work modes: Master Mode and Slave Mode.

Port Name	Width	Direction(M)	Direction(S)	Description
SPI_SCLK	1	OUT	IN	SPI Clock
SPI_MOSI	1	OUT	IN	SPI Master Output Slave Input Data Signal
SPI_MISO	1	IN	OUT	SPI Master Input Slave Output Data Signal
SPI_SS[3:0]	4	OUT	IN	SPI Chip Select Signal

Note: SPI0 module has four chip select signals and SPI1 module has only one chip select signal for pin saving.

SPI MODULE CLOCK SOURCE AND FREQUENCY

The SPI module uses two clock sources: AHB_CLK and SPI_CLK. The SPI_SCLK can in the range from 3Khz to 100 MHZ and $\text{AHB_CLK} \geq 2 \times \text{SPI_SCLK}$.

Clock Name	Description	Requirement
AHB_CLK	AHB bus clock, as the clock source of SPI module	$\text{AHB_CLK} \geq 2 \times \text{SPI_SCLK}$
SPI_CLK	SPI serial input clock	

7.4 UART

7.4.1 Overview

The UART is used for serial communication with a peripheral, modem (data carrier equipment, DCE) or data set. Data is written from a master (CPU) over the APB bus to the UART and it is converted to serial form and transmitted to the destination device. Serial data is also received by the UART and stored for the master (CPU) to read back.

The UART contains registers to control the character length, baud rate, parity generation/checking, and interrupt generation. Although there is only one interrupt output signal from the UART, there are several prioritized interrupt types that can be responsible for its assertion. Each of the interrupt types can be separately enabled/disabled with the control registers.

The UART has 16450 and 16550 modes of operation, which are compatible with a range of standard software drivers. In 16550 mode, transmit and receive operations are both buffered by FIFOs. In 16450 mode, these FIFOs are disabled.

The UART supports word lengths from five to eight bits, an optional parity bit and 1, 1 ½ or 2 stop bits, and is fully programmable by an AMBA APB CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, together with separate transmit and receive FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided.

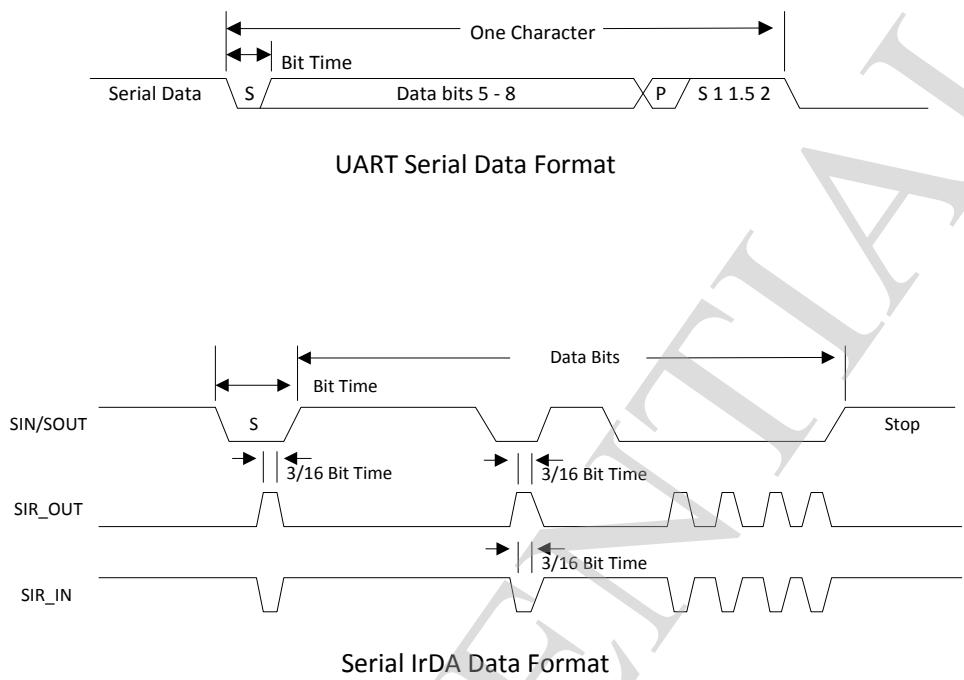
Interrupts can be generated for a range of TX Buffer/FIFO, RX Buffer/FIFO, Modem Status and Line Status conditions.

For integration in systems where Infrared SIR serial data format is required, the UART can be configured to have a software-programmable IrDA SIR Mode. If this mode is not selected, only the UART (RS232 standard) serial data format is available.

The UART includes the following features:

- Compatible with industry-standard 16550 UARTs
- 64-Bytes Transmit and receive data FIFOs
- DMA controller interface
- Software/ Hardware Flow Control
- Programmable Transmit Holding Register Empty interrupt
- Support IrDa 1.0 SIR
- Interrupt support for FIFOs, Status Change

7.4.2 UART Timing Diagram



7.4.3 UART Register List

There are 6 UART controllers. All UART controllers can be configured as Serial IrDA.

Module Name	Base Address	Notes
UART0		
UART1		
UART2		
UART3		
UART4		
R-UART		Accessed by CPUS

Register Name	Offset	Description
UART_RBR	0x00	UART Receive Buffer Register
UART_THR	0x00	UART Transmit Holding Register
UART_DLL	0x00	UART Divisor Latch Low Register
UART_DLH	0x04	UART Divisor Latch High Register
UART_IER	0x04	UART Interrupt Enable Register
UART_IIR	0x08	UART Interrupt Identity Register
UART_FCR	0x08	UART FIFO Control Register
UART_LCR	0x0C	UART Line Control Register
UART_MCR	0x10	UART Modem Control Register
UART_LSR	0x14	UART Line Status Register
UART_MSR	0x18	UART Modem Status Register
UART_SCH	0x1C	UART Scratch Register
UART_USR	0x7C	UART Status Register
UART_TFL	0x80	UART Transmit FIFO Level
UART_RFL	0x84	UART_RFL

UART_HALT	0xA4	UART Halt TX Register
/	0xB0	/
/	0xB4	/

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7.4.4 UART Register Description

UART RECEIVER BUFFER REGISTER

Offset: 0x00			Register Name: UART_RBR Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R	0	<p>RBR Receiver Buffer Register Data byte received on the serial input port (sin) in UART mode, or the serial infrared input (sir_in) in infrared mode. The data in this register is valid only if the Data Ready (DR) bit in the Line Status Register (LCR) is set.</p> <p>If in FIFO mode and FIFOs are enabled (FCR[0] set to one), this register accesses the head of the receive FIFO. If the receive FIFO is full and this register is not read before the next data character arrives, then the data already in the FIFO is preserved, but any incoming data are lost and an overrun error occurs.</p>

UART TRANSMIT HOLDING REGISTER

Offset: 0x00			Register Name: UART_THR Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/

			THR Transmit Holding Register Data to be transmitted on the serial output port (sout) in UART mode or the serial infrared output (sir_out_n) in infrared mode. Data should only be written to the THR when the THR Empty (THRE) bit (LSR[5]) is set. If in FIFO mode and FIFOs are enabled (FCR[0] = 1) and THRE is set, 16 number of characters of data may be written to the THR before the FIFO is full. Any attempt to write data when the FIFO is full results in the write data being lost.
7:0	W	0	

UART DIVISOR LATCH LOW REGISTER

Offset: 0x00			Register Name: UART_DLL
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0	<p>DLL</p> <p>Divisor Latch Low</p> <p>Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero).</p> <p>The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor).</p> <p>Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLL is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.</p>

UART DIVISOR LATCH HIGH REGISTER

			Register Name: UART_DLH
Offset: 0x04			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0	<p>DLH Divisor Latch High</p> <p>Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART. This register may only be accessed when the DLAB bit (LCR[7]) is set and the UART is not busy (USR[0] is zero).</p> <p>The output baud rate is equal to the serial clock (sclk) frequency divided by sixteen times the value of the baud rate divisor, as follows: baud rate = (serial clock freq) / (16 * divisor).</p> <p>Note that with the Divisor Latch Registers (DLL and DLH) set to zero, the baud clock is disabled and no serial communications occur. Also, once the DLH is set, at least 8 clock cycles of the slowest UART clock should be allowed to pass before transmitting or receiving data.</p>

UART INTERRUPT ENABLE REGISTER

			Register Name: UART_IER
Offset: 0x04			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	<p>/ PTIME Programmable THRE Interrupt Mode Enable</p> <p>This is used to enable/disable the generation of THRE Interrupt.</p> <p>0: Disable 1: Enable</p>
7	R/W		
6:4	/	/	/

			EDSSI Enable Modem Status Interrupt This is used to enable/disable the generation of Modem Status Interrupt. This is the fourth highest priority interrupt. 0: Disable 1: Enable
3	R/W	0	ELSI Enable Receiver Line Status Interrupt This is used to enable/disable the generation of Receiver Line Status Interrupt. This is the highest priority interrupt. 0: Disable 1: Enable
2	R/W	0	ETBEI Enable Transmit Holding Register Empty Interrupt This is used to enable/disable the generation of Transmitter Holding Register Empty Interrupt. This is the third highest priority interrupt. 0: Disable 1: Enable
1	R/W	0	ERBFI Enable Received Data Available Interrupt This is used to enable/disable the generation of Received Data Available Interrupt and the Character Timeout Interrupt (if in FIFO mode and FIFOs enabled). These are the second highest priority interrupts. 0: Disable 1: Enable
0	R/W	0	

UART INTERRUPT IDENTITY REGISTER

Offset: 0x08	Register Name: UART_IIR
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			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	<p>/</p> <p>FEFLAG</p> <p>FIFOs Enable Flag</p> <p>This is used to indicate whether the FIFOs are enabled or disabled.</p> <p>00: Disable</p>
7:6	R	0	11: Enable
5:4	/	/	/
3:0	R	0x1	<p>IID</p> <p>Interrupt ID</p> <p>This indicates the highest priority pending interrupt which can be one of the following types:</p> <ul style="list-style-type: none"> 0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status 0111: busy detect 1100: character timeout <p>Bit 3 indicates an interrupt can only occur when the FIFOs are enabled and used to distinguish a Character Timeout condition interrupt.</p>

Interrupt ID	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset
0001	-	None	None	-
0110	Highest	Receiver line status	Overrun/parity/ framing errors or break interrupt	Reading the line status register
0100	Second	Received data	Receiver data available (non-FIFO mode or FIFOs)	Reading the receiver buffer register (non-FIFO mode or

		available	disabled) or RCVR FIFO trigger level reached (FIFO mode and FIFOs enabled)	FIFOs disabled) or the FIFO drops below the trigger level (FIFO mode and FIFOs enabled)
1100	Second	Character timeout indication	No characters in or out of the RCVR FIFO during the last 4 character times and there is at least 1character in it during This time	Reading the receiver buffer register
0010	Third	Transmitter holding register empty	Transmitter holding register empty (Program THRE Mode disabled) or XMIT FIFO at or below threshold (Program THRE Mode enabled)	Reading the IIR register (if source of interrupt); or, writing into THR (FIFOs or THRE Mode not selected or disabled) or XMIT FIFO above threshold (FIFOs and THRE Mode selected and enabled).
0000	Fourth	Modem status	Clear to send or data set ready or ring indicator or data carrier detect. Note that if auto flow control mode is enabled, a change in CTS (that is, DCTS set) does not cause an interrupt.	Reading the Modem status Register
0111	Fifth	Busy detect indication	UART_16550_COMPATIBLE = NO and master has tried to write to the Line Control Register while the UART is busy (USR[0] is set to one).	Reading the UART status register

UART FIFO CONTROL REGISTER

Offset: 0x08			Register Name: UART_FCR
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/

			RT RCVR Trigger This is used to select the trigger level in the receiver FIFO at which the Received Data Available Interrupt is generated. In auto flow control mode it is used to determine when the rts_n signal is de-asserted. It also determines when the dma_rx_req_n signal is asserted in certain modes of operation. 00: 1 character in the FIFO 01: FIFO ¼ full 10: FIFO ½ full 11: FIFO-2 less than full
7:6	W	0	TFT TX Empty Trigger Writes have no effect when THRE_MODE_USER = Disabled. This is used to select the empty threshold level at which the THRE Interrupts are generated when the mode is active. It also determines when the dma_tx_req_n signal is asserted when in certain modes of operation. 00: FIFO empty 01: 2 characters in the FIFO 10: FIFO ¼ full 11: FIFO ½ full
5:4	W	0	DMAM DMA Mode 0: Mode 0 1: Mode 1
3	W	0	XFIFOR XMIT FIFO Reset This resets the control portion of the transmit FIFO and treats the FIFO as empty. This also de-asserts the DMA TX request.
2	W	0	It is 'self-clearing'. It is not necessary to clear this bit.
1	W	0	RFIFOR

			<p>RCVR FIFO Reset</p> <p>This resets the control portion of the receive FIFO and treats the FIFO as empty. This also de-asserts the DMA RX request.</p> <p>It is 'self-clearing'. It is not necessary to clear this bit.</p>
0	W	0	<p>FIFOE</p> <p>Enable FIFOs</p> <p>This enables/disables the transmit (XMIT) and receive (RCVR) FIFOs. Whenever the value of this bit is changed both the XMIT and RCVR controller portion of FIFOs is reset.</p>

UART LINE CONTROL REGISTER

Offset: 0x0C			Register Name: UART_LCR
Default Value: 0x0000_0000			
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0	<p>DLAB</p> <p>Divisor Latch Access Bit</p> <p>It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable reading and writing of the Divisor Latch register (DLL and DLH) to set the baud rate of the UART. This bit must be cleared after initial baud rate setup in order to access other registers.</p> <p>0: Select RX Buffer Register (RBR) / TX Holding Register(THR) and Interrupt Enable Register (IER)</p> <p>1: Select Divisor Latch LS Register (DLL) and Divisor Latch MS Register (DLM)</p>
6	R/W	0	<p>BC</p> <p>Break Control Bit</p> <p>This is used to cause a break condition to be transmitted to the receiving device. If set to one the serial output is forced to the spacing (logic 0) state. When not in Loopback Mode, as determined by MCR[4], the sout line is forced low until the Break bit is cleared. If SIR_MODE = Enabled and active (MCR[6] set to one) the sir_out_n line is continuously pulsed. When in</p>

			Loopback Mode, the break condition is internally looped back to the receiver and the sir_out_n line is forced low.
5:4	R/W	0	<p>EPS</p> <p>Even Parity Select</p> <p>It is writeable only when UART is not busy (USR[0] is zero) and always writable readable. This is used to select between even and odd parity, when parity is enabled (PEN set to one). Setting the LCR[5] is used to reverse the LCR[4].</p> <p>00: Odd Parity</p> <p>01: Even Parity</p> <p>1X: Reverse LCR[4]</p>
3	R/W	0	<p>PEN</p> <p>Parity Enable</p> <p>It is writeable only when UART is not busy (USR[0] is zero) and always readable. This bit is used to enable and disable parity generation and detection in transmitted and received serial character respectively.</p> <p>0: parity disabled</p> <p>1: parity enabled</p>
2	R/W	0	<p>STOP</p> <p>Number of stop bits</p> <p>It is writeable only when UART is not busy (USR[0] is zero) and always readable. This is used to select the number of stop bits per character that the peripheral transmits and receives. If set to zero, one stop bit is transmitted in the serial data. If set to one and the data bits are set to 5 (LCR[1:0] set to zero) one and a half stop bits are transmitted. Otherwise, two stop bits are transmitted. Note that regardless of the number of stop bits selected, the receiver checks only the first stop bit.</p> <p>0: 1 stop bit</p> <p>1: 1.5 stop bits when DLS (LCR[1:0]) is zero, else 2 stop bit</p>
1:0	R/W	0	<p>DLS</p> <p>Data Length Select</p> <p>It is writeable only when UART is not busy (USR[0] is zero) and</p>

		always readable. This is used to select the number of data bits per character that the peripheral transmits and receives. The number of bit that may be selected areas follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
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UART MODEM CONTROL REGISTER

Offset: 0x10			Register Name: UART_MCR Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:7	/	/	/
6	R/W	0	SIRE SIR Mode Enable 0: IrDA SIR Mode disabled 1: IrDA SIR Mode enabled
5	R/W	0	AFCE Auto Flow Control Enable When FIFOs are enabled and the Auto Flow Control Enable (AFCE) bit is set, Auto Flow Control features are enabled. 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled
4	R/W	0	LOOP Loop Back Mode 0: Normal Mode 1: Loop Back Mode This is used to put the UART into a diagnostic mode for test purposes. If operating in UART mode (SIR_MODE != Enabled or not active, MCR[6] set to zero), data on the sout line is held high, while serial data output is looped back to the sin line, internally. In this mode all the interrupts are fully functional.

			Also, in loopback mode, the modem control inputs (dsr_n, cts_n, ri_n, dcd_n) are disconnected and the modem control outputs (dtr_n, rts_n, out1_n, out2_n) are looped back to the inputs, internally. If operating in infrared mode (SIR_MODE == Enabled AND active, MCR[6] set to one), data on the sir_out_n line is held low, while serial data output is inverted and looped back to the sir_in line.
3	/	/	/
2	/	/	/
1	R/W	0	<p>RTS</p> <p>Request to Send</p> <p>This is used to directly control the Request to Send (rts_n) output. The Request To Send (rts_n) output is used to inform the modem or data set that the UART is ready to exchange data. When Auto RTS Flow Control is not enabled (MCR[5] set to zero), the rts_n signal is set low by programming MCR[1] (RTS) to a high. In Auto Flow Control, AFCE_MODE == Enabled and active (MCR[5] set to one) and FIFOs enable (FCR[0] set to one), the rts_n output is controlled in the same way, but is also gated with the receiver FIFO threshold trigger (rts_n is inactive high when above the threshold). The rts_n signal is de-asserted when MCR[1] is set low.</p> <p>0: rts_n de-asserted (logic 1)</p> <p>1: rts_n asserted (logic 0)</p> <p>Note that in Loopback mode (MCR[4] set to one), the rts_n output is held inactive high while the value of this location is internally looped back to an input.</p>
0	R/W	0	<p>DTR</p> <p>Data Terminal Ready</p> <p>This is used to directly control the Data Terminal Ready (dtr_n) output. The value written to this location is inverted and driven out on dtr_n.</p> <p>0: dtr_n de-asserted (logic 1)</p>

		<p>1: dtr_n asserted (logic 0)</p> <p>The Data Terminal Ready output is used to inform the modem or data set that the UART is ready to establish communications.</p> <p>Note that in Loopback mode (MCR[4] set to one), the dtr_n output is held inactive high while the value of this location is internally looped back to an input.</p>
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UART LINE STATUS REGISTER

Offset: 0x14			Register Name: UART_LSR
Default Value: 0x0000_0060			
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R	0	<p>FIFOERR</p> <p>RX Data Error in FIFO</p> <p>When FIFOs are disabled, this bit is always 0. When FIFOs are enabled, this bit is set to 1 when there is at least one PE, FE, or BI in the RX FIFO. It is cleared by a read from the LSR register provided there are no subsequent errors in the FIFO.</p>
6	R	1	<p>TEMT</p> <p>Transmitter Empty</p> <p>If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register and the TX Shift Register are empty. If the FIFOs are enabled, this bit is set whenever the TX FIFO and the TX Shift Register are empty. In both cases, this bit is cleared when a byte is written to the TX data channel.</p>
5	R	1	<p>THRE</p> <p>TX Holding Register Empty</p> <p>If the FIFOs are disabled, this bit is set to "1" whenever the TX Holding Register is empty and ready to accept new data and it is cleared when the CPU writes to the TX Holding Register.</p> <p>If the FIFOs are enabled, this bit is set to "1" whenever the TX FIFO is empty and it is cleared when at least one byte is written</p>

			to the TX FIFO.
4	R	0	<p>BI</p> <p>Break Interrupt</p> <p>This is used to indicate the detection of a break sequence on the serial input data.</p> <p>If in UART mode (SIR_MODE == Disabled), it is set whenever the serial input, sin, is held in a logic '0' state for longer than the sum of <i>start time + data bits + parity + stop bits</i>.</p> <p>If in infrared mode (SIR_MODE == Enabled), it is set whenever the serial input, sir_in, is continuously pulsed to logic '0' for longer than the sum of <i>start time + data bits + parity + stop bits</i>. A break condition on serial input causes one and only one character, consisting of all zeros, to be received by the UART.</p> <p>In the FIFO mode, the character associated with the break condition is carried through the FIFO and is revealed when the character is at the top of the FIFO. Reading the LSR clears the BI bit. In the non-FIFO mode, the BI indication occurs immediately and persists until the LSR is read.</p>
3	R	0	<p>FE</p> <p>Framing Error</p> <p>This is used to indicate the occurrence of a framing error in the receiver. A framing error occurs when the receiver does not detect a valid STOP bit in the received data.</p> <p>In the FIFO mode, since the framing error is associated with a character received, it is revealed when the character with the framing error is at the top of the FIFO. When a framing error occurs, the UART tries to resynchronize. It does this by assuming that the error was due to the start bit of the next character and then continues receiving the other bit i.e. data, and/or parity and stop. It should be noted that the Framing Error (FE) bit (LSR[3]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]).</p> <p>0: no framing error</p> <p>1:framing error</p> <p>Reading the LSR clears the FE bit.</p>

2	R	0	<p>PE Parity Error</p> <p>This is used to indicate the occurrence of a parity error in the receiver if the Parity Enable (PEN) bit (LCR[3]) is set. In the FIFO mode, since the parity error is associated with a character received, it is revealed when the character with the parity error arrives at the top of the FIFO. It should be noted that the Parity Error (PE) bit (LSR[2]) is set if a break interrupt has occurred, as indicated by Break Interrupt (BI) bit (LSR[4]).</p> <p>0: no parity error 1: parity error</p> <p>Reading the LSR clears the PE bit.</p>
1	R	0	<p>OE Overrun Error</p> <p>This occurs if a new data character was received before the previous data was read. In the non-FIFO mode, the OE bit is set when a new character arrives in the receiver before the previous character was read from the RBR. When this happens, the data in the RBR is overwritten. In the FIFO mode, an overrun error occurs when the FIFO is full and a new character arrives at the receiver. The data in the FIFO is retained and the data in the receive shift register is lost.</p> <p>0: no overrun error 1: overrun error</p> <p>Reading the LSR clears the OE bit.</p>
0	R	0	<p>DR Data Ready</p> <p>This is used to indicate that the receiver contains at least one character in the RBR or the receiver FIFO.</p> <p>0: no data ready 1: data ready</p> <p>This bit is cleared when the RBR is read in non-FIFO mode, or when the receiver FIFO is empty, in FIFO mode.</p>

UART MODEM STATUS REGISTER

Offset: 0x18			Register Name: UART_MSR Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R	0	<p>DCD Line State of Data Carrier Detect This is used to indicate the current state of the modem control line dcd_n. This bit is the complement of dcd_n. When the Data Carrier Detect input (dcd_n) is asserted it is an indication that the carrier has been detected by the modem or data set. 0: dcd_n input is de-asserted (logic 1) 1: dcd_n input is asserted (logic 0)</p>
6	R	0	<p>RI Line State of Ring Indicator This is used to indicate the current state of the modem control line ri_n. This bit is the complement of ri_n. When the Ring Indicator input (ri_n) is asserted it is an indication that a telephone ringing signal has been received by the modem or data set. 0: ri_n input is de-asserted (logic 1) 1: ri_n input is asserted (logic 0)</p>
5	R	0	<p>DSR Line State of Data Set Ready This is used to indicate the current state of the modem control line dsr_n. This bit is the complement of dsr_n. When the Data Set Ready input (dsr_n) is asserted it is an indication that the modem or data set is ready to establish communications with UART. 0: dsr_n input is de-asserted (logic 1) 1: dsr_n input is asserted (logic 0) In Loopback Mode (MCR[4] set to one), DSR is the same as</p>

			MCR[0] (DTR).
4	R	0	<p>CTS Line State of Clear To Send</p> <p>This is used to indicate the current state of the modem control line <code>cts_n</code>. This bit is the complement of <code>cts_n</code>. When the Clear to Send input (<code>cts_n</code>) is asserted it is an indication that the modem or data set is ready to exchange data with UART.</p> <p>0: <code>cts_n</code> input is de-asserted (logic 1) 1: <code>cts_n</code> input is asserted (logic 0)</p> <p>In Loopback Mode (MCR[4] = 1), CTS is the same as MCR[1] (RTS).</p>
3	R	0	<p>DDCD Delta Data Carrier Detect</p> <p>This is used to indicate that the modem control line <code>dcd_n</code> has changed since the last time the MSR was read.</p> <p>0: no change on <code>dcd_n</code> since last read of MSR 1: change on <code>dcd_n</code> since last read of MSR</p> <p>Reading the MSR clears the DDCD bit.</p> <p>Note: If the DDCD bit is not set and the <code>dcd_n</code> signal is asserted (low) and a reset occurs (software or otherwise), then the DDCD bit is set when the reset is removed if the <code>dcd_n</code> signal remains asserted.</p>
2	R	0	<p>TERI Trailing Edge Ring Indicator</p> <p>This is used to indicate that a change on the input <code>ri_n</code> (from an active-low to an inactive-high state) has occurred since the last time the MSR was read.</p> <p>0: no change on <code>ri_n</code> since last read of MSR 1: change on <code>ri_n</code> since last read of MSR</p> <p>Reading the MSR clears the TERI bit.</p>
1	R	0	DDSR

			<p>Delta Data Set Ready</p> <p>This is used to indicate that the modem control line <code>dsr_n</code> has changed since the last time the MSR was read.</p> <p>0: no change on <code>dsr_n</code> since last read of MSR</p> <p>1: change on <code>dsr_n</code> since last read of MSR</p> <p>Reading the MSR clears the DDSR bit. In Loopback Mode (<code>MCR[4] = 1</code>), DDSR reflects changes on <code>MCR[0]</code> (DTR).</p> <p>Note: If the DDSR bit is not set and the <code>dsr_n</code> signal is asserted (low) and a reset occurs (software or otherwise), then the DDSR bit is set when the reset is removed if the <code>dsr_n</code> signal remains asserted.</p>
0	R	0	<p>DCTS</p> <p>Delta Clear to Send</p> <p>This is used to indicate that the modem control line <code>cts_n</code> has changed since the last time the MSR was read.</p> <p>0: no change on <code>ctsd sr_n</code> since last read of MSR</p> <p>1: change on <code>ctsd sr_n</code> since last read of MSR</p> <p>Reading the MSR clears the DCTS bit. In Loopback Mode (<code>MCR[4] = 1</code>), DCTS reflects changes on <code>MCR[1]</code> (RTS).</p> <p>Note: If the DCTS bit is not set and the <code>cts_n</code> signal is asserted (low) and a reset occurs (software or otherwise), then the DCTS bit is set when the reset is removed if the <code>cts_n</code> signal remains asserted.</p>

UART SCRATCH REGISTER

			Register Name: <code>UART_SCH</code>
Offset: <code>0x1C</code>			Default Value: <code>0x0000_0000</code>
Bit	Read/Write	Default	Description
31:8	/	/	/
7:0	R/W	0	<p>SCRATCH_REG</p> <p>Scratch Register</p> <p>This register is for programmers to use as a temporary storage space. It has no defined purpose in the UART.</p>

UART STATUS REGISTER

Offset: 0x7C			Register Name: UART_USR Default Value: 0x0000_0006
Bit	Read/Write	Default	Description
31:5	/	/	/
4	R	0	<p>RFF Receive FIFO Full This is used to indicate that the receive FIFO is completely full. 0: Receive FIFO not full 1: Receive FIFO Full This bit is cleared when the RX FIFO is no longer full.</p>
3	R	0	<p>RFNE Receive FIFO Not Empty This is used to indicate that the receive FIFO contains one or more entries. 0: Receive FIFO is empty 1: Receive FIFO is not empty This bit is cleared when the RX FIFO is empty.</p>
2	R	1	<p>TFE Transmit FIFO Empty This is used to indicate that the transmit FIFO is completely empty. 0: Transmit FIFO is not empty 1: Transmit FIFO is empty This bit is cleared when the TX FIFO is no longer empty.</p>
1	R	1	<p>TFNF Transmit FIFO Not Full This is used to indicate that the transmit FIFO is not full. 0: Transmit FIFO is full</p>

			1: Transmit FIFO is not full This bit is cleared when the TX FIFO is full.
0	R	0	BUSY UART Busy Bit 0: Idle or inactive 1: Busy

UART TRANSMIT FIFO LEVEL REGISTER

Offset: 0x80			Register Name: UART_TFL Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:7	/	/	/
6:0			TFL Transmit FIFO Level This is indicates the number of data entries in the transmit FIFO.
6:0	R	0	

UART RECEIVE FIFO LEVEL REGISTER

Offset: 0x84			Register Name: UART_RFL Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:7	/	/	/
6:0			RFL Receive FIFO Level This is indicates the number of data entries in the receive FIFO.
6:0	R	0	

UART HALT TX REGISTER

Offset: 0xA4			Register Name: UART_HALTI Default Value: 0x0000_0000
--------------	--	--	---

Bit	Read/Write	Default	Description
31:6	/	/	/
5	R/W	0	<p>SIR_RX_INVERT</p> <p>SIR Receiver Pulse Polarity Invert</p> <p>0: Not invert receiver signal</p> <p>1: Invert receiver signal</p>
4	R/W	0	<p>SIR_TX_INVERT</p> <p>SIR Transmit Pulse Polarity Invert</p> <p>0: Not invert transmit pulse</p> <p>1: Invert transmit pulse</p>
3	/	/	/
2	R/W	0	<p>CHANGE_UPDATE</p> <p>After the user using HALT[1] to change the baudrate or LCR configuration, write 1 to update the configuration and waiting this bit self clear to 0 to finish update process. Write 0 to this bit has no effect.</p> <p>1: Update trigger, Self clear to 0 when finish update.</p>
1	R/W	0	<p>CHCFG_AT_BUSY</p> <p>This is an enable bit for the user to change LCR register configuration (except for the DLAB bit) and baudrate register (DLH and DLL) when the UART is busy (USB[0] is 1).</p> <p>1: Enable change when busy</p>
0	R/W	0	<p>HALT_TX</p> <p>Halt TX</p> <p>This register is use to halt transmissions for testing, so that the transmit FIFO can be filled by the master when FIFOs are implemented and enabled.</p> <p>0 : Halt TX disabled</p> <p>1 : Halt TX enabled</p> <p>Note: If FIFOs are not enabled, the setting of the halt TX register has no effect on operation.</p>

7.4.5 UART Special Requirement

UART PIN LIST

Port Name	Width	Direction	Description
UART0_TX	1	OUT	UART Serial Bit output
UART0_RX	1	IN	UART Serial Bit input
UART1_TX	1	OUT	UART Serial Bit output
UART1_RX	1	IN	UART Serial Bit input
UART1_RTS		OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART1_CTS		IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data
UART2_TX	1	OUT	UART Serial Bit output
UART2_RX	1	IN	UART Serial Bit input
UART2_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART2_CTS	1	IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data
UART3_TX	1	OUT	UART Serial Bit output
UART3_RX	1	IN	UART Serial Bit input
UART3_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART3_CTS	1	IN	UART Clear To End

			This active low signal is an input showing when Modem is ready to accept data
UART4_TX	1	OUT	UART Serial Bit output
UART4_RX	1	IN	UART Serial Bit input
UART4_RTS	1	OUT	UART Request To Send This active low output signal informs Modem that the UART is ready to send data
UART4_CTS	1	IN	UART Clear To End This active low signal is an input showing when Modem is ready to accept data
S_UART_TX	1	OUT	UART Serial Bit output
S_UART_RX	1	IN	UART Serial Bit input

IRDA INVERTED SIGNALS

When the UART is working in IrDA mode ($MCR[6] = '1'$), if $HALT[4]$ is set to '1', the signal is inverted before transferring to pin SOUT and if $HALT[5]$ is set to '1', the signal is inverted after receiving from pin SIN

7.5 USB OTG

7.5.1 Overview

The USB OTG is a Dual-Role Device (DRD) controller, which supports both device and host functions which can also be configured as a Host-only or Device-only controller, fully compliant with the USB 2.0 Specification. It can support high-speed (HS, 480-Mbps), full-speed (FS, 12-Mbps), and low-speed (LS, 1.5-Mbps) transfers in Host mode. It can support high-speed (HS, 480-Mbps), and full-speed (FS, 12-Mbps) in Device mode. Standard USB transceiver can be used through its UTMI+PHY Level3 interface. The UTMI+PHY interface is bidirectional with 8-bit data bus.

The USB2.0 OTG controller (SIE) includes the following features:

- Comply with USB 2.0 Specification
- Supports High-Speed (HS, 480Mbps), Full-Speed (FS, 12Mbps), and Low-Speed (LS, 1.5Mbps) in Host mode and support High-Speed (HS, 480Mbps), Full-Speed (FS, 12Mbps) in Device mode
- Supports the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used.
- 64-Byte Endpoint 0 for Control Transfer (Endpoint0)
- Supports up to 10 User-Configurable Endpoints for Bulk , Isochronous, Interrupt bi-directional transfers (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)
- Supports up to 8128Bytes (8KB-64B) FIFO for EPs (Excluding EPO)
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Includes automatic ping capabilities
- Soft connect/disconnect function
- Performs all transaction scheduling in hardware
- Power Optimization and Power Management capabilities

7.5.2 USB_OTG Timing Diagram

Please refer USB2.0 Specification.

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7.5.3 USB/OTG Clock Source and Frequency

There are two clocks for USB/OTG SIE module. One is from AHB bus and one is from UTMI Transceiver which is called USB/OTG PHY.

Name	Description
USB_CLK	System clock (provided by AHB bus clock). This clock needs to be >30MHz where the core is configured for an 8-bit transceiver interface and up to 180Mhz
USB_XCLK	Transceiver macrocell clock. 60MHz for an 8-bit interface

7.6 USB Host

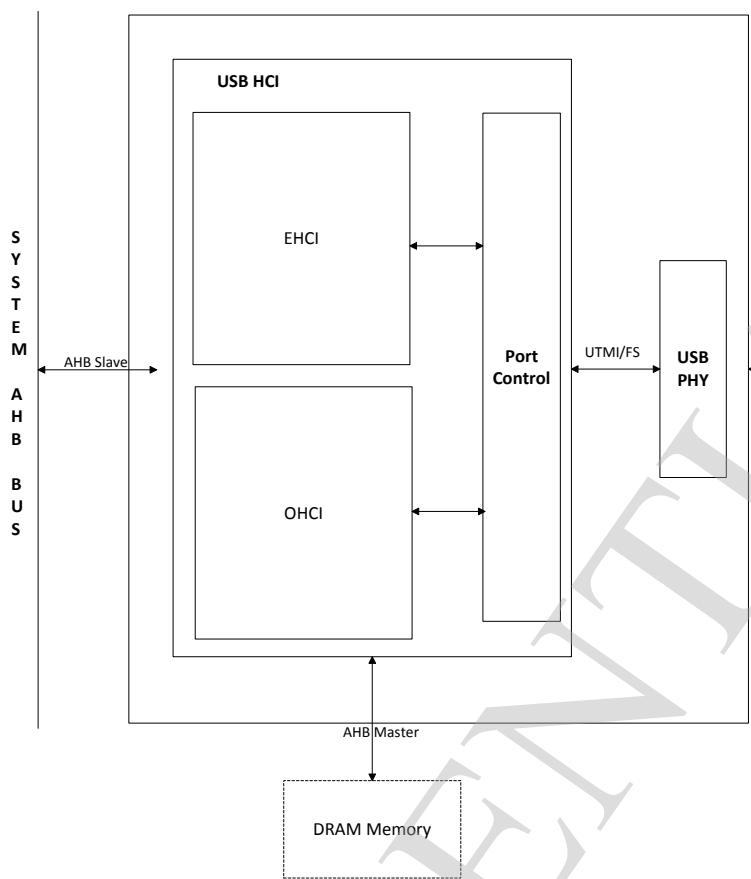
7.6.1 Overview

USB Host Controller is fully compliant with the USB 2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Revision 1.0, and the Open Host Controller Interface (OHCI) Specification Release 1.0a. The controller supports high-speed, 480Mbps transfers (40 times faster than USB 1.1 full-speed mode) using an EHCI Host Controller, as well as full and low speeds through one integrated OHCI Host Controllers.

The USB host controller includes the following features:

- Support industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports bus.
- Support 32-bit Little Endian AMBA AHB Slave Bus for Register Access.
- Support 32-bit Little Endian AMBA AHB Master Bus for Memory Access.
- Comply with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Support High-Speed (HS, 480Mbps), Full-Speed (FS, 12Mbps), and Low-Speed (LS, 1.5Mbps) Device.
- Support the UTMI+ Level 3 interface. The 8-bit bidirectional data buses are used.
- Support only 1 USB Root Port shared between EHCI and OHCI.

The USB host controller system-level block diagram is showed below:



7.6.2 USB Host Timing Diagram

Please refer to USB2.0 specification, Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.

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7.6.3 USB Host Register List

Module Name	Base Address
USB_HCI0	0x01C1A000
USB_HCI1	0x01C1B000
USB_OHCI2	0x01C1C000

Register Name	Offset	Description
EHCI Capability Register		
E_CAPLENGTH	0x000	EHCI Capability register Length Register
E_HCIVERSION	0x002	EHCI Host Interface Version Number Register
E_HCSPARAMS	0x004	EHCI Host Control Structural Parameter Register
E_HCCPARAMS	0x008	EHCI Host Control Capability Parameter Register
E_HCSPPORTROUTE	0x00c	EHCI Companion Port Route Description
EHCI Operational Register		
E_USBCMD	0x010	EHCI USB Command Register
E_USBSTS	0x014	EHCI USB Status Register
E_USBINTR	0x018	EHCI USB Interrupt Enable Register
E_FRINDEX	0x01c	EHCI USB Frame Index Register
E_CTRLDSSEGMENT	0x020	EHCI 4G Segment Selector Register
E_PERIODICLISTBASE	0x024	EHCI Frame List Base Address Register
E_ASYNCNLISTADDR	0x028	EHCI Next Asynchronous List Address Register
E_CONFIGFLAG	0x050	EHCI Configured Flag Register
E_PORTSC	0x054	EHCI Port Status/Control Register
OHCI Control and Status Partition Register		
O_HcRevision	0x400	OHCI Revision Register
O_HcControl	0x404	OHCI Control Register
O_HcCommandStatus	0x408	OHCI Command Status Register

O_HcInterruptStatus	0x40c	OHCI Interrupt Status Register
O_HcInterruptEnable	0x410	OHCI Interrupt Enable Register
O_HcInterruptDisable	0x414	OHCI Interrupt Disable Register
OHCI Memory Pointer Partition Register		
O_HcHCCA	0x418	OHCI HCCA Base
O_HcPeriodCurrentED	0x41c	OHCI Period Current ED Base
O_HcControlHeadED	0x420	OHCI Control Head ED Base
O_HcControlCurrentED	0x424	OHCI Control Current ED Base
O_HcBulkHeadED	0x428	OHCI Bulk Head ED Base
O_HcBulkCurrentED	0x42c	OHCI Bulk Current ED Base
O_HcDoneHead	0x430	OHCI Done Head Base
OHCI Frame Counter Partition Register		
O_HcFmInterval	0x434	OHCI Frame Interval Register
O_HcFmRemaining	0x438	OHCI Frame Remaining Register
O_HcFmNumber	0x43c	OHCI Frame Number Register
O_HcPeriodicStart	0x440	OHCI Periodic Start Register
O_HcLSThreshold	0x444	OHCI LS Threshold Register
OHCI Root Hub Partition Register		
O_HcRhDescriptorA	0x448	OHCI Root Hub Descriptor Register A
O_HcRhDescriptorB	0x44c	OHCI Root Hub Descriptor Register B
O_HcRhStatus	0x450	OHCI Root Hub Status Register
O_HcRhPortStatus	0x454	OHCI Root Hub Port Status Register

7.6.4 EHCI Register Description

EHCI IDENTIFICATION REGISTER

Offset:0x00			Register Name: CAPLENGTH Default Value: Implementation Dependent
Bit	Read/Write	Default	Description
7:0	R	0x10	CAPLENGTH The value in these bits indicates an offset to add to register base to find the beginning of the Operational Register Space.

EHCI HOST INTERFACE VERSION NUMBER REGISTER

Offset: 0x02			Register Name: HCIVERSION Default Value: 0x0100
Bit	Read/Write	Default	Description
15:0	R	0x0100	HCIVERSION This is a 16-bits register containing a BCD encoding of the EHCI revision number supported by this host controller. The most significant byte of this register represents a major revision and the least significant byte is the minor revision.

EHCI HOST CONTROL STRUCTURAL PARAMETER REGISTER

Offset: 0x04			Register Name: HCSPARAMS Default Value: Implementation Dependent
Bit	Read/Write	Default	Description
31:24	/	0	Reserved. These bits are reserved and should be set to zero.
23:20	R	0	/
19:16	/	0	Reserved.

			These bits are reserved and should be set to zero.						
15:12	R	0	<p>Number of Companion Controller (N_CC)</p> <p>This field indicates the number of companion controllers associated with this USB2.0 host controller. A zero in this field indicates there are no companion host controllers. And a value larger than zero in this field indicates there are companion USB1.1 host controller(s).</p> <p>This field will always be '0'.</p>						
11:8	R	0	<p>Number of Port per Companion Controller(N_PCC)</p> <p>This field indicates the number of ports supported per companion host controller host controller. It is used to indicate the port routing configuration to system software.</p> <p>This field will always fix with '0'.</p>						
7	R	0	<p>Port Routing Rules</p> <p>This field indicates the method used by this implementation for how all ports are mapped to companion controllers. The value of this field has the following interpretation:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Meaning</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.</td> </tr> <tr> <td>1</td> <td>The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.</td> </tr> </tbody> </table> <p>This field will always be '0'.</p>	Value	Meaning	0	The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.	1	The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.
Value	Meaning								
0	The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on.								
1	The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTTOUTE array.								
6:4	/	0	<p>Reserved.</p> <p>These bits are reserved and should be set to zero.</p>						
3:0	R	1	<p>N_PORTS</p> <p>This field specifies the number of physical downstream ports implemented on this host controller. The value of this field determines how many port registers are addressable in the Operational Register Space. Valid values are in the range of 0x1 to 0x0f.</p> <p>This field is always 1.</p>						

EHCI HOST CONTROL CAPABILITY PARAMETER REGISTER

Offset: 0x08			Register Name: HCCPARAMS Default Value: Implementation Dependent
Bit	Read/Write	Default	Description
31:16	/	0	Reserved These bits are reserved and should be set to zero.
15:18	R	0	EHCI Extended Capabilities Pointer (EECP) This optional field indicates the existence of a capabilities list. A value of 00b indicates no extended capabilities are implemented. A non-zero value in this register indicates the offset in PCI configuration space of the first EHCI extended capability. The pointer value must be 40h or greater if implemented to maintain consistency of the PCI header defined for this class of device. The value of this field is always '00b'.
7:4	R		Isochronous Scheduling Threshold This field indicates, relative to the current position of the executing host controller, where software can reliably update the isochronous schedule. When bit[7] is zero, the value of the least significant 3 bits indicates the number of micro-frames a host controller can hold a set of isochronous data structures(one or more) before flushing the state. When bit[7] is a one, then host software assumes the host controller may cache an isochronous data structure for an entire frame.
3	R	0	Reserved These bits are reserved and should be set to zero.
2	R		Asynchronous Schedule Park Capability If this bit is set to a one, then the host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. The feature can be disabled or enabled and set to a specific level by using the Asynchronous Schedule Park Mode Enable and Asynchronous Schedule Park Mode Count fields in the USBCMD register.

			Programmable Frame List Flag If this bit is set to a zero, then system software must use a frame list length of 1024 elements with this host controller. The USBCMD register Frame List Size field is a read-only register and should be set to zero. If set to 1, then system software can specify and use the frame list in the USBCMD register Frame List Size field to configure the host controller. The frame list must always aligned on a 4K page boundary. This requirement ensures that the frame list is always physically contiguous.
1	R	0	Reserved These bits are reserved for future use and should return a value of zero when read.

EHCI COMPANION PORT ROUTE DESCRIPTION

Offset: 0x0C			Register Name: HCSP-PORTROUTE Default Value: UNDEFINED
Bit	Read/Write	Default	Description
31:0	R		HCSP-PORTROUTE This optional field is valid only if Port Routing Rules field in HCSPARAMS register is set to a one. This field is used to allow a host controller implementation to explicitly describe to which companion host controller each implemented port is mapped. This field is a 15-element nibble array (each 4 bit is one array element). Each array location corresponds one-to-one with a physical port provided by the host controller (e.g. PORTROUTE [0] corresponds to the first PORTSC port, PORTROUTE [1] to the second PORTSC port, etc.). The value of each element indicates to which of the companion host controllers this port is routed. Only the first N_PORTS elements have valid information. A value of zero indicates that the port is routed to the lowest numbered

			function companion host controller. A value of one indicates that the port is routed to the next lowest numbered function companion host controller, and so on.
--	--	--	---

EHCI USB COMMAND REGISTER

Offset: 0x10			Register Name: USBCMD Default Value: 0x00080000(0x00080B00 if Asynchronous Schedule Park Capability is a one)																		
Bit	Read/Write	Default	Description																		
31:24	/	0	Reserved These bits are reserved and should be set to zero.																		
23:16	R/W	0x08	<p>Interrupt Threshold Control</p> <p>The value in this field is used by system software to select the maximum rate at which the host controller will issue interrupts. The only valid values are defined below:</p> <table border="1"> <thead> <tr> <th>Value</th> <th>Minimum Interrupt Interval</th> </tr> </thead> <tbody> <tr> <td>0x00</td> <td>Reserved</td> </tr> <tr> <td>0x01</td> <td>1 micro-frame</td> </tr> <tr> <td>0x02</td> <td>2 micro-frame</td> </tr> <tr> <td>0x04</td> <td>4 micro-frame</td> </tr> <tr> <td>0x08</td> <td>8 micro-frame(default, equates to 1 ms)</td> </tr> <tr> <td>0x10</td> <td>16 micro-frame(2ms)</td> </tr> <tr> <td>0x20</td> <td>32 micro-frame(4ms)</td> </tr> <tr> <td>0x40</td> <td>64 micro-frame(8ms)</td> </tr> </tbody> </table> <p>Any other value in this register yields undefined results.</p> <p>The default value in this field is 0x08 .</p> <p>Software modifications to this bit while HC Halted bit is equal to zero results in undefined behavior.</p>	Value	Minimum Interrupt Interval	0x00	Reserved	0x01	1 micro-frame	0x02	2 micro-frame	0x04	4 micro-frame	0x08	8 micro-frame(default, equates to 1 ms)	0x10	16 micro-frame(2ms)	0x20	32 micro-frame(4ms)	0x40	64 micro-frame(8ms)
Value	Minimum Interrupt Interval																				
0x00	Reserved																				
0x01	1 micro-frame																				
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0x04	4 micro-frame																				
0x08	8 micro-frame(default, equates to 1 ms)																				
0x10	16 micro-frame(2ms)																				
0x20	32 micro-frame(4ms)																				
0x40	64 micro-frame(8ms)																				
15:12	/	0	Reserved These bits are reserved and should be set to zero.																		

11	R/W or R	0	<p>Asynchronous Schedule Park Mode Enable(OPTIONAL)</p> <p>If the Asynchronous Park Capability bit in the HCCPARAMS register is a one, then this bit defaults to a 1 and is R/W. Otherwise the bit must be a zero and is Read Only. Software uses this bit to enable or disable Park mode. When this bit is one, Park mode is enabled. When this bit is zero, Park mode is disabled.</p>
10	/	0	<p>Reserved</p> <p>These bits are reserved and should be set to zero.</p>
9:8	R/W or R	0	<p>Asynchronous Schedule Park Mode Count(OPTIONAL)</p> <p>Asynchronous Park Capability bit in the HCCPARAMS register is a one,</p> <p>Then this field defaults to 0x3 and is W/R. Otherwise it defaults to zero and is R. It contains a count of the number of successive transactions the host controller is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule.</p> <p>Valid value are 0x1 to 0x3. Software must not write a zero to this bit when Park Mode Enable is a one as it will result in undefined behavior.</p>
7	R/W	0	<p>Light Host Controller Reset(OPTIONAL)</p> <p>This control bit is not required.</p> <p>If implemented, it allows the driver to reset the EHCI controller without affecting the state of the ports or relationship to the companion host controllers. For example, the PORSTC registers should not be reset to their default values and the CF bit setting should not go to zero (retaining port ownership relationships).</p> <p>A host software read of this bit as zero indicates the Light Host Controller Reset has completed and it is safe for software to re-initialize the host controller. A host software read of this bit as a one indicates the Light Host</p>
6	R/W	0	<p>Interrupt on Async Advance Doorbell</p> <p>This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Soft-</p>

			<p>Ware must write a 1 to this bit to ring the doorbell.</p> <p>When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS. if the Interrupt on Async Advance Enable bit in the USBINTR register is a one then the host controller will assert an interrupt at the next interrupt threshold.</p> <p>The host controller sets this bit to a zero after it has set the Interrupt on Async Advance status bit in the USBSTS register to a one.</p> <p>Software should not write a one to this bit when the asynchronous schedule is disabled. Doing so will yield undefined results.</p>						
5	R/W	0	<p>Asynchronous Schedule Enable</p> <p>This bit controls whether the host controller skips processing the Asynchronous Schedule. Values mean:</p> <table border="1"> <thead> <tr> <th>Bit Value</th><th>Meaning</th></tr> </thead> <tbody> <tr> <td>0</td><td>Do not process the Asynchronous Schedule.</td></tr> <tr> <td>1</td><td>Use the ASYNLISTADDR register to access the Asynchronous Schedule.</td></tr> </tbody> </table> <p>The default value of this field is '0b'.</p>	Bit Value	Meaning	0	Do not process the Asynchronous Schedule.	1	Use the ASYNLISTADDR register to access the Asynchronous Schedule.
Bit Value	Meaning								
0	Do not process the Asynchronous Schedule.								
1	Use the ASYNLISTADDR register to access the Asynchronous Schedule.								
4	R/W	0	<p>Periodic Schedule Enable</p> <p>This bit controls whether the host controller skips processing the Periodic Schedule. Values mean:</p> <table border="1"> <thead> <tr> <th>Bit Value</th><th>Meaning</th></tr> </thead> <tbody> <tr> <td>0</td><td>Do not process the Periodic Schedule.</td></tr> <tr> <td>1</td><td>Use the PERIODICLISTBASE register to access the Periodic Schedule.</td></tr> </tbody> </table> <p>The default value of this field is '0b'.</p>	Bit Value	Meaning	0	Do not process the Periodic Schedule.	1	Use the PERIODICLISTBASE register to access the Periodic Schedule.
Bit Value	Meaning								
0	Do not process the Periodic Schedule.								
1	Use the PERIODICLISTBASE register to access the Periodic Schedule.								
3:2	R/W or R	0	<p>Frame List Size</p> <p>This field is R/W only if Programmable Frame List Flag in the HCCPARAMS registers is set to a one. This field specifies the size of the</p> <p>Frame list. The size the frame list controls which bits in the Frame Index</p>						

			<p>Register should be used for the Frame List Current index.</p> <p>Values mean:</p> <table border="1"> <thead> <tr> <th>Bits</th><th>Meaning</th></tr> </thead> <tbody> <tr> <td>00b</td><td>1024 elements(4096bytes)Default value</td></tr> <tr> <td>01b</td><td>512 elements(2048bytes)</td></tr> <tr> <td>10b</td><td>256 elements(1024bytes)For resource-constrained condition</td></tr> <tr> <td>11b</td><td>reserved</td></tr> </tbody> </table> <p>The default value is '00b'.</p>	Bits	Meaning	00b	1024 elements(4096bytes)Default value	01b	512 elements(2048bytes)	10b	256 elements(1024bytes)For resource-constrained condition	11b	reserved
Bits	Meaning												
00b	1024 elements(4096bytes)Default value												
01b	512 elements(2048bytes)												
10b	256 elements(1024bytes)For resource-constrained condition												
11b	reserved												
1	R/W	0	<p>Host Controller Reset</p> <p>This control bit is used by software to reset the host controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset.</p> <p>When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports.</p> <p>All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller as described in Section 4.1 of the CHEI Specification in order to return the host controller to an operational state.</p> <p>This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register.</p> <p>Software should not set this bit to a one when the HC Halted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behaviour.</p>										
0	R/W	0	<p>Run/Stop</p> <p>When set to a 1, the Host Controller proceeds with execution of the schedule. When set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts. The Host Controller must halt within 16</p>										

			<p>micro-frames after software clears this bit.</p> <p>The HC Halted bit indicates when the Host Controller has finished its pending pipelined transactions and has entered the stopped state.</p> <p>Software must not write a one to this field unless the Host Controller is in the Halt State.</p> <p>The default value is 0x0.</p>
--	--	--	---

EHCI USB STATUS REGISTER

Offset: 0x14			Register Name: USBSTS
Default Value: 0x00001000			
Bit	Read/Write	Default	Description
31:16	/	0	<p>Reserved</p> <p>These bits are reserved and should be set to zero.</p>
15	R	0	<p>Asynchronous Schedule Status</p> <p>The bit reports the current real status of Asynchronous Schedule. If this bit is a zero then the status of the Asynchronous Schedule is disabled. If this bit is a one then the status of the Asynchronous Schedule is enabled. The Host Controller is not required to immediately disable or enable the Asynchronous Schedule when software transitions the Asynchronous Schedule Enable bit in the USBCMD register. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).</p>
14	R	0	<p>Periodic Schedule Status</p> <p>The bit reports the current real status of the Periodic Schedule. If this bit is a zero then the status of the Periodic Schedule is disabled. If this bit is a one then the status of the Periodic Schedule is enabled. The Host Controller is not required to <i>immediately</i> disable or enable the Periodic Schedule when software transitions the <i>Periodic Schedule Enable</i> bit in the USBCMD register. When this bit and the <i>Periodic Schedule Enable</i> bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).</p>
13	R	0	Reclamation

			This is a read-only status bit, which is used to detect an empty asynchronous schedule.
12	R	1	<p>HC Halted</p> <p>This bit is a zero whenever the Run/Stop bit is a one. The Host Controller Sets this bit to one after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the Host Controller Hardware (e.g. internal error).</p> <p>The default value is '1'.</p>
11:6	/	0	<p>Reserved</p> <p>These bits are reserved and should be set to zero.</p>
5	R/WC	0	<p>Interrupt on Async Advance</p> <p>System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.</p>
4	R/WC	0	<p>Host System Error</p> <p>The Host Controller set this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.</p>
3	R/WC	0	<p>Frame List Rollover</p> <p>The Host Controller sets this bit to a one when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size is 1024, the Frame Index Register rolls over every time FRINDEX [13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a one every time FRINDEX [12] toggles.</p>
2	R/WC	0	<p>Port Change Detect</p> <p>The Host Controller sets this bit to a one when any port for which the Port Owner bit is set to zero has a change bit transition from a zero to a one or a Force Port Resume bit transition from a zero to a one as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Chang being set to a one after</p>

			system software has relinquished ownership of a connected port by writing a one to a port's Port Owner bit.
1	R/WC	0	<p>USB Error Interrupt(USBERRINT)</p> <p>The Host Controller sets this bit to 1 when completion of USB transaction results in an error condition(e.g. error counter underflow).If the TD on which the error interrupt occurred also had its IOC bit set, both.</p> <p>This bit and USBINT bit are set.</p>
0	R/WC	0	<p>USB Interrupt(USBINT)</p> <p>The Host Controller sets this bit to a one on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set.</p> <p>The Host Controller also sets this bit to 1 when a short packet is detected</p> <p>(actual number of bytes received was less than the expected number of bytes)</p>

EHCI USB INTERRUPT ENABLE REGISTER

Offset: 0x18			Register Name: USBINTR
			Default Value:0x00000000
Bit	Read/Write	Default	Description
31:6	/	0	<p>Reserved</p> <p>These bits are reserved and should be zero.</p>
5	R/W	0	<p>Interrupt on Async Advance Enable</p> <p>When this bit is 1, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.</p>
4	R/W	0	<p>Host System Error Enable</p> <p>When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host</p>

			System Error bit.
3	R/W	0	<p>Frame List Rollover Enable</p> <p>When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.</p>
2	R/W	0	<p>Port Change Interrupt Enable</p> <p>When this bit is 1, and the Port Chang Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Chang Detect bit.</p>
1	R/W	0	<p>USB Error Interrupt Enable</p> <p>When this bit is 1, and the USBERRINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold.</p> <p>The interrupt is acknowledged by software clearing the USBERRINT bit.</p>
0	R/W	0	<p>USB Interrupt Enable</p> <p>When this bit is 1, and the USBINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold.</p> <p>The interrupt is acknowledged by software clearing the USBINT bit</p>

EHCI FRAME INDEX REGISTER

Offset: 0x1c			Register Name: FRINDEX
			Default Value: 0x00000000
Bit	Read/Write	Default	Description
31:14	/	0	Reserved These bits are reserved and should be zero.
13:0	R/W	0	Frame Index The value in this register increment at the end of each time

		<p>frame</p> <p>(e.g. micro-frame). Bits[N:3] are used for the Frame List current index. It</p> <p>Means that each location of the frame list is accessed 8 times(frames or</p> <p>Micro-frames) before moving to the next index. The following illustrates</p> <p>Values of N based on the value of the Frame List Size field in the USBCMD register.</p> <table border="1"> <thead> <tr> <th>USBCMD[Frame List Size]</th><th>Number Elements</th><th>N</th></tr> </thead> <tbody> <tr> <td>00b</td><td>1024</td><td>12</td></tr> <tr> <td>01b</td><td>512</td><td>11</td></tr> <tr> <td>10b</td><td>256</td><td>10</td></tr> <tr> <td>11b</td><td>Reserved</td><td></td></tr> </tbody> </table>	USBCMD[Frame List Size]	Number Elements	N	00b	1024	12	01b	512	11	10b	256	10	11b	Reserved	
USBCMD[Frame List Size]	Number Elements	N															
00b	1024	12															
01b	512	11															
10b	256	10															
11b	Reserved																

Note: This register must be written as a DWord. Byte writes produce undefined results.

EHCI PERIODIC FRAME LIST BASE ADDRESS REGISTER

Offset: 0x24			Register Name: PERIODICLISTBASE
			Default Value: Undefined
Bit	Read/Write	Default	Description
31:12	R/W		<p>Base Address</p> <p>These bits correspond to memory address signals [31:12], respectively.</p> <p>This register contains the beginning address of the Periodic Frame List in the system memory.</p> <p>System software loads this register prior to starting the schedule execution by the Host Controller. The memory structure referenced by this physical memory pointer is assumed to be 4-K byte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.</p>
11:0	/		Reserved

			Must be written as 0x0 during runtime, the values of these bits are undefined.
--	--	--	--

Note: Writes must be Dword Writes.

EHCI CURRENT ASYNCHRONOUS LIST ADDRESS REGISTER

Offset: 0x28			Register Name: ASYNCLISTADDR Default Value: Undefined
Bit	Read/Write	Default	Description
31:5	R/W		<p>Link Pointer (LP)</p> <p>This field contains the address of the next asynchronous queue head to be executed.</p> <p>These bits correspond to memory address signals [31:5], respectively.</p>
4:0	/	/	<p>Reserved</p> <p>These bits are reserved and their value has no effect on operation.</p> <p>Bits in this field cannot be modified by system software and will always return a zero when read.</p>

Note: Write must be DWord Writes.

EHCI CONFIGURE FLAG REGISTER

Offset: 0x50			Register Name: CONFIGFLAG Default Value: 0x00000000		
Bit	Read/Write	Default	Description		
31:1	/	0	<p>Reserved</p> <p>These bits are reserved and should be set to zero.</p>		
0	R/W	0	<p>Configure Flag(CF)</p> <p>Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic as follow:</p> <table border="1"> <tr> <th>Value</th> <th>Meaning</th> </tr> </table>	Value	Meaning
Value	Meaning				

			0	Port routing control logic default-routs each port to an implementation dependent classic host controller.
			1	Port routing control logic default-routs all ports to this host controller.
The default value of this field is '0'.				

Note: This register is not use in the normal implementation.

EHCI PORT STATUS AND CONTROL REGISTER

Offset: 0x54			Register Name: PORTSC					
Bit	Read/Write	Default	Description					
31:22	/	0	Reserved These bits are reserved for future use and should return a value of zero when read.					
21	R/W	0	Wake on Disconnect Enable(WKDSCNNT_E) Writing this bit to a one enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.					
20	R/W	0	Wake on Connect Enable(WKCNNT_E) Writing this bit to a one enable the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero. The default value in this field is '0'.					
19:16	R/W	0	Port Test Control The value in this field specifies the test mode of the port. The encoding of the test mode bits are as follow: <table border="1" style="margin-left: 20px;"> <tr> <td>Bits</td> <td>Test Mode</td> </tr> <tr> <td>0000b</td> <td>The port is NOT operating in a test mode.</td> </tr> </table>		Bits	Test Mode	0000b	The port is NOT operating in a test mode.
Bits	Test Mode							
0000b	The port is NOT operating in a test mode.							

			<table border="1"> <tr><td>0001b</td><td>Test J_STATE</td></tr> <tr><td>0010b</td><td>Test K_STATE</td></tr> <tr><td>0011b</td><td>Test SEO_NAK</td></tr> <tr><td>0100b</td><td>Test Packet</td></tr> <tr><td>0101b</td><td>Test FORCE_ENABLE</td></tr> <tr><td>0110b - 1111b</td><td>Reserved</td></tr> </table> <p>The default value in this field is '0000b'.</p>	0001b	Test J_STATE	0010b	Test K_STATE	0011b	Test SEO_NAK	0100b	Test Packet	0101b	Test FORCE_ENABLE	0110b - 1111b	Reserved
0001b	Test J_STATE														
0010b	Test K_STATE														
0011b	Test SEO_NAK														
0100b	Test Packet														
0101b	Test FORCE_ENABLE														
0110b - 1111b	Reserved														
15:14	R/W	0	<p>Reserved</p> <p>These bits are reserved for future use and should return a value of zero when read.</p>												
13	R/W	1	<p>Port Owner</p> <p>This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero.</p> <p>System software uses this field to release ownership of the port to selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.</p> <p>Default Value = 1b.</p>												
12	/	0	<p>Reserved</p> <p>These bits are reserved for future use and should return a value of zero when read.</p>												
11:10	R	0	<p>Line Status</p> <p>These bits reflect the current logical levels of the D+ (bit11) and D-(bit10) signal lines. These bits are used for detection of low-speed USB devices prior to port reset and enable sequence. This read only field is valid only when the port enable bit is zero and the current connect status bit is set to a one.</p> <p>The encoding of the bits are:</p>												

			Bit[11:10]	USB State	Interpretation	
			00b	SEO	Not Low-speed device, perform EHCI reset.	
			10b	J-state	Not Low-speed device, perform EHCI reset.	
			01b	K-state	Low-speed device, release ownership of port.	
			11b	Undefined	Not Low-speed device, perform EHCI reset.	
			This value of this field is undefined if Port Power is zero.			
9	/	0	Reserved This bit is reserved for future use, and should return a value of zero when read.			
8	R/W	0	<p>Port Reset</p> <p>1=Port is in Reset. 0=Port is not in Reset. Default value = 0.</p> <p>When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at a one long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes. Notes: when software writes this bit to a one , it must also write a zero to the Port Enable bit.</p> <p>Note that when software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g. set the Port Enable bit to a one). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero. For example: if the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state with 2ms of software writing this bit to a zero.</p> <p>The HC Halted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller</p>			

			<p>may hold Port Reset asserted to a one when the HC Halted bit is a one.</p> <p>This field is zero if Port Power is zero.</p>								
			<p>Suspend</p> <p>Port Enabled Bit and Suspend bit of this register define the port states as follows:</p> <table border="1"> <thead> <tr> <th>Bits[Port Enables, Suspend]</th> <th>Port State</th> </tr> </thead> <tbody> <tr> <td>0x</td> <td>Disable</td> </tr> <tr> <td>10</td> <td>Enable</td> </tr> <tr> <td>11</td> <td>Suspend</td> </tr> </tbody> </table> <p>When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspend and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.</p> <p>A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:</p> <ul style="list-style-type: none"> ① Software sets the Force Port Resume bit to a zero(from a one). ② Software sets the Port Reset bit to a one(from a zero). <p>If host software sets this bit to a one when the port is not enabled(i.e. Port enabled bit is a zero), the results are undefined.</p> <p>This field is zero if Port Power is zero.</p>	Bits[Port Enables, Suspend]	Port State	0x	Disable	10	Enable	11	Suspend
Bits[Port Enables, Suspend]	Port State										
0x	Disable										
10	Enable										
11	Suspend										
7	R/W	0	<p>The default value in this field is '0'.</p>								
6	R/W	0	<p>Force Port Resume</p> <p>1 = Resume detected/driven on port. 0 = No resume (K-state) detected/ driven on port. Default value = 0.</p> <p>This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspend and software transitions this bit to a one, then the</p>								

			<p>effects on the bus are undefined.</p> <p>Software sets this bit to a 1 drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a one because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a one. If software sets this bit to a one, the host controller must not set the Port Change Detect bit.</p> <p>Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (Full-speed 'K') is driven on the port as long as this remains a one. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from one) causes the port to return high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a one until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero.</p> <p>This field is zero if Port Power is zero.</p>
5	R/WC	0	<p>Over-current Change</p> <p>Default = 0. This bit gets set to a one when there is a change to Over-current Active. Software clears this bit by writing a one to this bit position.</p>
4	R	0	<p>Over-current Active</p> <p>0 = This port does not have an over-current condition. 1 = This port currently has an over-current condition. This bit will automatically transition from a one to a zero when the over current condition is removed.</p> <p>The default value of this bit is '0'.</p>
3	R/WC	0	<p>Port Enable/Disable Change</p> <p>Default = 0. 1 = Port enabled/disabled status has changed. 0 = No change.</p> <p>For the root hub, this bit gets set to a one only when a port is disabled due to the appropriate conditions existing at the EOF2 point (See Chapter 11 of the USB Specification for the definition of a Port Error). Software clears this bit by writing a</p>

			1 to it. This field is zero if Port Power is zero.
2	R/W	0	<p>Port Enabled/Disabled</p> <p>1=Enable, 0=Disable. Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a one when the reset sequence determines that the attached device is a high-speed device.</p> <p>Ports can be disabled by either a fault condition(disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events.</p> <p>When the port is disabled, downstream propagation of data is blocked on this port except for reset.</p> <p>The default value of this field is '0'.</p> <p>This field is zero if Port Power is zero.</p>
1	R/WC	0	<p>Connect Status Change</p> <p>1=Change in Current Connect Status, 0=No change, Default=0.</p> <p>Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be "setting" an already-set bit. Software sets this bit to 0 by writing a 1 to it.</p> <p>This field is zero if Port Power is zero.</p>
0	R	0	<p>Current Connect Status</p> <p>Device is present on port when the value of this field is a one, and no device is present on port when the value of this field is a zero. This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change(Bit 1) to be set.</p> <p>This field is zero if Port Power zero.</p>

Note: This register is only reset by hardware or in response to a host controller reset.

7.6.5 OHCI Register Description

HCREVISION REGISTER

Offset: 0x400				Register Name: HcRevision Default Value: 0x10
Bit	Read/Write		Default	Description
	HCD	HC		
31:8	/	/	0x00	Reserved
7:0	R	R	0x10	<p>Revision</p> <p>This read-only field contains the BCD representation of the version of the HCI specification that is implemented by this HC. For example, a value of 0x11 corresponds to version 1.1. All of the HC implementations that are compliant with this specification will have a value of 0x10.</p>

HCCONTROL REGISTER

Offset: 0x404				Register Name: HcRevision Default Value: 0x0
Bit	Read/Write		Default	Description
	HCD	HC		
31:11	/	/	0x00	Reserved
10	R/W	R	0x0	<p>RemoteWakeupEnable</p> <p>This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt.</p>
9	R/W	R/W	0x0	<p>RemoteWakeupConnected</p> <p>This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the</p>

				system, it is the responsibility of system firmware to set this bit during POST. HC clear the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this specification.								
8	R/W	R	0x0	<p>InterruptRouting</p> <p>This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupt are routed to the normal host bus interrupt mechanism. If set interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.</p>								
7:6	R/W	R/W	0x0	<p>HostControllerFunctionalState for USB</p> <table border="1"> <tr> <td>00b</td> <td>USBReset</td> </tr> <tr> <td>01b</td> <td>USBResume</td> </tr> <tr> <td>10b</td> <td>USBOperational</td> </tr> <tr> <td>11b</td> <td>USBSuspend</td> </tr> </table> <p>A transition to USBOperational from another state causes SOF generation to begin 1 ms later. HCD may determine whether HC has begun sending SOFs by reading the StartOfFrame field of HcInterruptStatus.</p> <p>This field may be changed by HC only when in the USBSUSPEND state. HC may move from the USBSUSPEND state to the USBRESUME state after detecting the resume signal from a downstream port.</p> <p>HC enters USBSUSPEND after a software reset, whereas it enters</p> <p>USBRESET after a hardware reset. The latter also resets the Root</p> <p>Hub and asserts subsequent reset signal to downstream ports.</p>	00b	USBReset	01b	USBResume	10b	USBOperational	11b	USBSuspend
00b	USBReset											
01b	USBResume											
10b	USBOperational											
11b	USBSuspend											
5	R/W	R	0x0	<p>BulkListEnable</p> <p>This bit is set to enable the processing of the Bulk list in the next</p> <p>Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it</p>								

				determines to process the list. When disabled, HCD may modify the list. If <i>HcBulkCurrentED</i> is pointing to an ED to be removed, HCD must advance the pointer by updating <i>HcBulkCurrentED</i> before re-enabling processing of the list.		
4	R/W	R	0x0	<p>ControlListEnable</p> <p>This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If <i>HcControlCurrentED</i> is pointing to an ED to be removed, HCD must advance the pointer by updating <i>HcControlCurrentED</i> before re-enabling processing of the list.</p>		
3	R/W	R	0x0	<p>IsochronousEnable</p> <p>This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists.</p> <p>Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).</p>		
2	R/W	R	0x0	<p>PeriodicListEnable</p> <p>This bit is set to enable the processing of periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.</p>		
1:0	R/W	R	0x0	<p>ControlBulkServiceRatio</p> <p>This specifies the service ratio between Control and Bulk EDs. Before processing any of the nonperiodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 20%;">CBSR</td> <td style="width: 80%;">No. of Control EDs Over Bulk EDs Served</td> </tr> </table>	CBSR	No. of Control EDs Over Bulk EDs Served
CBSR	No. of Control EDs Over Bulk EDs Served					

				<table border="1"> <tr><td>0</td><td>1:1</td></tr> <tr><td>1</td><td>2:1</td></tr> <tr><td>2</td><td>3:1</td></tr> <tr><td>3</td><td>4:1</td></tr> </table> <p>The default value is 0x0.</p>	0	1:1	1	2:1	2	3:1	3	4:1
0	1:1											
1	2:1											
2	3:1											
3	4:1											

HCCOMMANDSTATUS REGISTER

Offset: 0x408				Register Name: HcCommandStatus
Bit	Read/Write		Default	Description
31:18	/	/	0x0	Reserved
17:16	R	R/W	0x0	<p>SchedulingOverrunCount</p> <p>These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in <i>HcInterruptStatus</i> has already been set. This is used by HCD to monitor any persistent scheduling problem.</p>
15:4	/	/	0x0	Reserved
3	R/W	R/W	0x0	<p>OwnershipChangeRequest</p> <p>This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in <i>HcInterruptStatus</i>. After the changeover, this bit is cleared and remains so until the next request from OS HCD.</p>
2	R/W	R/W	0x0	<p>BulkListFilled</p> <p>This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list.</p> <p>When HC begins to process the head of the Bulk list, it checks BLF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to</p>

				continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled , then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.
1	R/W	R/W	0x0	<p>ControlListFilled</p> <p>This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list.</p> <p>When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.</p>
0	R/W	R/E	0x0	<p>HostControllerReset</p> <p>This bit is by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the USBsuspend state in which most of the operational registers are reset except those stated otherwise; e.g., the InterruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10 ms. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.</p>

HCINTERRUPTSTATUS REGISTER

Offset: 0x40c			Register Name: HcInterruptStatus	
			Default Value:0x00	
Bit	Read/Write		Default	Description
	HCD	HC		
31:7	/	/	0x0	Reserved
6	R/W	R/W	0x0	RootHubStatusChange

			0x1?	This bit is set when the content of <i>HcRhStatus</i> or the content of any of <i>HcRhPortStatus[NumberofDownstreamPort]</i> has changed.
5	R/W	R/W	0x0	<p>FrameNumberOverflow</p> <p>This bit is set when the MSb of <i>HcFmNumber</i> (bit 15) changes value, from 0 to 1 or from 1 to 0, and after <i>HccaFrameNumber</i> has been updated.</p>
4	R/W	R/W	0x0	<p>UnrecoverableError</p> <p>This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.</p>
3	R/W	R/W	0x0	<p>ResumeDetected</p> <p>This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the <i>USBRseume</i> state.</p>
2	R/W	R/W	0x0	<p>StartofFrame</p> <p>This bit is set by HC at each start of frame and after the update of <i>HccaFrameNumber</i>. HC also generates a SOF token at the same time.</p>
1	R/W	R/W	0x0	<p>WritebackDoneHead</p> <p>This bit is set immediately after HC has written <i>HcDoneHead</i> to <i>HccaDoneHead</i>. Further updates of the <i>HccaDoneHead</i> will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of <i>HccaDoneHead</i>.</p>
0	R/W	R/W	0x0	<p>SchedulingOverrun</p> <p>This bit is set when the USB schedule for the current Frame overruns and after the update of <i>HccaFrameNumber</i>. A scheduling overrun will also cause the SchedulingOverrunCount of <i>HcCommandStatus</i> to be Incremented.</p>

HCINTERRUPTENABLE REGISTER

Offset: 0x410	Register Name: HcInterruptEnable Register
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				Default Value: 0x0				
Bit	Read/Write		Default	Description				
	HCD	HC						
31	R/W	R	0x0	<p>MasterInterruptEnable</p> <p>A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as Master Interrupt Enable.</p>				
30:7	/	/	0x0	Reserved				
6	R/W	R	0x0	<p>RootHubStatusChange Interrupt Enable</p> <table border="1"> <tr> <td>0</td><td>Ignore;</td></tr> <tr> <td>1</td><td>Enable interrupt generation due to Root Hub Status Change;</td></tr> </table>	0	Ignore;	1	Enable interrupt generation due to Root Hub Status Change;
0	Ignore;							
1	Enable interrupt generation due to Root Hub Status Change;							
5	R/W	R	0x0	<p>FrameNumberOverflow Interrupt Enable</p> <table border="1"> <tr> <td>0</td><td>Ignore;</td></tr> <tr> <td>1</td><td>Enable interrupt generation due to Frame Number Over Flow;</td></tr> </table>	0	Ignore;	1	Enable interrupt generation due to Frame Number Over Flow;
0	Ignore;							
1	Enable interrupt generation due to Frame Number Over Flow;							
4	R/W	R	0x0	<p>UnrecoverableError Interrupt Enable</p> <table border="1"> <tr> <td>0</td><td>Ignore;</td></tr> <tr> <td>1</td><td>Enable interrupt generation due to Unrecoverable Error;</td></tr> </table>	0	Ignore;	1	Enable interrupt generation due to Unrecoverable Error;
0	Ignore;							
1	Enable interrupt generation due to Unrecoverable Error;							
3	R/W	R	0x0	<p>ResumeDetected Interrupt Enable</p> <table border="1"> <tr> <td>0</td><td>Ignore;</td></tr> <tr> <td>1</td><td>Enable interrupt generation due to Resume Detected;</td></tr> </table>	0	Ignore;	1	Enable interrupt generation due to Resume Detected;
0	Ignore;							
1	Enable interrupt generation due to Resume Detected;							
2	R/W	R	0x0	<p>StartofFrame Interrupt Enable</p> <table border="1"> <tr> <td>0</td><td>Ignore;</td></tr> <tr> <td>1</td><td>Enable interrupt generation due to Start of Flame;</td></tr> </table>	0	Ignore;	1	Enable interrupt generation due to Start of Flame;
0	Ignore;							
1	Enable interrupt generation due to Start of Flame;							
1	R/W	R	0x0	<p>WritebackDoneHead Interrupt Enable</p> <table border="1"> <tr> <td>0</td><td>Ignore;</td></tr> </table>	0	Ignore;		
0	Ignore;							

				1	Enable interrupt generation due to Write back Done Head;
0	R/W	R	0x0	SchedulingOverrun Interrupt Enable	
				0	Ignore;
				1	Enable interrupt generation due to Scheduling Overrun;

HCINTERRUPTDISABLE REGISTER

Offset: 0x414				Register Name: HcInterruptDisable Register					
Bit	Read/Write		Default	Description					
	HCD	HC							
31	R/W	R	0x0	MasterInterruptEnable A written '0' to this field is ignored by HC. A '1' written to this field disables interrupt generation due events specified in the other bits of this register. This field is set after a hardware or software reset.					
30:7	/	/	0x00	Reserved					
6	R/W	R	0x0	RootHubStatusChange Interrupt Disable <table border="1"> <tr> <td>0</td> <td>Ignore;</td> </tr> <tr> <td>1</td> <td>Disable interrupt generation due to Root Hub Status Change;</td> </tr> </table>	0	Ignore;	1	Disable interrupt generation due to Root Hub Status Change;	
0	Ignore;								
1	Disable interrupt generation due to Root Hub Status Change;								
5	R/W	R	0x0	FrameNumberOverflow Interrupt Disable <table border="1"> <tr> <td>0</td> <td>Ignore;</td> </tr> <tr> <td>1</td> <td>Disable interrupt generation due to Frame Number Over Flow;</td> </tr> </table>	0	Ignore;	1	Disable interrupt generation due to Frame Number Over Flow;	
0	Ignore;								
1	Disable interrupt generation due to Frame Number Over Flow;								
4	R/W	R	0x0	UnrecoverableError Interrupt Disable <table border="1"> <tr> <td>0</td> <td>Ignore;</td> </tr> <tr> <td>1</td> <td>Disable interrupt generation due to Unrecoverable Error;</td> </tr> </table>	0	Ignore;	1	Disable interrupt generation due to Unrecoverable Error;	
0	Ignore;								
1	Disable interrupt generation due to Unrecoverable Error;								
3	R/W	R	0x0	ResumeDetected Interrupt Disable					

					0	Ignore;
					1	Disable interrupt generation due to Resume Detected;
2	R/W	R	0x0	StartofFrame Interrupt Disable		
				0	Ignore;	
				1	Disable interrupt generation due to Start of Flame;	
1	R/W	R	0x0	WritebackDoneHead Interrupt Disable		
				0	Ignore;	
				1	Disable interrupt generation due to Write back Done Head;	
0	R/w	R	0x0	SchedulingOverrun Interrupt Disable		
				0	Ignore;	
				1	Disable interrupt generation due to Scheduling Overrun;	

HCHCCA REGISTER

Offset: 0x418				Register Name: HcHCCA
Bit	Read/Write		Default	Description
	HCD	HC		
31:8	R/W	R	0x0	HCCA[31:8] This is the base address of the Host Controller Communication Area. This area is used to hold the control structures and the Interrupt table that are accessed by both the Host Controller and the Host Controller Driver.
7:0	R	R	0x0	HCCA[7:0] The alignment restriction in HcHCCA register is evaluated by examining the number of zeros in the lower order bits. The minimum alignment is 256 bytes, therefore, bits 0 through 7 must always return 0 when read.

HC PERIOD CURRENTED REGISTER

				Register Name: HcPeriodCurrentED(PCED)
Offset: 0x41c				Default Value: 0x0
Bit	Read/Write		Default	Description
31:4	HCD	HC	0x0	<p>PCED[31:4]</p> <p>This is used by HC to point to the head of one of the Periodic list which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.</p>
3:0	R	R/W	0x0	<p>PCED[3:0]</p> <p>Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.</p>

HC CONTROL HEADED REGISTER

				Register Name: HcControlHeadED[CHED]
Offset: 0x420				Default Value: 0x0
Bit	Read/Write		Default	Description
31:4	HCD	HC	0x0	<p>EHCD[31:4]</p> <p>The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list. HC traverse the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.</p>
3:0	R/W	R	0x0	<p>EHCD[3:0]</p> <p>Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.</p>

HCCONTROLCURRENTED REGISTER

				Register Name: HcControlCurrentED[CCED]
Offset: 0x424				Default Value: 0x0
Bit	Read/Write		Default	Description
	HCD	HC		
31:4	R/W	R/W	0x0	<p>CCED[31:4]</p> <p>The pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, HC checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing.</p> <p>HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.</p>
3:0	R	R	0x0	<p>CCED[3:0]</p> <p>Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.</p>

HCBULKHEADED REGISTER

				Register Name: HcBulkHeadED[BHED]
Offset: 0x428				Default Value: 0x0
Bit	Read/Write		Default	Description
	HCD	HC		
31:4	R/W	R	0x0	<p>BHED[31:4]</p> <p>The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.</p>
3:0	R	R	0x0	BHED[3:0]

				Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.
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HCBULKCURRENTED REGISTER

Offset: 0x42c				Register Name: HcBulkCurrentED [BCED]
Bit	Read/Write		Default	Description
	HCD	HC		
31:4	R/W	R/W	0x0	<p>BulkCurrentED[31:4]</p> <p>This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of <i>HcControl</i>. If set, it copies the content of <i>HcBulkHeadED</i> to <i>HcBulkCurrentED</i> and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of <i>HcControl</i> is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.</p>
3:0	R	R	0x0	<p>BulkCurrentED [3:0]</p> <p>Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.</p>

HCDONEHEAD REGISTER

Offset: 0x430				Register Name: HcDoneHead
Bit	Read/Write		Default	Description
	HCD	HC		
31:4	R	R/W	0x0	HcDoneHead[31:4] When a TD is completed, HC writes the content of

				<p><i>HcDoneHead</i> to the NextTD field of the TD. HC then overwrites the content of <i>HcDoneHead</i> with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of <i>HcInterruptStatus</i>.</p>
3:0	R	R	0x0	<p><i>HcDoneHead[3:0]</i></p> <p>Because the general TD length is 16 bytes, the memory structure for the TD must be aligned to a 16-byte boundary. So the lower bits in the PCED, through bit 0 to bit 3 must be zero in this field.</p>

HCFMINTERVAL REGISTER

Offset: 0x434				Register Name: HcFmInterval Register Default Value: 0x2EDF
Bit	Read/Write		Default	Description
	HCD	HC		
31	R/W	R	0x0	<p>FrameIntervalToggler</p> <p>HCD toggles this bit whenever it loads a new value to FrameInterval.</p>
30:16	R/W	R	0x0	<p>FSLargestDataPacket</p> <p>This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.</p>
15:14	/	/	0x0	Reserved
13:0	R/W	R	0x2edf	<p>FrameInterval</p> <p>This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to be 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of <i>HcCommandStatus</i> as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.</p>

HCFMREMAINING REGISTER

				Register Name: HcFmRemaining
Offset: 0x438				Default Value: 0x0
Bit	Read/Write		Default	Description
31	R	R/W	0x0	<p>FrameRemaining Toggle</p> <p>This bit is loaded from the FrameIntervalToggle field of <i>HcFmInterval</i> whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.</p>
30:14	/	/	0x0	Reserved
13:0	R	RW	0x0	<p>FramRemaining</p> <p>This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in <i>HcFmInterval</i> at the next bit time boundary. When entering the USBOPERATIONAL state, HC re-loads the content with the FrameInterval of <i>HcFmInterval</i> and uses the updated value from the next SOF.</p>

HCFMNUMBER REGISTER

				Register Name: HcFmNumber
Offset: 0x43c				Default Value: 0x0
Bit	Read/Write		Default	Description
31:16				Reserved
15:0	R	R/W	0x0	<p>FrameNumber</p> <p>This is incremented when <i>HcFmRemaining</i> is re-loaded. It will be rolled over to 0x0 after 0xffff. When entering the USBOPERATIONAL state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in <i>HcInterruptStatus</i>.</p>

HC PERIODIC START REGISTER

				Register Name: HcPeriodicStatus
Offset: 0x440				Default Value: 0x0
Bit	Read/Write		Default	Description
	HCD	HC		
31:14				Reserved
13:0	R/W	R	0x0	<p>PeriodicStart</p> <p>After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from <i>HcFmInterval</i>. A typical value will be 0x2A3F (0x3e67??). When <i>HcFmRemaining</i> reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.</p>

HCLSTHRESHOLD REGISTER

				Register Name: HcLSThreshold
Offset: 0x444				Default Value: 0x0628
Bit	Read/Write		Default	Description
	HCD	HC		
31:12				Reserved
11:0	R/W	R	0x0628	<p>LSThreshold</p> <p>This field contains a value which is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ³ this field. The value is calculated by HCD with the consideration of transmission and setup overhead.</p>

HCRHDESCRIPTORA REGISTER

				Register Name: HcRhDescriptorA				
Offset: 0x448				Default Value:				
Bit	Read/Write		Default	Description				
31:24	R/W	R	0x2	<p>PowerOnToPowerGoodTime[POTPGT]</p> <p>This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2 ms. The duration is calculated as POTPGT * 2ms.</p>				
23:13				Reserved				
12	R/W	R	1	<p>NoOverCurrentProtection</p> <p>This bit describes how the overcurrent status for the Root Hub ports are reported. When this bit is cleared, the OverCurrentProtectionMode field specifies global or per-port reporting.</p> <table border="1"> <tr> <td>0</td><td>Over-current status is reported collectively for all downstream ports.</td></tr> <tr> <td>1</td><td>No overcurrent protection supported.</td></tr> </table>	0	Over-current status is reported collectively for all downstream ports.	1	No overcurrent protection supported.
0	Over-current status is reported collectively for all downstream ports.							
1	No overcurrent protection supported.							
11	R/W	R	0	<p>OverCurrentProtectionMode</p> <p>This bit describes how the overcurrent status for the Root Hub ports are reported. At reset, these fields should reflect the same mode as PowerSwitchingMode. This field is valid only if the NoOverCurrentProtection field is cleared.</p> <table border="1"> <tr> <td>0</td><td>Over-current status is reported collectively for all downstream ports.</td></tr> <tr> <td>1</td><td>Over-current status is reported on per-port basis.</td></tr> </table>	0	Over-current status is reported collectively for all downstream ports.	1	Over-current status is reported on per-port basis.
0	Over-current status is reported collectively for all downstream ports.							
1	Over-current status is reported on per-port basis.							
10	R	R	0x0	<p>Device Type</p> <p>This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write 0.</p>				
9	R/W	R	1	<p>PowerSwitchingMode</p> <p>This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field</p>				

				is only valid if the NoPowerSwitching field is cleared.				
				<table border="1"> <tr> <td>0</td><td>All ports are powered at the same time.</td></tr> <tr> <td>1</td><td>Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).</td></tr> </table>	0	All ports are powered at the same time.	1	Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
0	All ports are powered at the same time.							
1	Each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).							
8	R/W	R	0	<p>NoPowerSwithcing</p> <p>These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching.</p> <table border="1"> <tr> <td>0</td><td>Ports are power switched.</td></tr> <tr> <td>1</td><td>Ports are always powered on when the HC is powered on.</td></tr> </table>	0	Ports are power switched.	1	Ports are always powered on when the HC is powered on.
0	Ports are power switched.							
1	Ports are always powered on when the HC is powered on.							
7:0	R	R	0x01	<p>NumberDownstreamPorts</p> <p>These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported.</p>				

HCRHDESCRIPTORB REGISTER

Offset: 0x44c			Register Name: HcRhDescriptorB Register	
Bit	Read/Write		Default	Description
	HCD	HC		
31:16	R/W	R	0x0	<p>PortPowerControlMask</p> <p>Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode</p>

				= 0), this field is not valid.										
				Bit0 Reserved										
				Bit1 Ganged-power mask on Port #1.										
				Bit2 Ganged-power mask on Port #2.										
				...										
				Bit15 Ganged-power mask on Port #15.										
15:0	R/W	R	0x0	<p>DeviceRemovable</p> <p>Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable.</p> <table border="1"> <tr> <td>Bit0</td><td>Reserved</td></tr> <tr> <td>Bit1</td><td>Device attached to Port #1.</td></tr> <tr> <td>Bit2</td><td>Device attached to Port #2.</td></tr> <tr> <td>...</td><td></td></tr> <tr> <td>Bit15</td><td>Device attached to Port #15.</td></tr> </table>	Bit0	Reserved	Bit1	Device attached to Port #1.	Bit2	Device attached to Port #2.	...		Bit15	Device attached to Port #15.
Bit0	Reserved													
Bit1	Device attached to Port #1.													
Bit2	Device attached to Port #2.													
...														
Bit15	Device attached to Port #15.													

HCRHSTATUS REGISTER

Offset: 0x450				Register Name: HcRhStatus Register
Default Value:				
Bit	Read/Write		Default	Description
31	W	R	0	(write)ClearRemoteWakeupEnable Write a '1' clears DeviceRemoteWakeupEnable . Write a '0' has no effect.
30:18	/	/	0x0	Reserved
17	R/W	R	0	OverCurrentIndicatorChang This bit is set by hardware when a change has occurred to the OverCurrentIndicator field of this register. The HCD clears this bit by writing a '1'. Writing a '0' has no effect.

				(read)LocalPowerStartusChange The Root Hub does not support the local power status features, thus, this bit is always read as '0'. (write)SetGlobalPower In global power mode (PowerSwitchingMode =0), This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.				
16	R/W	R	0x0	(read)DeviceRemoteWakeupEnable This bit enables a ConnectStatusChange bit as a resume event, causing a USBSUSPEND to USBRESUME state transition and setting the ResumeDetected interrupt. <table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td style="padding: 2px;">0</td><td style="padding: 2px;">ConnectStatusChange is not a remote wakeup event.</td></tr> <tr> <td style="padding: 2px;">1</td><td style="padding: 2px;">ConnectStatusChange is a remote wakeup event.</td></tr> </table> (write)SetRemoteWakeupEnable Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.	0	ConnectStatusChange is not a remote wakeup event.	1	ConnectStatusChange is a remote wakeup event.
0	ConnectStatusChange is not a remote wakeup event.							
1	ConnectStatusChange is a remote wakeup event.							
15	R/W	R	0x0	Reserved				
14:2				Reserved				
1	R	R/W	0x0	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always '0'				
0	R/W	R	0x0	(Read)LocalPowerStatus When read, this bit returns the LocalPowerStatus of the Root Hub. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write)ClearGlobalPower When write, this bit is operated as the ClearGlobalPower. In global power mode (PowerSwitchingMode =0), This bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears				

				PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.
--	--	--	--	---

HCRHPORTSTATUS REGISTER

Offset: 0x454				Register Name: HcRhPortStatus				
Bit	Read/Write		Default	Description				
	HCD	HC						
31:21	/	/	0x0	Reserved				
20	R/W	R/W	0x0	<p>PortResetStatusChange This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.</p> <table border="1"> <tr> <td>0</td><td>port reset is not complete</td></tr> <tr> <td>1</td><td>port reset is complete</td></tr> </table>	0	port reset is not complete	1	port reset is complete
0	port reset is not complete							
1	port reset is complete							
19	R/W	R/W	0x0	<p>PortOverCurrentIndicatorChange This bit is valid only if overcurrent conditions are reported on a per-port basis. This bit is set when Root Hub changes the PortOverCurrentIndicator bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.</p> <table border="1"> <tr> <td>0</td><td>no change in PortOverCurrentIndicator</td></tr> <tr> <td>1</td><td>PortOverCurrentIndicator has changed</td></tr> </table>	0	no change in PortOverCurrentIndicator	1	PortOverCurrentIndicator has changed
0	no change in PortOverCurrentIndicator							
1	PortOverCurrentIndicator has changed							
18	R/W	R/W	0x0	<p>PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resynchronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set.</p> <table border="1"> <tr> <td>0</td><td>resume is not completed</td></tr> <tr> <td>1</td><td>resume completed</td></tr> </table>	0	resume is not completed	1	resume completed
0	resume is not completed							
1	resume completed							
17	R/W	R/W	0x0	<p>PortEnableStatusChange This bit is set when hardware events cause the</p>				

				<p>PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect.</p> <table border="1"> <tr> <td>0</td><td>no change in PortEnableStatus</td></tr> <tr> <td>1</td><td>change in PortEnableStatus</td></tr> </table>	0	no change in PortEnableStatus	1	change in PortEnableStatus
0	no change in PortEnableStatus							
1	change in PortEnableStatus							
16	R/W	R/W	0x0	<p>ConnectStatusChange</p> <p>This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected.</p> <table border="1"> <tr> <td>0</td><td>no change in PortEnableStatus</td></tr> <tr> <td>1</td><td>change in PortEnableStatus</td></tr> </table> <p>Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.</p>	0	no change in PortEnableStatus	1	change in PortEnableStatus
0	no change in PortEnableStatus							
1	change in PortEnableStatus							
15:10	/	/	0x0	Reserved				
9	R/W	R/W	-	<p>(read) LowSpeedDeviceAttached</p> <p>This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set.</p> <table border="1"> <tr> <td>0</td><td>full speed device attached</td></tr> <tr> <td>1</td><td>low speed device attached</td></tr> </table> <p>(write) ClearPortPower</p> <p>The HCD clears the PortPowerStatus bit by writing a '1' to this bit. Writing a '0' has no effect.</p>	0	full speed device attached	1	low speed device attached
0	full speed device attached							
1	low speed device attached							

				(read)PortPowerStatus				
8	R/W	R/W	0x1	<p>This bit reflects the port's power status, regardless of the type of power switching implemented. This bit is cleared if an overcurrent condition is detected. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NumberDownstreamPort]. In global switching mode(PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset.</p> <table border="1"> <tr> <td>0</td><td>port power is off</td></tr> <tr> <td>1</td><td>port power is on</td></tr> </table>	0	port power is off	1	port power is on
0	port power is off							
1	port power is on							
7:5	/	/	0x0	(write)SetPortPower				
4	R/W	R/W	0x0	<p>The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect.</p> <p>Note: This bit is always reads '1b' if power switching is not supported.</p> <p>Reserved</p> <p>(read)PortResetStatus</p> <p>When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared.</p> <table border="1"> <tr> <td>0</td><td>port reset signal is not active</td></tr> </table>	0	port reset signal is not active		
0	port reset signal is not active							

				<table border="1"> <tr> <td>1</td><td>port reset signal is active</td></tr> </table>	1	port reset signal is active		
1	port reset signal is active							
				<p>(write)SetPortReset</p> <p>The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.</p>				
3	R/W	R/W	0x0	<p>(read)PortOverCurrentIndicator</p> <p>This bit is only valid when the Root Hub is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is not supported, this bit is set to 0. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. This bit always reflects the overcurrent input signal.</p> <table border="1"> <tr> <td>0</td> <td>no overcurrent condition.</td> </tr> <tr> <td>1</td> <td>overcurrent condition detected.</td> </tr> </table> <p>(write)ClearSuspendStatus</p> <p>The HCD writes a '1' to initiate a resume. Writing a '0' has no effect. A resume is initiated only if PortSuspendStatus is set.</p>	0	no overcurrent condition.	1	overcurrent condition detected.
0	no overcurrent condition.							
1	overcurrent condition detected.							
2	R/W	R/W	0x0	<p>(read)PortSuspendStatus</p> <p>This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the USBRESUME state. If an upstream resume is in progress, it should propagate to the HC.</p> <table border="1"> <tr> <td>0</td> <td>port is not suspended</td> </tr> <tr> <td>1</td> <td>port is suspended</td> </tr> </table> <p>(write)SetPortSuspend</p>	0	port is not suspended	1	port is suspended
0	port is not suspended							
1	port is suspended							

				The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus ; instead it sets ConnectStatusChange . This informs the driver that it attempted to suspend a disconnected port.				
1	R/W	R/W	0x0	<p>(read)PortEnableStatus</p> <p>This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set.</p> <table border="1"> <tr> <td>0</td><td>port is disabled</td></tr> <tr> <td>1</td><td>port is enabled</td></tr> </table> <p>(write)SetPortEnable</p> <p>The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected Port.</p>	0	port is disabled	1	port is enabled
0	port is disabled							
1	port is enabled							
0	R/W	R/W	0x0	<p>(read)CurrentConnectStatus</p> <p>This bit reflects the current state of the downstream port.</p> <table border="1"> <tr> <td>0</td><td>No device connected</td></tr> <tr> <td>1</td><td>Device connected</td></tr> </table> <p>(write)ClearPortEnable</p> <p>The HCD writes a '1' to clear the PortEnableStatus bit. Writing '0' has no effect. The CurrentConnectStatus is not affected by any write.</p> <p>Note: This bit is always read '1' when the attached device is</p>	0	No device connected	1	Device connected
0	No device connected							
1	Device connected							

				nonremovable(DviceRemoveable[NumberDownstreamPort]).
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USB HOST SPECIAL REQUIREMENT

USB Host Clock Requirement

Name	Description
HCLK	System clock (provided by AHB bus clock). This clock needs to be >30MHz.
CLK60M	Clock from PHY for HS SIE, is constant to be 60MHz.
CLK48M	Clock from PLL for FS/LS SIE, is constant to be 48MHz.

7.7 Digital Audio Interface

7.7.1 Overview

The Digital Audio Interface can be configured as I2S interface or PCM interface.

When configured as I2S interface, it can support the industry standard format for I2S, left-justified, or right-justified. PCM is a standard method used to digital audio for transmission over digital communication channels.

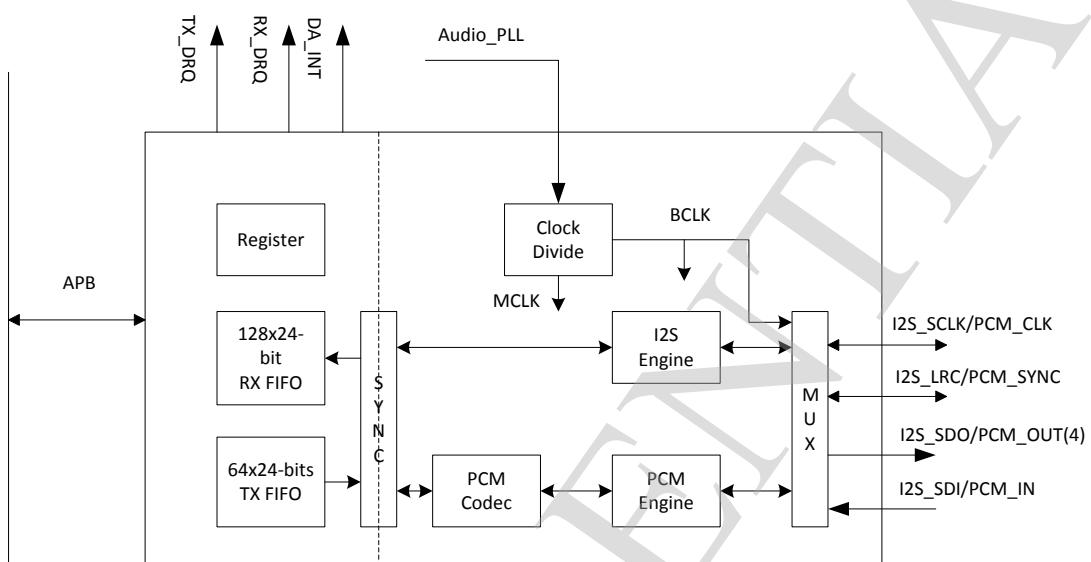
It supports linear 13 or 16-bits linear, or 8-bit u-law or A-law companded sample formats at 8K samples/s and can receive and transmit on any selection of four of the first four slots following PCM_SYNC.

It includes the following features:

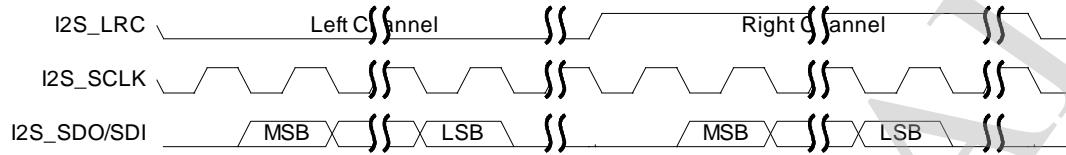
- I2S or PCM configured by software
- Full-duplex synchronous serial interface
- Master / Slave Mode operation configured by software
- Audio data resolutions of 16, 20, 24
- I2S audio data sample rate from 8KHz to 192KHz
- I2S Data format for standard I2S, Left Justified and Right Justified
- I2S supports 2-channel output and 2-channel input
- PCM supports linear sample (8-bits or 16-bits), 8-bits u-law and A-law companded sample
- One 128x24-bits FIFO for data transmit, one 64x24-bits FIFO for data receive
- Programmable FIFO thresholds
- Interrupt and DMA support
- Two 32-bits counters for A/V sync application
- Loopback mode for test
- 2 sets of digital audio interface

7.7.2 Block Diagram

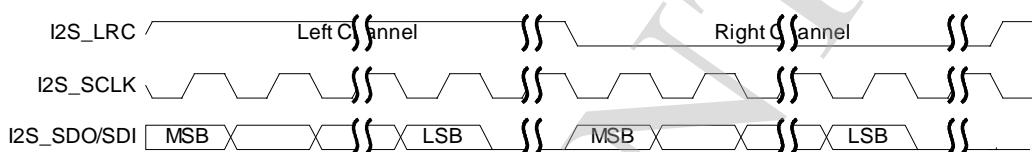
The digital audio interface block diagram is shown below:



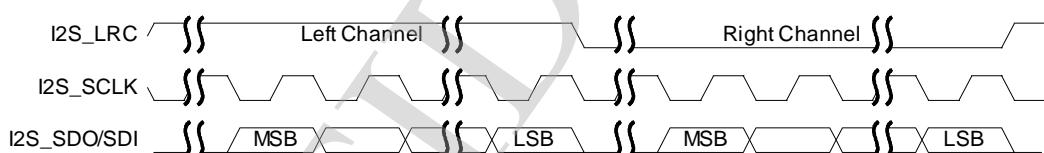
7.7.3 Digital Audio Interface Timing Diagram



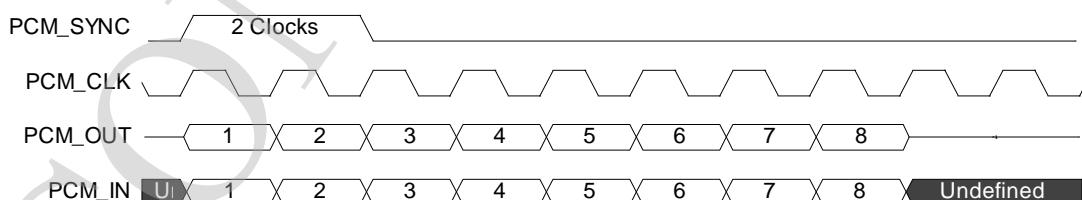
Standard I2S Timing Diagram



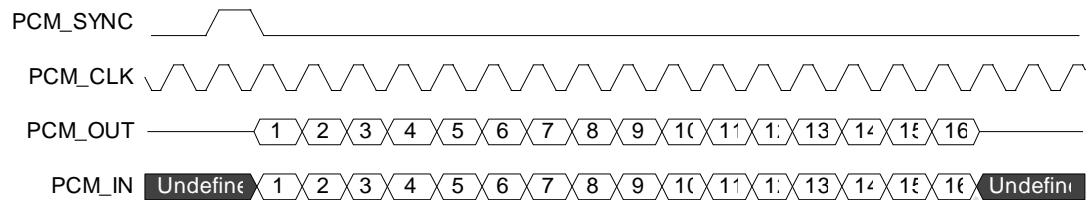
Left-justified I2S Timing Diagram



Right-justified I2S Timing Diagram



PCM Long Frame SYNC Timing Diagram (8-bits Companded Sample Example)



PCM Short Frame SYNC Timing Diagram (16-bits sample example)

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7.7.4 Digital Audio Interface Register List

Module Name	Base Address
DA0	0x01C22000
DA1	0x01C22400

Register Name	Offset	Description
DA_CTL	0x00	Digital Audio Control Register
DA_FATO	0x04	Digital Audio Format Register 0
DA_FAT1	0x08	Digital Audio Format Register 1
DA_TXFIFO	0x0C	Digital Audio TX FIFO Register
DA_RXFIFO	0x10	Digital Audio RX FIFO Register
DA_FCTL	0x14	Digital Audio FIFO Control Register
DA_FSTA	0x18	Digital Audio FIFO Status Register
DA_INT	0x1C	Digital Audio Interrupt Control Register
DAISTA	0x20	Digital Audio Interrupt Status Register
DA_CLKD	0x24	Digital Audio Clock Divide Register
DA_TXCNT	0x28	Digital Audio RX Sample Counter Register
DA_RXCNT	0x2C	Digital Audio TX Sample Counter Register
DA_TXCHSEL	0x30	Digital Audio TX Channel Select register
DA_TXCHMAP	0x34	Digital Audio TX Channel Mapping Register

7.7.5 Digital Audio Interface Register Description

DIGITAL AUDIO CONTROL REGISTER

Offset: 0x00			Register Name: DA_CTL Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:9	/	/	/
8	R/W	0	SDO_EN 0: Disable 1: Enable
7	/	/	/
6	R/W	0	ASS Audio sample select when TX FIFO under run 0: Sending zero 1: Sending last audio sample
5	R/W	0	MS Master Slave Select 0: Master 1: Slave
4	R/W	0	PCM 0: I2S Interface 1: PCM Interface
3	R/W	0	LOOP Loop back test 0: Normal mode 1: Loop back test When set '1', connecting the SDO with the SDI in Master mode.

2	R/W	0	TXEN Transmitter Block Enable 0: Disable 1: Enable
1	R/W	0	RXEN Receiver Block Enable 0: Disable 1: Enable
0	R/W	0	GEN Globe Enable A disable on this bit overrides any other block or channel enables and flushes all FIFOs. 0: Disable 1: Enable

DIGITAL AUDIO FORMAT REGISTER 0

Offset: 0x04			Register Name: DA_FATO
Default Value: 0x0000_000C			
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0	LRCP Left/ Right Clock Parity 0: Normal 1: Inverted In DSP/ PCM mode 0: MSB is available on 2nd BCLK rising edge after LRC rising edge 1: MSB is available on 1st BCLK rising edge after LRC rising edge
6	R/W	0	BCP

			BCLK Parity 0: Normal 1: Inverted
5:4	R/W	0	SR Sample Resolution 00: 16-bits 01: 20-bits 10: 24-bits 11: Reserved
3:2	R/W	0x3	WSS Word Select Size 00: 16 BCLK 01: 20 BCLK 10: 24 BCLK 11: 32 BCLK
1:0	R/W	0	FMT Serial Data Format 00: Standard I2S Format 01: Left Justified Format 10: Right Justified Format 11: Reserved

DIGITAL AUDIO FORMAT REGISTER 1

Offset: 0x08			Register Name: DA_FAT1 Default Value: 0x0000_4020
Bit	Read/Write	Default	Description
31:15	/	/	/
14:12	R/W	0x4	PCM_SYNC_PERIOD PCM SYNC Period Clock Number

			000: 16 BCLK period 001: 32 BCLK period 010: 64 BCLK period 011: 128 BCLK period 100: 256 BCLK period Others : Reserved
11	R/W	0	PCM_SYNC_OUT PCM Sync Out 0: Enable PCM_SYNC output in Master mode 1: Suppress PCM_SYNC whilst keeping PCM_CLK running. Some Codec utilize this to enter a low power state.
10	R/W	0	PCM Out Mute Write 1 force PCM_OUT to 0
9	R/W	0	MLS MSB / LSB First Select 0: MSB First 1: LSB First
8	R/W	0	SEXT Sign Extend (only for 16 bits slot) 0: Zeros or audio gain padding at LSB position 1: Sign extension at MSB position When writing the bit is 0, the unused bits are audio gain for 13-bit linear sample and zeros padding for 8-bit companding sample. When writing the bit is 1, the unused bits are both sign extension.
7:6	R/W	0	SI Slot Index 00: the 1st slot 01: the 2nd slot

			10: the 3rd slot 11: the 4th slot
5	R/W	1	SW Slot Width 0: 8 clocks width 1: 16 clocks width Notes: For A-law or u-law PCM sample, if this bit is set to 1, eight zero bits are following with PCM sample.
4	R/W	0	SSYNC Short Sync Select 0: Long Frame Sync 1: Short Frame Sync It should be set '1' for 8 clocks width slot.
3:2	R/W	0	RX_PDM PCM Data Mode 00: 16-bits Linear PCM 01: 8-bits Linear PCM 10: 8-bits u-law 11: 8-bits A-law
1:0	R/W	0	TX_PDM PCM Data Mode 00: 16-bits Linear PCM 01: 8-bits Linear PCM 10: 8-bits u-law 11: 8-bits A-law

DIGITAL AUDIO TX FIFO REGISTER

Offset: 0x0C	Register Name: DA_TXFIFO Default Value: 0x0000_0000
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Bit	Read/Write	Default	Description
31:0	W	0	<p>TX_DATA</p> <p>TX Sample</p> <p>Transmitting left, right channel sample data should be written this register one by one. The left channel sample data is first and then the right channel sample.</p>

DIGITAL AUDIO RX FIFO REGISTER

Offset: 0x10			Register Name: DA_RXFIFO Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	R	0	<p>RX_DATA</p> <p>RX Sample</p> <p>Host can get one sample by reading this register. The left channel sample data is first and then the right channel sample.</p>

DIGITAL AUDIO FIFO CONTROL REGISTER

Offset: 0x14			Register Name: DA_FCTL Default Value: 0x0004_00F0
Bit	Read/Write	Default	Description
31	R/W	0	<p>FIFOSRC</p> <p>TX FIFO source select</p> <p>0: APB bus</p> <p>1: Analog Audio CODEC</p>
30:26	/	/	/
25	R/W	0	<p>FTX</p> <p>Write '1' to flush TX FIFO, self clear to '0'.</p>
24	R/W	0	<p>FRX</p> <p>Write '1' to flush RX FIFO, self clear to '0'.</p>
23:19	/	/	/

			TXTL
			TX FIFO Empty Trigger Level
			Interrupt and DMA request trigger level for TXFIFO normal condition
18:12	R/W	0x40	Trigger Level = TXTL
11:10	/	/	/
			RXTL
			RX FIFO Trigger Level
			Interrupt and DMA request trigger level for RXFIFO normal condition
9:4	R/W	0xF	Trigger Level = RXTL + 1
3	/	/	/
			TXIM
			TX FIFO Input Mode (Mode 0, 1)
			0: Valid data at the MSB of TXFIFO register
			1: Valid data at the LSB of TXFIFO register
			Example for 20-bits transmitted audio sample:
			Mode 0: FIFO_I[23:0] = {4'h0, TXFIFO[31:12]}
			Mode 1: FIFO_I[23:0] = {4'h0, TXFIFO[19:0]}
2	R/W	0	
			RXOM
			RX FIFO Output Mode (Mode 0, 1, 2, 3)
			00: Expanding '0' at LSB of DA_RXFIFO register.
			01: Expanding received sample sign bit at MSB of DA_RXFIFO register.
			10: Truncating received samples at high half-word of DA_RXFIFO register and low half-word of DA_RXFIFO register is filled by '0'.
			11: Truncating received samples at low half-word of DA_RXFIFO register and high half-word of DA_RXFIFO register is expanded by its sign bit.
1:0	R/W	0	Example for 20-bits received audio sample:

			Mode 0: RXFIFO[31:0] = {FIFO_O[19:0], 12'h0} Mode 1: RXFIFO[31:0] = {12{FIFO_O[19]}, FIFO_O[19:0]} Mode 2: RXFIFO[31:0] = {FIFO_O[19:4], 16'h0} Mode 3: RXFIFO[31:0] = {16{FIFO_O[19]}, FIFO_O[19:4]}
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DIGITAL AUDIO FIFO STATUS REGISTER

Offset: 0x18			Register Name: DA_FSTA
Bit	Read/Write	Default	Description
31:29	/	/	/
28	R	1	TXE TX FIFO Empty 0: No room for new sample in TX FIFO 1: More than one room for new sample in TX FIFO (>= 1 word)
27:24	/	/	/
23:16	R	0x80	TXE_CNT TX FIFO Empty Space Word Counter
15:9	/	/	/
8	R	0	RXA RX FIFO Available 0: No available data in RX FIFO 1: More than one sample in RX FIFO (>= 1 word)
7	/	/	/
6:0	R	0	RXA_CNT RX FIFO Available Sample Word Counter

DIGITAL AUDIO DMA & INTERRUPT CONTROL REGISTER

Offset: 0x1C			Register Name: DA_INT
			Default Value: 0x0000_0000

Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0	<p>TX_DRQ</p> <p>TX FIFO Empty DRQ Enable</p> <p>0: Disable</p> <p>1: Enable</p>
6	R/W	0	<p>TXUI_EN</p> <p>TX FIFO Under run Interrupt Enable</p> <p>0: Disable</p> <p>1: Enable</p>
5	R/W	0	<p>TXOI_EN</p> <p>TX FIFO Overrun Interrupt Enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>When set to '1', an interrupt happens when writing new audio data if TX FIFO is full.</p>
4	R/W	0	<p>TXEI_EN</p> <p>TX FIFO Empty Interrupt Enable</p> <p>0: Disable</p> <p>1: Enable</p>
3	R/W	0	<p>RX_DRQ</p> <p>RX FIFO Data Available DRQ Enable</p> <p>0: Disable</p> <p>1: Enable</p> <p>When set to '1', RXFIFO DMA Request line is asserted if Data is available in RX FIFO.</p>
2	R/W	0	<p>RXUI_EN</p> <p>RX FIFO Under run Interrupt Enable</p> <p>0: Disable</p> <p>1: Enable</p>

1	R/W	0	RXOI_EN RX FIFO Overrun Interrupt Enable 0: Disable 1: Enable
0	R/W	0	RXAI_EN RX FIFO Data Available Interrupt Enable 0: Disable 1: Enable

DIGITAL AUDIO INTERRUPT STATUS REGISTER

Offset: 0x20			Register Name: DAISTA
Default Value: 0x0000_0010			
Bit	Read/Write	Default	Description
31:7	/	/	/
6	R/W	0	TXU_INT TX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1: FIFO Under run Pending Interrupt
5	R/W	0	TXO_INT TX FIFO Overrun Pending Interrupt 0: No Pending Interrupt 1: FIFO Overrun Pending Interrupt Write '1' to clear this interrupt
4	R/W	1	TXE_INT TX FIFO Empty Pending Interrupt 0: No Pending IRQ 1: FIFO Empty Pending Interrupt Write '1' to clear this interrupt or automatic clear if interrupt condition fails.

3:2	/	/	/
2	R/W	0	<p>RXU_INT RX FIFO Under run Pending Interrupt 0: No Pending Interrupt 1:FIFO Under run Pending Interrupt</p> <p>Write 1 to clear this interrupt</p>
1	R/W	0	<p>RXO_INT RX FIFO Overrun Pending Interrupt 0: No Pending IRQ 1: FIFO Overrun Pending IRQ</p> <p>Write '1' to clear this interrupt</p>
0	R/W	0	<p>RXA_INT RX FIFO Data Available Pending Interrupt 0: No Pending IRQ 1: Data Available Pending IRQ</p> <p>Write '1' to clear this interrupt or automatic clear if interrupt condition fails.</p>

DIGITAL AUDIO CLOCK DIVIDE REGISTER

Offset: 0x24			Register Name: DA_CLKD
			Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:8	/	/	/
7	R/W	0	<p>MCLKO_EN 0: Disable MCLK Output 1: Enable MCLK Output</p> <p>Notes: Whether in Slave or Master mode, when this bit is set to 1, MCLK should be output.</p>
6:4	R/W	0	BCLKDIV

			BCLK Divide Ratio from MCLK 000: Divide by 2 (BCLK = MCLK/2) 001: Divide by 4 010: Divide by 6 011: Divide by 8 100: Divide by 12 101: Divide by 16 110: Divide by 32 111: Divide by 64
3:0	R/W	0	MCLKDIV MCLK Divide Ratio from Audio PLL Output 0000: Divide by 1 0001: Divide by 2 0010: Divide by 4 0011: Divide by 6 0100: Divide by 8 0101: Divide by 12 0110: Divide by 16 0111: Divide by 24 1000: Divide by 32 1001: Divide by 48 1010: Divide by 64 Others : Reserved

DIGITAL AUDIO TX COUNTER REGISTER

Offset: 0x28			Register Name: DA_TXCNT Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	R/W	0	TX_CNT

			<p>TX Sample Counter</p> <p>The audio sample number of sending into TXFIFO. When one sample is put into TXFIFO by DMA or by host IO, the TX sample counter register increases by one. The TX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.</p>
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DIGITAL AUDIO RX COUNTER REGISTER

Offset: 0x2C			Register Name: DA_RXCNT Default Value: 0x0000_0000
Bit	Read/Write	Default	Description
31:0	R/W	0	<p>RX_CNT</p> <p>RX Sample Counter</p> <p>The audio sample number of writing into RXFIFO. When one sample is written by Digital Audio Engine, the RX sample counter register increases by one. The RX sample counter register can be set to any initial value at any time. After been updated by the initial value, the counter register should count on base of this initial value.</p>

DIGITAL AUDIO TX CHANNEL SELECT REGISTER

Offset: 0x30			Register Name: DA_TXCHSEL Default Value: 0x0000_0001
Bit	Read/Write	Default	Description
31:3	/	/	/
2:0	R/W	1	<p>TX_CHSEL</p> <p>TX Channel Select</p> <p>0: 1-ch 1: 2-ch 2: 3-ch 3: 4-ch</p>

DIGITAL AUDIO TX CHANNEL MAPPING REGISTER

Offset: 0x34			Register Name: DA_TXCHMAP
Default Value: 0x7654_3210			
Bit	Read/Write	Default	Description
31:15	/	/	/
14:12	R/W	3	<p>TX_CH3_MAP</p> <p>TX Channel3 Mapping</p> <p>000: 1st sample</p> <p>001: 2nd sample</p> <p>010: 3rd sample</p> <p>011: 4th sample</p> <p>100: 5th sample</p> <p>101: 6th sample</p> <p>110: 7th sample</p> <p>111: 8th sample</p>
11	/	/	/
10:8	R/W	2	<p>TX_CH2_MAP</p> <p>TX Channel2 Mapping</p> <p>000: 1st sample</p> <p>001: 2nd sample</p> <p>010: 3rd sample</p> <p>011: 4th sample</p> <p>100: 5th sample</p> <p>101: 6th sample</p> <p>110: 7th sample</p> <p>111: 8th sample</p>
7	/	/	/
6:4	R/W	1	<p>TX_CH1_MAP</p> <p>TX Channel1 Mapping</p>

			000: 1 st sample 001: 2 nd sample 010: 3 rd sample 011: 4 th sample 100: 5 th sample 101: 6 th sample 110: 7 th sample 111: 8 th sample
3	/	/	/
2:0	R/W	0	TX_CH0_MAP TX Channel0 Mapping 000: 1 st sample 001: 2 nd sample 010: 3 rd sample 011: 4 th sample 100: 5 th sample 101: 6 th sample 110: 7 th sample 111: 8 th sample

DIGITAL AUDIO RX CHANNEL SELECT REGISTER

Offset: 0x38			Register Name: DA_RXCHSEL
			Default Value: 0x0000_0001
Bit	Read/Write	Default	Description
31:3	/	/	/
2:0	R/W	1	RX_CHSEL RX Channel Select 0: 1-ch 1: 2-ch

			2: 3-ch 3: 4-ch Others: Reserved
--	--	--	--

DIGITAL AUDIO RX CHANNEL MAPPING REGISTER

Offset: 0x3C			Register Name: DA_RXCHMAP
Bit	Read/Write	Default	Description
31:15	/	/	/
14:12	R/W	3	<p>RX_CH3_MAP</p> <p>RX Channel3 Mapping</p> <p>000: 1st sample</p> <p>001: 2nd sample</p> <p>010: 3rd sample</p> <p>011: 4th sample</p> <p>Others: Reserved</p>
11	/	/	/
10:8	R/W	2	<p>RX_CH2_MAP</p> <p>RX Channel2 Mapping</p> <p>000: 1st sample</p> <p>001: 2nd sample</p> <p>010: 3rd sample</p> <p>011: 4th sample</p> <p>Others: Reserved</p>
7	/	/	/
6:4	R/W	1	<p>RX_CH1_MAP</p> <p>RX Channel1 Mapping</p> <p>000: 1st sample</p> <p>001: 2nd sample</p>

			010: 3 rd sample 011: 4 th sample Others: Reserved
3	/	/	/
2:0	R/W	0	RX_CH0_MAP RX Channel0 Mapping 000: 1 st sample 001: 2 nd sample 010: 3 rd sample 011: 4 th sample Others: Reserved

7.7.6 Digital Audio Interface Special Requirement

DIGITAL AUDIO INTERFACE PIN LIST

Port Name	Width	Direction(M)	Description
DA_BCLK	1	IN/OUT	Digital Audio Serial Clock
DA_LRC	1	IN/OUT	Digital Audio Sample Rate Clock/ Sync
DA_SDO	1	OUT	Digital Audio Serial Data Output
DA_SDI	1	IN	Digital Audio Serial Data Input

DIGITAL AUDIO INTERFACE MCLK AND BCLK

The Digital Audio Interface can support sampling rates from 128fs to 768fs, where fs is the audio sampling frequency typically 32kHz, 44.1kHz, 48kHz or 96kHz. For different sampling frequency, the tables list the coefficient value of MCLKDIV and BCLKDIV.

Sampling Rate (kHz)	128fs	192fs	256fs	384fs	512fs	768fs
8	24	16	12	8	6	4
16	12	8	6	4	X	2
32	6	4	X	2	X	1
64	X	2	X	1	X	X
128	X	1	X	X	X	X
12	16	X	8	X	4	X
24	8	X	4	X	2	X
48	4	X	2	X	1	X
96	2	X	1	X	X	X
192	1	X	X	X	X	X

MCLKDIV value for 24.576MHz Audio Serial Frequency

Sampling Rate (kHz)	128fs	192fs	256fs	384fs	512fs	768fs
11.025	16	X	8	X	4	X
22.05	8	X	4	X	2	X
44.1	4	X	2	X	1	X
88.2	2	X	1	X	X	X
176.4	1	X	X	X	X	X

MCLKDIV value for 22.5792 MHz Audio Serial Frequency

Word Select Size	128fs	192fs	256fs	384fs	512fs	768fs
16	4	6	8	12	16	X
24	X	4	X	8	X	16
32	2	X	4	6	8	12

BCLKDIV value for Different Word Select Size

DIGITAL AUDIO INTERFACE CLOCK SOURCE AND FREQUENCY

There are two clocks for Digital Audio Interface. One is from APB bus and one is from Audio PLL.

Name	Description
Audio_PLL	24.576Mhz or 22.528Mhz generated by Audio PLL
APB_CLK	APB bus system clock. In I2S mode, it is requested ≥ 0.25 BCLK. In PCM mode, it is requested ≥ 0.5 BCLK.

7.8 Reduced Serial Bus

7.8.1 Overview

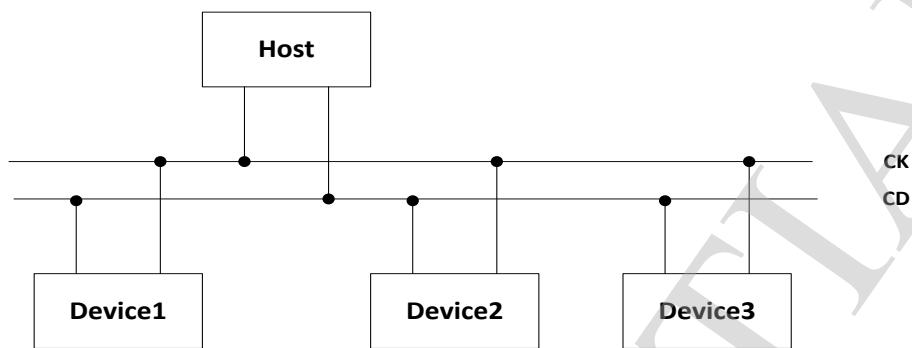
The RSBTM (Reduced Serial Bus) is a push-pull two wire bus developed by Allwinner Technology that supports multiple devices. It supports speed up to 20MHz.

It features:

- Support industry-standard AMBA Peripheral Bus (APB) and it is fully compliant with the AMBA Specification, Revision 2.0.
- Support speed up to 20MHz with lower power consumption
- Support Push-Pull bus
- Support Host mode
- Support multiple devices
- Support programmable output delay of CD signal
- Support parity check for address and data transmission

7.8.2 RSB Bus Topology

The bus topology is showed below:



Allwinner A23 User Manual

Errata Notice

This section contains all errata known at the date of issue in supported releases up to and including revision 1.0 of Allwinner A23 user manual.

It describes errata categorised by level of severity, which are:

Category 1 Behavior that is impossible to work around and that severely restricts the use of the product in all, or the majority of applications, rendering the device unusable.

Category 2 Behavior that contravenes the specified behavior and that might limit or severely impair the intended use of specified features, but does not render the product unusable in all or the majority of applications.

Category 3 Behavior that was not the originally intended behavior but should not cause any problems in applications.

Errata: Category 1

There are no errata in this category.

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Errata: Category 2

There are no errata in this category.

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Errata: Category 3

There are no errata in this category.

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Glossary

A

AES Advanced Encryption Standard A specification for the encryption of electronic data established by the U.S. National Institute of Standards and Technology (NIST) in 2001

AGC Automatic Gain Control An adaptive system found in electronic devices that automatically controls the gain of a signal: the average output signal level is fed back to adjust the gain to an appropriate level for a range of input signal levels.

AHB AMBA High-speed Bus A bus protocol introduced in Advanced Microcontroller Bus Architecture version 2 published by ARM Ltd company

APB Advanced Peripheral Bus APB is designed for low bandwidth control accesses, which has an address and data phase similar to AHB, but a much reduced, low complexity signal list (for example no bursts).

AVS Audio Video Standard A compression standard for digital audio and video

C

CIR Consumer IR The CIR (Consumer IR) interface is used for remote control through infra-red light

CRC Cyclic Redundancy Check A type of hash function used to produce a checksum in order to detect errors in data storage or transmission

CSI CMOS Sensor Interface The hardware block that interfaces with different image sensor interfaces and provides a standard output that can be used for subsequent image processing

D

DES Data Encryption Standard A previously predominant algorithm for the encryption of electronic data

DEU Detail Enhancement Unit A unit used for display engine frontend data post-processing

DLL Delay-Locked Loop A digital circuit similar to a phase-locked loop (PLL), with the main difference being the absence of an internal voltage-controlled oscillator, replaced by a delay line

DRC Dynamic Range Compression It reduces the volume of loud sounds or amplifies quiet sounds by narrowing or "compressing" an audio signal's dynamic range.

DVFS Dynamic Voltage Frequency Scaling and Dynamic voltage scaling is a power management technique where the voltage used in a component is increased or decreased, depending on circumstances. Dynamic frequency scaling is a technique whereby the frequency of a microprocessor can be automatically adjusted on the fly so that the power consumption or heat generated by the chip can be reduced. These two are often used together to save power in mobile devices.

E

EHCI Enhanced Host Controller Interface The register-level interface for a Host Controller for the USB Revision 2.0.

eMMC Embedded Multi-Media Card An architecture consisting of an embedded storage solution with MMC interface, flash memory and controller, all in a small BGA package

F

FBGA	Fine Ball Grid Array	FBGA is based on BGA technology, but comes with thinner contacts and is mainly used in SoC design
G		
GIC	Generic Interrupt Controller	A centralized resource for supporting and managing interrupts in a system that includes at least one processor
I		
IEP	Image Enhancement Processor	A unit used for the improvement of digital image quality, including DEU, DRC, CMU.
I2S	IIS	An electrical serial bus interface standard used for connecting digital audio devices together
L		
LSB	Least Significant Bit	The bit position in a binary integer giving the units value, that is, determining whether the number is even or odd. It is sometimes referred to as the right-most bit, due to the convention in positional notation of writing less significant digits further to the right.
LRADC	Low Resolution Analog to Digital Converter	A module which can transfer analog signals to digital signals
M		
MIPI DSI	MIPI Display Serial Interface	A specification by the Mobile Industry Processor Interface (MIPI) Alliance aimed at reducing the cost of display sub-systems in a mobile device
MSB	Most Significant Bit	The bit position in a binary number having the greatest value, which is sometimes referred to as the left-most bit due to the convention in positional notation of writing more significant

digits further to the left

N

NTSC National Television System Committee An analog television system that is used in most of North America, and many other countries

O

OHCI Open Host Controller Interface A register-level interface that enables a host controller for USB or FireWire hardware to communicate with a host controller driver in software

OSD

On-Screen Display

A feature of visual devices like VCRs and DVD players that displays program, position, and setting data on a connected TV or computer display

P

PAL

Phase Alternating Line

An analogue television color encoding system used in broadcast television systems in many countries

PCM

Pulse Code Modulation

A method used to digitally represent sampled analog signals

PID

Packet Identifier

Each table or elementary stream in a transport stream is identified by a 13-bit packet ID (PID). A demultiplexer extracts elementary streams from the transport stream in part by looking for packets identified by the same PID.

R

RSB

Reduced Serial Bus

A push-pull two wire bus invented by Allwinner Technology that supports speed up to 20MHz.

S

SPI	Synchronous Interface	Peripheral	A synchronous serial data link standard named by Motorola that operates in full duplex mode. Devices communicate in master/slave mode where the master device initiates the data frame
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T

TP	Touch Panel	A human-machine interactive interface
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TS

TS	Transport Stream	A data stream defined by ISO13818-1, which consists of one or more programs with video and audio data.
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U

USB OTG	Universal Serial Bus On-The-Go	A dual-role controller, which supports both Host and Device functions and is fully compliant with the On-The-Go Supplement to the USB 2.0 Specification, Revision 1.0a
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